



3.0MHz High Efficiency Low I_Q Synchronous Boost

Features

- Wide Input Voltage Range: 2.5V to 5.5V
- Output Voltage 5.4V
- Iout up to 1.0 A at Vout = 5.4 V, $V_{IN} \ge 3.0$ V
- 3MHz PWM Switching Frequency
- High Efficiency and Low Quiescent Current
 - Over 95% Efficiency
- ► 35µA Quiescent Current in Bypass Mode
- ► 55µA Quiescent Current in PFM Operation
- ±2% DC Voltage Accuracy in PWM mode
- Undervoltage Lockout (UVLO)
- Short Circuit Protection
- Hiccup Current Limit
- Over Temperature Protection
- Output Capacitor Pre-Charge and Soft-Start
- Pb-free 9-Bump, WLCSP 1.38mm x 1.38mm
- RoHS and Green Compliant
- -40°C to 85°C Operating Temperature Range

Applications

- Smartphones and Tablets
- Mobile Internet Devices
- USB OTG
- Wearables
- NFC Applications
- Portable Devices

Typical Application

Brief Description

The KTC2110A features a high-efficiency, micropower synchronous boost for Lithium-Ion/Polymer battery applications.

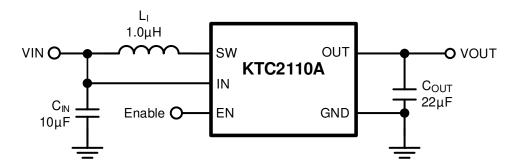
The KTC2110A achieves high efficiency over a wide output current range by operating in auto PWM/PFM control. The control method is automatically selected according to the output load conditions.

The KTC2110A also features Bypass Mode which allows passing input power directly to output with over current protection when EN pin is pulled LOW.

The constant on-time design does not require any external compensation components, simplifying the design and also provides ultra-fast transient response.

Inrush current-limiting feature is provided to reduce inrush current, which minimizes the voltage droop on the battery when the device is turned on.

The KTC2110A is packaged in advanced, RoHS and Green compliant, 1.38mm x 1.38mm, 9-balls Wafer-Level Chip-Scale Package (WLCSP).

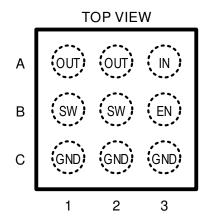


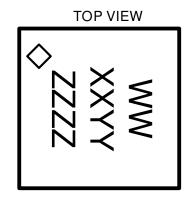


Pin Descriptions

| Pin # | Name | Function |
|------------|------|--|
| A1, A2 | OUT | Boost converter output |
| A3 | IN | Power supply input |
| B1, B2 | SW | Boost switching node, connect to inductor |
| B3 | EN | Active high enable. If the EN pin is pulled HIGH, the device starts operating in Boost Mode. Once the EN pin is pulled LOW, the device is forced into Bypass Mode. |
| C1, C2, C3 | GND | Ground |

WLCSP-9





Top View 9-Bump 1.38mm x 1.38mm x 0.620mm WLCSP Package

Top Mark WW = Device ID Code XX = Date Code, YY = Assembly Code ZZZZ = Serial Number



Absolute Maximum Ratings¹

| Symbol | Description | Value | Units |
|---------------|--|-------------|-------|
| IN | Voltage on IN pin | -0.3 to 6 | V |
| OUT | OUT to GND | -0.3 to 6 | V |
| C)W | SW to GND DC | -0.3 to 7 | V |
| SW | SW to GND AC Transient: 10 ns, 3 MHz | -1.0 to 8.7 | V |
| EN | EN to GND | -0.3 to 6 | V |
| Input Current | Continuous average current into SW | 3.0 | А |
| Input Current | Peak current into SW | 3.5 | А |
| TJ | Junction Operating Temperature Range | -40 to 150 | °C |
| Ts | Storage Temperature Range | -65 to 150 | °C |
| TLEAD | Maximum Soldering Temperature (at leads, 10 sec) | 260 | °C |

$(T_A = 25^{\circ}C \text{ unless otherwise noted})$

ESD Ratings

| Symbol | Description | Value | Units |
|---------|---|-------|-------|
| VESD | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 | ±2000 | V |
| Vesd_cd | Charged Device Model (CDM), per ANSI/ESDA/JEDEC JS-002-2018 | ±1000 | V |
| ILU | Latch-Up, per JEDEC STANDARD JESD78E | ±200 | mA |

Thermal Capabilities²

| Symbol | Description | Value | Units |
|-------------------------|---|-------|-------|
| Θја | Thermal Resistance – Junction to Ambient | 99.3 | °C/W |
| PD | Maximum Power Dissipation at 25°C | 1.69 | W |
| $\Delta P_D / \Delta_T$ | Derating Factor Above T _A = 25°C | -13.5 | mW/°C |

Ordering Information

| Part Number | V _{OUT} | Marking ³ | Operating Temperature | Package |
|-------------------|------------------|----------------------|--------------------------|-----------|
| KTC2110AECAA-D-TR | 5.40V | NWXXYYZZZZ | -40°C to +85°C | WLCSP33-9 |

^{1.} Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. Functional operation at conditions other than the operating conditions specified is not implied. Only one Absolute Maximum rating should be applied at any one time.

^{2.} Junction to Ambient thermal resistance is highly dependent on PCB layout. Values are based on thermal properties of the device when soldered to an EV board.

^{3.} XX = Date Code, YY = Assembly Code, ZZZZ = Serial Number.



Electrical Characteristics⁴

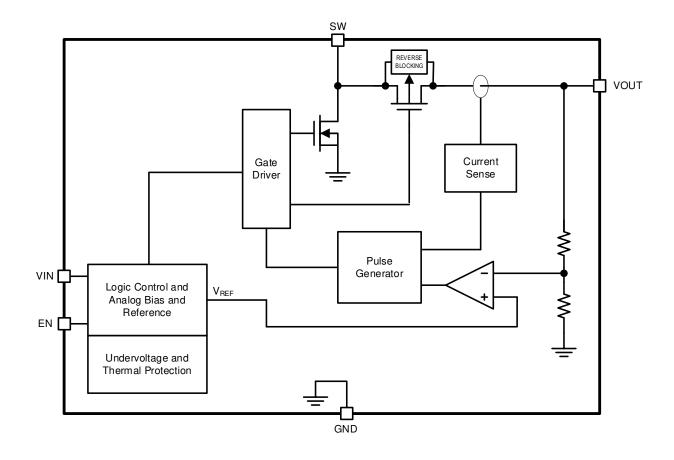
Unless otherwise noted, the *Min* and *Max* specs are applied over the full operation temperature range of -40°C to +85°C, $V_{IN} = 2.5V$ to 5.5V. Typical values are specified at room temperature (25°C) with $V_{IN} = 3.6V$, $V_{OUT} = 5.4V$, EN = High, $C_{OUT} = 22\mu$ F, L = 1.0 μ H and T_A = 25°C.

| Symbol | Description | Conditions | Min | Тур | Max | Units |
|--------------------------|--|--|------|------|------|-------|
| Supply Sp | ecifications | • | | | | |
| VIN | Input Voltage Range | | 2.5 | | 5.5 | V |
| Vuvlo | | V _{IN} Rising | 2.3 | 2.4 | 2.5 | V |
| | UVLO Threshold | V _{IN} Falling | | 100 | | mV |
| M | | V _{IN} Rising | 5.5 | 5.8 | 6.1 | V |
| Vovlo | OVLO Threshold | V _{IN} Falling | | 5.55 | | V |
| la | Input Quiescent Current | Non-Switching, $V_{EN} = High$ | | 55 | 80 | μA |
| Івур | Input Bypass Mode Current | $V_{EN}=0V;V_{IN}=5.5V$ | | 35 | 60 | μA |
| Enable Co | ntrol (EN) | · | | | • | |
| V _{TH-H} | EN pin logic high voltage | | 1.2 | | | V |
| $V_{\text{TH-L}}$ | EN pin logic low voltage | | | | 0.4 | V |
| l | Enable Low Leakage Current | $V_{EN} = 0V$ | | 0.01 | 0.1 | μA |
| IEN | Enable High Leakage Current | $V_{EN} = 1.8V$, Rpd = 1M Ω internally | | 2 | 3 | μA |
| Timing | | | | | • | |
| Ts | Soft-Start | EN H to Regulation, $R_L = Open$, V _{OUT} = 5.4V | | 330 | | μs |
| T _{RES} | Fault Restart Timer | | | 22 | | ms |
| Boost | | | | | | |
| ΔV_{OUT} | Output Voltage Accuracy | $V_{IN} = 2.5V$ to $4.5V$, $V_{OUT} = 5.4V$ | -2 | | 2 | % |
| Δ_{VOUT_LOAD} | Output Voltage Load Transient | $V_{IN} = 3.6V, V_{OUT} = 5.4V, I_{OUT} = 50mA$ to 1000mA | | 0.5 | | % |
| RDS(ON)P | High-Side P-Ch On-Resistance | $I_{SW} = 1A, V_{IN} = 5.0V$ | | 80 | | mΩ |
| RDS(ON)N | Low-Side N-Ch On-Resistance | $I_{SW}=-1A,\ V_{IN}=5.0V$ | | 80 | | mΩ |
| lsw_in | Leakage Current into SW | $V_{\text{IN}} = 5V, \ V_{\text{SW}} = 5V, \ V_{\text{EN}} = 0V$ | | 0.1 | 2 | μA |
| Isw_out | Leakage Current out of SW | $V_{\text{IN}}=5V,\ V_{\text{SW}}=0V,\ V_{\text{EN}}=0V$ | | 0.1 | 2 | μA |
| fosc | Frequency | $V_{IN} = 3.6V, Vo = 5.4V, Io = 1A$ | 2.64 | 3.0 | 3.36 | MHz |
| TON | Minimum On-Time | | | 40 | | ns |
| TOFF | Minimum OFF Time | | | 90 | | ns |
| Ilim | Switch Valley Current Limit | | | 2.3 | | Α |
| | Softstart Valley Current Limit | | | 1.5 | | Α |
| IPRE | Pre-charge Current Limit (Linear Mode) | | | 1.6 | | А |
| IC Therma | I Protection | | | | | |
| Тј_тн | Thermal Shutdown | T _J Rising | | 150 | | □C |
| | Thermal Hysteresis | TJ Falling | | 20 | | □C |
| | | • | | | | |

^{4.} KTC2110A is guaranteed to meet performance specifications over the -40°C to +85°C operating temperature range by design, characterization and correlation with statistical process controls.



Functional Block Diagram

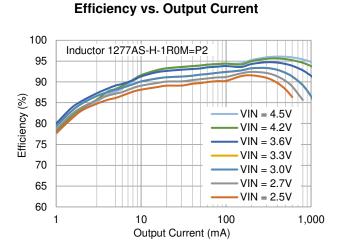




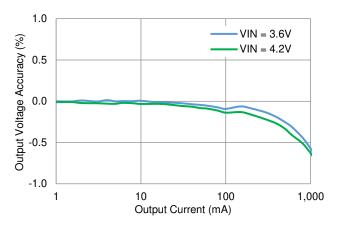
Typical Characteristics

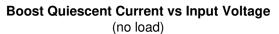
 V_{IN} = 3.6V, V_{OUT} = 5.4V, EN = High, C_{OUT} = 22 μ F, L = 1.0 μ H and T_A = 25°C unless otherwise specified.

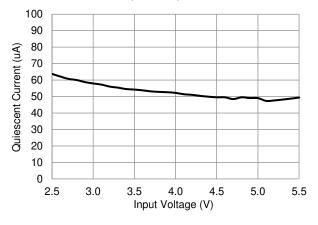
DC Typical Characteristics



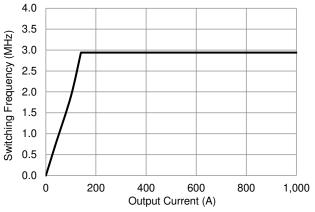
Output Voltage Accuracy vs Output Current



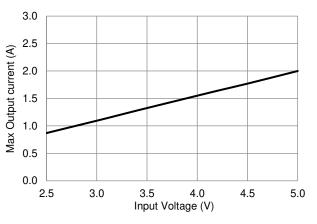




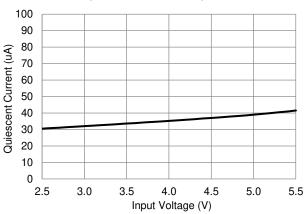
Switching Frequency vs. Output Current



Boost Max Output Current vs VIN



Bypass Mode Quiescent Current vs VIN (no load, EN = Low)

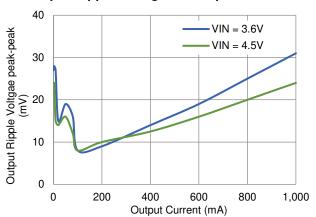




Typical Characteristics (continued)

 $V_{IN} = 3.6V$, $V_{OUT} = 5.4V$, EN = High, $C_{OUT} = 22\mu F$, $L = 1.0\mu H$ and $T_A = 25^{\circ}C$ unless otherwise specified.

DC Typical Characteristics



Output Ripple Voltage vs. Output Current



EN 5V / div

5V / div

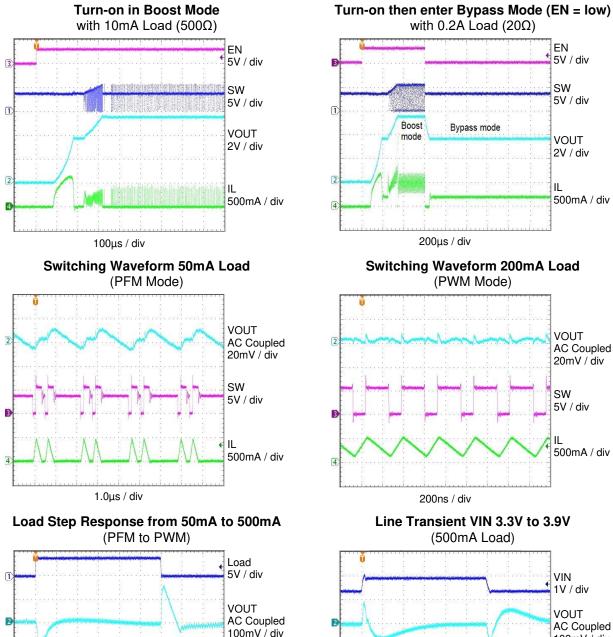
VOUT

SW

Typical Characteristics (continued)

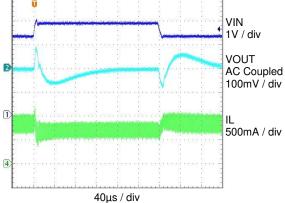
 $V_{IN} = 3.6V$, $V_{OUT} = 5V$, EN = High, $C_{OUT} = 22\mu F$, $L = 1.0\mu H$ and $T_A = 25^{\circ}C$ unless otherwise specified.

AC Typical Characteristics



IL 500mA / div

2V / div IL 500mA / div Switching Waveform 200mA Load (PWM Mode) VOUT AC Coupled 20mV / div SW 5V / div 11 500mA / div Line Transient VIN 3.3V to 3.9V (500mA Load)



20µs / div

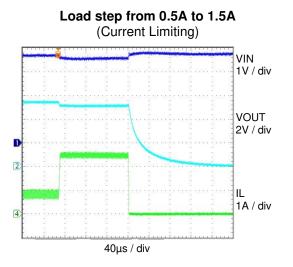
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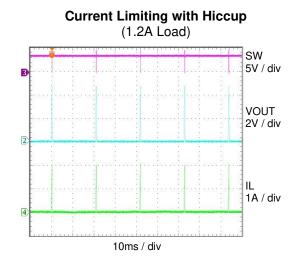


Typical Characteristics (continued)

 V_{IN} = 3.6V, V_{OUT} = 5V, EN = High, C_{OUT} = 22 μ F, L = 1.0 μ H and T_A = 25°C unless otherwise specified.

AC Typical Characteristics







Functional Description

Overview

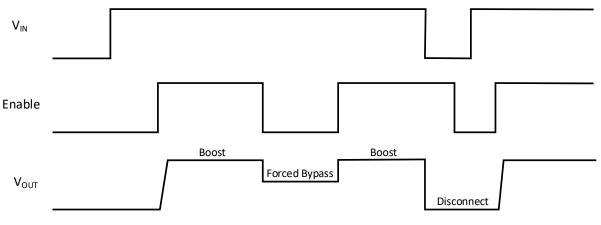
The KTC2110A is 3.0MHz synchronous boost converter with Boost Mode and Bypass Mode. In Boost Mode, KTC2110A works automatically in PFM/PWM control for the best efficiency under light load and achieving excellent line and load regulation under heavy load. KTC2110A can work in Bypass Mode by pulling EN to LOW. In Bypass Mode, V_{OUT} will be connected to V_{IN} through the high-side MOSFET.

For the best load transient performance, KTC2110A uses a constant on-time control. At the beginning of each switching cycle, the low-side switch is turned on for an adaptive on-time to ramp up inductor current. At the end of the on-time, the high-side switch is turned-on and the inductor current will decay to a value determined by compensation voltage. Finally, the switching cycle repeats by triggering the on timer again and activating the low-side switch.

Internal soft-start and loop compensation simplifies the design process while minimizing the number of external components.

Enable

User can force KTC2110A in Bypass Mode through the EN pin. If the EN pin is pulled HIGH, the device starts operating in Boost Mode. Once the EN pin is pulled LOW, the device is forced into Bypass Mode. To disable the device, the input supply voltage must be removed. The device cannot start-up in Bypass Mode. During start-up, keep the EN pulled HIGH for 1ms, before pulling it LOW and putting the device into Bypass Mode. The EN pin has an internal pull-down resistor (see Figure 1 for the sequence).





Boost Mode: Startup

The KTC2110A internal soft start circuit limits the inrush current during startup. The start-up first phase is Precharge, where the circuit takes about 200 μ s to ramp up the output voltage while the charging current increases within the 1.6A current limit. If after 200 μ s, the output voltage V_{OUT} is higher than 1V, the device keeps charging the output, otherwise a fault is declared. If the output voltage V_{OUT} reaches V_{IN}-0.3V within a 1ms charging time limit, the device enters the Soft-start phase, otherwise a fault is declared.

After successfully completing the Pre-charge phase, the next phase is Soft start where the boost regulator starts switching with 1.5A current limit. If the output V_{OUT} fails to reach regulation during soft start for more than 128us, a fault is triggered. For larger output capacitor C_{OUT} , the output voltage ramp up speed is slower to avoid excessive input current. During Soft start phase, if $V_{OUT} < V_{IN} - 0.3V$ and overcurrent is triggered, a fault will also be declared.

Boost Mode: Normal Operation

In Boost Mode, once Startup successfully finished, KTC2110A enters normal Operation. In Boost mode, KTC2110A can operate in Auto-Bypass when $V_{IN} > V_{OUT_NOM}$ and no switching is detected for 5us , the control



scheme keeps V_{OUT} following V_{IN}. As soon as V_{IN} falls below 0.98*V_{OUT_NOM}, it resumes normal boost operation. KTC2110A can smoothly switch between auto-bypass state and boost state to keep V_{OUT} within regulation targets. In Auto-Bypass state, if the condition V_{OUT} < V_{IN} - 0.3V occurs, a fault is declared. In boost state, the switch valley current limit is increased to 2.3A. If the current limit happens for longer than 150µs, a fault is declared.

The KTC2110A features a valley current limit sensing scheme. Current limit control happens during the off-time by sensing the voltage drop across the high-side FET. The output voltage will be reduced when current limit happens, because the power stage operates in a limited current mode. The maximum continuous output current lout_MAX can be defined by below formula.

(1)
$$I_{OUT_MAX} = (1-D) \bullet (IL_{VALLEY} + \frac{\Delta I_L}{2})$$

When the load current increases causing inductor valley current larger than the current limit threshold, the offtime is extended automatically to allow the inductor current to decrease to the valley current limit threshold before starting the next on-time cycle.

Bypass Mode:

In Bypass Mode (EN = 0), KTC2110A enters normal bypass operation where the High-Side MOSFET will be fully turned on. KTC2110A keeps the output voltage following the input voltage with only $35\mu A$ (typ) quiescent current. In this mode, if $V_{OUT} < V_{IN} - 0.3V$ is detected, a fault will be declared and the device will go back to shutdown mode (V_{OUT} disconnects with V_{IN}).

Fault State:

KTC2110A enters Fault State under any of the following conditions:

- 1. VOUT fails to achieve the voltage required during Boost Mode Pre-Charge Phase.
- 2. VOUT fails to reach regulation for 128us during Boost Mode Softstart Phase.
- 3. $V_{OUT} < V_{IN} 0.3V$ and overcurrent is triggered during Boost Mode Softstart Phase.
- 4. Boost current limit exceeded for 150us during Boost Mode Normal Operation.
- 5. V_{OUT} < V_{IN} 0.3V during Bypass Mode Normal Operation or Boost Mode Auto-Bypass State and Boost State.
- 6. V_{IN} < Input UVLO

Once a fault is triggered, the regulator stops switching and disconnects the path between V_{IN} and V_{OUT} . After 22ms hiccup period, it will automatically try to restart.

Thermal Shutdown

As soon as the junction temperature Tj is higher than 150°C (typ.), the device enters thermal shutdown mode where the power stage is turned-off. When Tj falls below 130°C (typ.), the device turns back on.





Application Information

Recommended PCB Layout

KTC2110A is a high frequency switching regulator. Therefore the traces must be kept as short as possible between the inductor and the device SW pin. The input bypass capacitor C_{IN} should be located as close as possible to the inductor and to the device in order to minimize the ripple voltage and improve the stability. The output capacitor should be located as close as possible to the IC in order to minimize the output ripple and improve the stability. It is recommended to connect both capacitors GND pads directly to the GND plane with a direct path to the device GND pins. Good layout practices should be used to avoid excessive noise spikes on SW pin which could cause voltages above Absolute Maximum Rating.

In order to support heavy load current and maximize the efficiency, it is important to keep traces wide on VIN, VOUT and on both sides of the inductor.

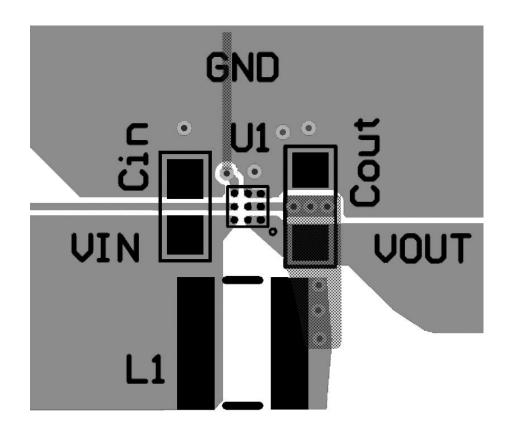
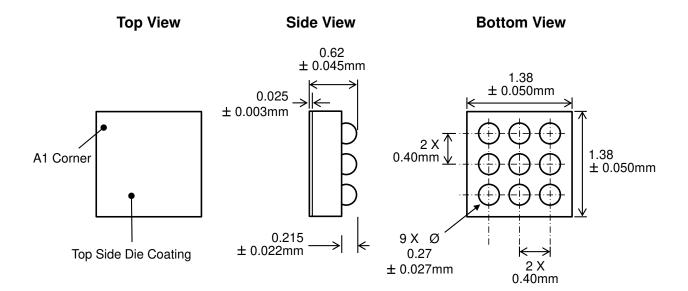


Figure 2. Recommended PCB Layout

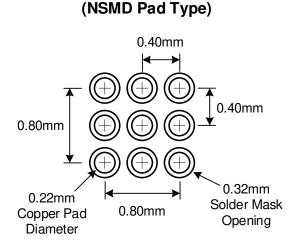


Packaging Information

WLCSP33-9 (1.38mm x 1.38mm x 0.620mm)



Recommended Footprint



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