TCAN1462-Q1 and TCAN1462V-Q1 Automotive Fault-Protected CAN FD Transceiver with Signal Improvement Capability (SIC) and Standby Mode

1 Features

- AEC Q100 (Grade 1): Qualified for automotive applications
- Functional Safety-Capable
  - Documentation available to aid functional safety system design
- Meets the requirements of ISO 11898-2:2016 and CiA 601-4 standards
- Classical CAN and CAN FD up to 8 Mbps
  - Actively improves the bus signal by reducing ringing effects in complex topologies
  - Backward compatible for use in classic CAN networks
- V_{IO} level shifting supports: 1.7 V to 5.5 V
- Operating Modes
  - Normal mode
  - Low-power standby mode supporting remote wake-up request
- Passive behavior when unpowered
  - Bus and logic terminals are high impedance (no load to operating bus or application)
  - Hot plug capable: power up or down glitch free operation on bus and RXD output
  - Defined device behavior with floating logic pins and in undervoltage supply conditions
- Protection features
  - IEC ESD protection on bus pins
  - ±58 V CAN bus fault tolerant
  - Undervoltage protection on V_{CC} and V_{IO} (V variants only) supply terminals
  - TXD dominant state timeout (TXD DTO)
  - Thermal shutdown protection (TSD)
- Available in SOIC (8), small footprint SOT-23 (8) and leadless 3mm x 3mm VSON (8) package with wettable flanks for improved automated optical inspection (AOI) capability

2 Applications

- Automotive gateway
- Advanced driver assistance system (ADAS)
- Body electronics and lighting
- Hybrid, electric & powertrain systems
- Automotive infotainment & cluster

3 Description

The TCAN1462-Q1 and TCAN1462V-Q1 are high speed Controller Area Network (CAN) transceivers that meet the physical layer requirements of the ISO 11898-2:2016 high speed CAN specification and the CiA 601-4 Signal Improvement Capability (SIC) specification. The devices reduce signal ringing at dominant-to-recessive edge and enable higher throughput in complex network topologies. Signal improvement capability allows the applications to extract real benefit of CAN FD (flexible data rate) by operating at 2 Mbps, or operating at 5 Mbps or higher in large networks with multiple unterminated stubs.

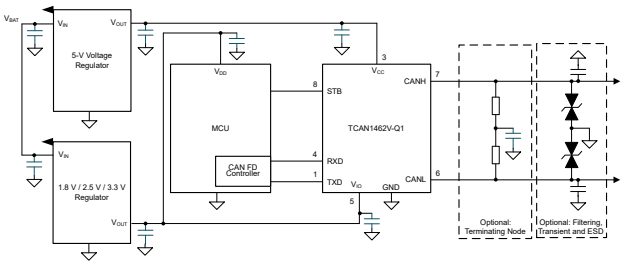
The devices meet the timing specifications mandated by CiA 601-4; thus, have much tighter bit timing symmetry compared to a regular CAN FD transceivers. This provides larger timing window to sample the correct bit and enables error-free communication in large complex star networks where ringing and bit distortion are inherent.

These devices are pin-compatible to 8-pin CAN FD transceivers, such as TCAN1044A-Q1 or TCAN1042-Q1.

Package Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
TCAN1462(V)-Q1	SOT-23 (DDF)	2.90 mm x 1.60 mm
	VSON (DRB)	3.00 mm x 3.00 mm
	SOIC (D)	4.90 mm x 3.91 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Block Diagram

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4 Revision History

Changes from Revision * (February 2022) to Revision A (June 2022)	Page
• Changed the data sheet from *Advanced information* to *Production* data	1

5 Description Continued

The TCAN1462-Q1 devices with suffix 'V' include internal logic level translation via the V_{IO} logic supply terminal to allow for interfacing directly to 1.8 V, 2.5 V, or 3.3 V controllers. The transceivers support low power standby mode which allows remote wake-up via CAN bus compliant with ISO 11898-2:2016 defined wake-up pattern (WUP). The device family also includes many protection features such as undervoltage detection, thermal shutdown (TSD), driver dominant timeout (TXD DTO), and ±58 V bus fault protection.

6 Device Comparison Table

Device Number	Bus Fault Protection	Low voltage I/O Logic Support on Pin 5	Pin 8 Mode Selection
TCAN1462-Q1	± 58 V	No	Low Power Standby Mode with Remote Wake
TCAN1462V-Q1	± 58 V	Yes	

7 Pin Configurations and Functions

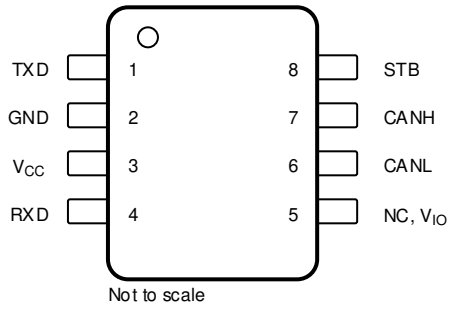


Figure 7-1. SOIC (D) and SOT-23 (DDF) Package, 8 Pin (Top View)

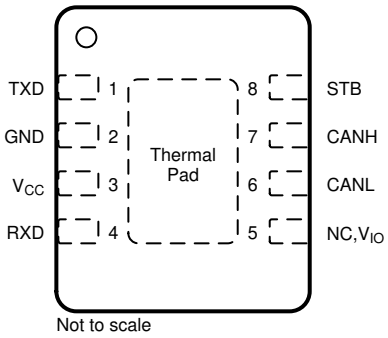


Figure 7-2. VSON (DRB) Package, 8 Pin (Top View)

Table 7-1. Pin Functions

PINS		TYPE	DESCRIPTION
NAME	NO.		
TXD	1	Digital Input	CAN transmit data input, integrated pull-up
GND	2	GND	Ground connection
V_{CC}	3	Supply	5 V supply voltage
RXD	4	Digital Output	CAN receive data output, tristate when powered off
V_{IO}	5	Supply	Logic supply voltage
NC		--	No Connect (not internally connected); Devices without V_{IO}
CANL	6	Bus IO	Low-level CAN bus input/output line
CANH	7	Bus IO	High-level CAN bus input/output line
STB	8	Digital Input	Standby mode control input, integrated pull-up
Thermal Pad (VSON only)	—		Electrically connected to GND, connect the thermal pad to the printed circuit board (PCB) ground plane for thermal relief

8 Specifications

8.1 Absolute Maximum Ratings

(1) (2)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	–0.3	6	V
V_{IO}	Supply voltage IO level shifter (Devices with the "V" suffix)	–0.3	6	V
V_{BUS}	CAN bus IO voltage range on CANH and CANL	–58	58	V
V_{DIFF}	Max differential voltage between CANH and CANL V_{DIFF} = (CANH - CANL)	–45	45	V
V_{Logic_Input}	Logic pin input voltage (TXD, STB)	–0.3	6	V
V_{RXD}	Logic output voltage range (RXD)	–0.3	6	V
$I_{O(RXD)}$	RXD output current	–8	8	mA
T_J	Junction temperature	–40	165	°C
T_{STG}	Storage temperature	–65	165	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values, except differential I/O bus voltages, are with respect to ground terminal.

8.2 ESD Ratings

				VALUE	UNIT
V_{ESD}	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	HBM classification level 3A for all pins	±4000	V
			HBM classification level 3B for global pins CANH and CANL with respect to GND	±10000	V
		Charged-device model (CDM), per AEC Q100-011 CDM classification level C5 for all pins		±750	V

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

8.3 ESD Ratings, IEC Transients

				VALUE	UNIT
V_{ESD}	System level electrostatic discharge	CAN bus terminals (CANH, CANL) to GND	SAE J2962-2 per ISO 10605 Powered contact discharge	±8000	V
			SAE J2962-2 per ISO 10605 Powered air discharge	±15000	V
			IEC 62228-3 per ISO 10605	±8000	V
V_{Tran}	ISO 7637-2 Transient immunity(1)		Pulse 1	–100	V
			Pulse 2a	75	V
			Pulse 3a	–150	V
			Pulse 3b	100	V
	Direct capacitor coupling, SAE J2962-2 per ISO 7637-3(2)		DCC slow transient pulse	±30	V

(1) Tested according to IEC 62228-3:2019 CAN Transceivers, Section 6.3; standard pulses parameters defined in ISO 7637-2 (2011)
(2) Tested according to SAE J2962-2

8.4 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IO}	Supply voltage for IO level shifter (Devices with V_{IO})	1.7		5.5	V
$I_{OH(RXD)}$	RXD terminal high-level output current	–1.5			mA
$I_{OL(RXD)}$	RXD terminal low-level output current			1.5	mA
T_J	Junction temperature	–40		150	°C

8.5 Thermal Characteristics

THERMAL METRIC(1)		TCAN1462(V)-Q1			UNIT
		D (SOIC)	DDF (SOT)	DRB (VSON)	
$R_{\Theta JA}$	Junction-to-ambient thermal resistance	120	115.3	52.8	°C/W
$R_{\Theta JC(top)}$	Junction-to-case (top) thermal resistance	57.8	56.2	58.9	°C/W
$R_{\Theta JB}$	Junction-to-board thermal resistance	64.2	38	25.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	13.1	1.8	1.8	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	63.3	37.7	25.2	°C/W
$R_{\Theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	-	–	9.3	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

8.6 Supply Characteristics

parameters valid over recommended operating conditions with -40°C ≤ T_J ≤ 150°C (Typical values are at V_{CC} = 5 V, V_{IO} = 3.3 V (for devices with V_{IO}), Device ambient maintained at 27°C) unless otherwise noted

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC}	Supply current normal mode	Dominant	TXD = 0 V, STB = 0 V R_L = 60 Ω, C_L = open See Figure 9-1		45	70	mA
		Dominant	TXD = 0 V, STB = 0 V R_L = 50 Ω, C_L = open See Figure 9-1		49	80	mA
		Recessive	TXD = V_{IO}, STB = 0 V R_L = 50 Ω, C_L = open See Figure 9-1		4.5	8	mA
		Dominant with bus fault	TXD = 0 V, STB = 0 V CANH = CANL = ±25 V R_L = open, C_L = open See Figure 9-1			130	mA
	Supply current standby mode (devices with V_{IO})		TXD = STB = V_{IO} , R_L = 50 Ω, C_L = open, Tj <= 85 °C, See Figure 9-1			0.6	µA
			TXD = STB = V_{IO} , R_L = 50 Ω, C_L = open, Tj <= 125 °C, See Figure 9-1		0.2	2	
			TXD = STB = V_{IO} , R_L = 50 Ω, C_L = open, Tj <= 150 °C, See Figure 9-1			5	
	Supply current standby mode (devices without V_{IO})		TXD = STB = V_{CC} , R_L = 50 Ω, C_L = open, Tj <= 85 °C, See Figure 9-1			14	µA
			TXD = STB = V_{CC} , R_L = 50 Ω, C_L = open, Tj <= 125 °C, See Figure 9-1			16	
			TXD = STB = V_{CC} , R_L = 50 Ω, C_L = open, Tj <= 150 °C, See Figure 9-1			21	

8.6 Supply Characteristics (continued)

parameters valid over recommended operating conditions with -40°C ≤ T_J ≤ 150°C (Typical values are at V_{CC} = 5 V, V_{IO} = 3.3 V (for devices with V_{IO}), Device ambient maintained at 27°C) unless otherwise noted

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IO} Devices with V_{IO}	IO supply current normal mode	Dominant	TXD = 0 V, STB = 0 V R_L = 60 Ω, C_L = open RXD floating		125	300	µA
		Recessive	TXD = V_{IO}, STB = 0 V R_L = 60 Ω, C_L = open RXD floating		25	48	µA
	IO supply current standby mode		TXD = V_{IO}, STB = V_{IO} R_L = 60 Ω, C_L = open RXD floating, Tj <= 85 °C			13.5	µA
			TXD = V_{IO}, STB = V_{IO} R_L = 60 Ω, C_L = open RXD floating, Tj <= 125 °C		8.5	15	
			TXD = V_{IO}, STB = V_{IO} R_L = 60 Ω, C_L = open RXD floating, Tj <= 150 °C			16	
$UV_{CC(R)}$	Undervoltage detection V_{CC} rising		Ramp up		4.2	4.4	V
$UV_{CC(F)}$	Undervoltage detection on V_{CC} falling		Ramp down	3.5	4		V
$UV_{IO(R)}$	Undervoltage detection V_{IO} rising (Devices with V_{IO})		Ramp up		1.6	1.65	V
$UV_{IO(F)}$	Undervoltage detection on V_{IO} falling (Devices with V_{IO})		Ramp down	1.4	1.5		V

8.7 Dissipation Ratings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_D	Average power dissipation Normal mode	V_{CC} = 5 V, V_{IO} = 3.3 V, T_J = 27°C, R_L = 60Ω, C_{L_RXD} = 15 pF TXD input = 250 kHz 50% duty cycle square wave		60		mW
		V_{CC} = 5.5 V, V_{IO} = 5.5 V, T_J = 150°C, R_L = 50Ω, C_{L_RXD} = 15 pF TXD input = 2.5 MHz 50% duty cycle square wave		120		mW
T_{TSD}	Thermal shutdown temperature			192		°C
T_{TSD_HYS}	Thermal shutdown hysteresis			10		

8.8 Electrical Characteristics

parameters valid over recommended operating conditions with -40°C ≤ T_J ≤ 150°C (Typical values are at V_{CC} = 5 V, V_{IO} = 3.3 V, Device ambient maintained at 27°C) unless otherwise noted

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
Driver Electrical Characteristics							
$V_{O(DOM)}$	Dominant output voltage normal mode	CANH	TXD = 0 V, STB = 0 V 50 Ω ≤ R_L ≤ 65 Ω, C_L = open, See Figure 9-2 and Figure 10-5	2.75		4.5	V
		CANL		0.5		2.25	V
$V_{O(REC)}$	Recessive output voltage normal mode	CANH and CANL	TXD = V_{IO}, STB = 0 V R_L = open (no load), C_L = open, See Figure 9-2 and Figure 10-5	2	0.5 V_{CC}	3	V
V_{SYM}	Driver symmetry ($V_{O(CANH)}$ + $V_{O(CANL)}$)/V_{CC}		TXD = 250 kHz, 1 MHz, 2.5 MHz, STB = 0 V R_L = 60, C_{SPLIT} = 4.7 nF, C_L = open, See Figure 9-2 and Figure 11-2	0.9		1.1	V/V
V_{SYM_DC}	DC output symmetry (V_{CC} - $V_{O(CANH)}$ - $V_{O(CANL)}$)		STB = 0 V R_L = 60 Ω, C_L = open, See Figure 9-2 and Figure 10-5	–400		400	mV
$R_{ID(DOM)}$	Differential input resistance in dominant phase		TXD= 0 V, STB = 0 V, See Figure 10-2		40		Ω

8.8 Electrical Characteristics (continued)

parameters valid over recommended operating conditions with -40℃ ≤ T_J ≤ 150℃ (Typical values are at V_{CC} = 5 V, V_{IO} = 3.3 V, Device ambient maintained at 27℃) unless otherwise noted

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{ID(ACTIVE\_REC)}$	Differential input resistance in active recessive drive phase		Duration from TXD low-to-high edge to elapse of active recessive drive period ($t_{SIC\_TX\_base}$), See Figure 10-2		100		Ω
$V_{OD(DOM)}$	Differential output voltage normal mode Dominant	CANH - CANL	TXD = 0 V, STB = 0 V 50 Ω ≤ R_L ≤ 65 Ω, C_L = open, See Figure 9-2 and Figure 10-5	1.5		3	V
			TXD = 0 V, STB = 0 V 45 Ω ≤ R_L ≤ 70 Ω, C_L = open, See Figure 9-2 and Figure 10-5	1.4		3.3	V
			TXD = 0 V, STB = 0 V R_L = 2240 Ω, C_L = open, See Figure 9-2 and Figure 10-5	1.5		5	V
$V_{OD(REC)}$	Differential output voltage normal mode Recessive	CANH - CANL	TXD = V_{IO}, STB = 0 V R_L = 60 Ω, C_L = open, See Figure 9-2 and Figure 10-5	–120		12	mV
			TXD = V_{IO}, STB = 0 V R_L = open, C_L = open, See Figure 9-2 and Figure 10-5	–50		50	mV
$V_{O(STB)}$	Bus output voltage standby mode	CANH	TXD = STB = V_{IO} R_L = open , C_L = open, See Figure 9-2 and Figure 10-5	-0.1		0.1	V
		CANL		-0.1		0.1	V
		CANH - CANL		-0.2		0.2	V
I_{OS}	Short-circuit bus output current, TXD is dominant or recessive or toggling, normal mode		$V_{(CANH)}$ = -15 V to 40 V, CANL = open, TXD = 0 V or V_{IO} or 250 kHz, 2.5 MHz square wave, See Figure 9-7 and Figure 10-5	–115		115	mA
			$V_{(CAN\_L)}$ = -15 V to 40 V, CANH = open, TXD = 0 V or V_{IO} or 250 kHz, 2.5 MHz square wave, See Figure 9-7 and Figure 10-5	–115		115	mA
Receiver Electrical Characteristics							
V_{IT}	Input threshold voltage normal mode		-12 V ≤ V_{CM} ≤ 12 V, STB= 0 V, See Figure 9-3 and Table 10-6	500		900	mV
$V_{IT(STB)}$	Input threshold standby mode		-12 V ≤ V_{CM} ≤ 12 V, STB= V_{IO} , See Figure 9-3 and Table 10-6	400		1150	mV
V_{DOM}	Normal mode dominant state differential input voltage range		-12 V ≤ V_{CM} ≤ 12 V, STB= 0 V, See Figure 9-3 and Table 10-6	0.9		9	V
V_{REC}	Normal mode recessive state differential input voltage range		-12 V ≤ V_{CM} ≤ 12 V , STB= 0 V, See Figure 9-3 and Table 10-6	-4		0.5	V
$V_{DOM(STB)}$	Standby mode dominant state differential input voltage range		STB = V_{IO}, -12 V ≤ V_{CM} ≤ 12 V, See Figure 9-3 and Table 10-6	1.15		9	V
$V_{REC(STB)}$	Standby mode recessive state differential input voltage range		STB = V_{IO}, -12 V ≤ V_{CM} ≤ 12 V, See Figure 9-3 and Table 10-6	-4		0.4	V
V_{HYS}	Hysteresis voltage for input threshold normal mode		-12 V ≤ V_{CM} ≤ 12 V, STB= 0 V, See Figure 9-3 and Table 10-6		100		mV
V_{CM}	Common mode range normal and standby modes		See Figure 9-3 and Table 10-6	–12		12	V
$I_{LKG(IOFF)}$	Unpowered bus input leakage current		CANH = CANL = 5 V, V_{CC} = V_{IO} = GND			5	µA
C_I	Input capacitance to ground (CANH or CANL)		TXD = V_{IO}			40	pF
C_{ID}	Differential input capacitance					20	pF
R_{ID}	Differential input resistance		TXD = V_{IO}, STB = 0 V -12 V ≤ V_{CM} ≤ 12 V, Delta V/Delta I	40		90	kΩ
R_{IN}	Single ended input resistance (CANH or CANL)			20		45	kΩ
$R_{IN(M)}$	Input resistance matching [1 – ($R_{IN(CANH)}$ / $R_{IN(CANL)}$)] × 100 %		$V_{(CAN\_H)}$ = $V_{(CAN\_L)}$ = 5 V	–1		1	%
TXD Terminal (CAN Transmit Data Input)							
V_{IH}	High-level input voltage		Devices without V_{IO}	0.7 V_{CC}			V
V_{IH}	High-level input voltage		Devices with V_{IO}	0.7 V_{IO}			V

8.8 Electrical Characteristics (continued)

parameters valid over recommended operating conditions with -40°C ≤ T_J ≤ 150°C (Typical values are at V_{CC} = 5 V, V_{IO} = 3.3 V, Device ambient maintained at 27°C) unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IL}	Low-level input voltage	Devices without V_{IO}			0.3 V_{CC}	V
V_{IL}	Low-level input voltage	Devices with V_{IO}			0.3 V_{IO}	V
I_{IH}	High-level input leakage current	TXD = V_{CC} = V_{IO} = 5.5 V	–2.5	0	1	µA
I_{IL}	Low-level input leakage current	TXD = 0 V, V_{CC} = V_{IO} = 5.5 V	–200	-100	–20	µA
$I_{LKG(OFF)}$	Unpowered leakage current	TXD = 5.5 V, V_{CC} = V_{IO} = 0 V	–1	0	1	µA
C_I	Input capacitance	V_{IN} = 0.4×sin(2×π×2×10^6×t)+2.5 V		5		pF
RXD Terminal (CAN Receive Data Output)						
V_{OH}	High-level output voltage	Devices without V_{IO} I_O = –1.5 mA, See Figure 9-3	0.8 V_{CC}			V
V_{OH}	High-level output voltage	I_O = –1.5 mA, Devices with V_{IO} See Figure 9-3	0.8 V_{IO}			V
V_{OL}	Low-level output voltage	Devices without V_{IO} I_O = 1.5 mA, See Figure 9-3			0.2 V_{CC}	V
V_{OL}	Low-level output voltage	Devices with V_{IO} I_O = 1.5 mA, Devices with V_{IO} See Figure 9-3			0.2 V_{IO}	V
$I_{LKG(OFF)}$	Unpowered leakage current	RXD = 5.5 V, V_{CC} = V_{IO} = 0 V	–1	0	1	µA
STB Terminal (Standby Mode Input)						
V_{IH}	High-level input voltage	Devices without V_{IO}	0.7 V_{CC}			V
V_{IH}	High-level input voltage	Devices with V_{IO}	0.7 V_{IO}			V
V_{IL}	Low-level input voltage	Devices without V_{IO}			0.3 V_{CC}	V
V_{IL}	Low-level input voltage	Devices with V_{IO}			0.3 V_{IO}	V
I_{IH}	High-level input leakage current	V_{CC} = V_{IO} = STB = 5.5 V	–2		2	µA
I_{IL}	Low-level input leakage current	V_{CC} = V_{IO} = 5.5 V, STB = 0 V	–20		–2	µA
$I_{LKG(OFF)}$	Unpowered leakage current	STB = 5.5V, V_{CC}= V_{IO} = 0 V	–1	0	1	µA

8.9 Switching Characteristics

parameters valid over recommended operating conditions with -40°C ≤ T_J ≤ 150°C (Typical values are at V_{CC} = 5 V, V_{IO} = 3.3 V, Device ambient maintained at 27°C) unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Device Switching Characteristics						
$t_{PROP(LOOP1)}$	Total loop delay, driver input (TXD) to receiver output (RXD), recessive to dominant	See Figure 9-4 , normal mode, V_{IO} = 4.5 V to 5.5 V, R_L = 60 Ω, C_L = 100 pF, $C_{L(RXD)}$ = 15 pF		95	145	ns
		See Figure 9-4 , normal mode, V_{IO} = 3 V to 3.6 V, R_L = 60 Ω, C_L = 100 pF, $C_{L(RXD)}$ = 15 pF		100	155	ns
		See Figure 9-4 , normal mode, V_{IO} = 2.25 V to 2.75 V, R_L = 60 Ω, C_L = 100 pF, $C_{L(RXD)}$ = 15 pF		105	170	ns
		See Figure 9-4 , normal mode, V_{IO} = 1.71 V to 1.89 V, R_L = 60 Ω, C_L = 100 pF, $C_{L(RXD)}$ = 15 pF		120	190	ns

8.9 Switching Characteristics (continued)

parameters valid over recommended operating conditions with -40℃ ≤ T_J ≤ 150℃ (Typical values are at V_{CC} = 5 V, V_{IO} = 3.3 V, Device ambient maintained at 27℃) unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PROP(LOOP2)}$	Total loop delay, driver input (TXD) to receiver output (RXD), dominant to recessive	See Figure 9-4 , normal mode, V_{IO} = 4.5 V to 5.5 V, R_L = 60 Ω, C_L = 100 pF, $C_{L(RXD)}$ = 15 pF		110	150	ns
		See Figure 9-4 , normal mode, V_{IO} = 3 V to 3.6 V, R_L = 60 Ω, C_L = 100 pF, $C_{L(RXD)}$ = 15 pF		115	160	ns
		See Figure 9-4 , normal mode, V_{IO} = 2.25 V to 2.75 V, R_L = 60 Ω, C_L = 100 pF, $C_{L(RXD)}$ = 15 pF		120	175	ns
		See Figure 9-4 , normal mode, V_{IO} = 1.71 V to 1.89 V, R_L = 60 Ω, C_L = 100 pF, $C_{L(RXD)}$ = 15 pF		135	190	ns
t_{MODE}	Mode change time, from normal to standby or from standby to normal	See Figure 9-5			30	µs
t_{WK_FILTER}	Filter time for a valid wake-up pattern	See Figure 10-7	0.5		1.8	µs
$t_{WK\_TIMEOUT}$	Bus wake-up timeout value	See Figure 10-7	0.8		6	ms
Tstartup	Time duration after V_{CC} or V_{IO} hass cleared rising undervoltage threshold, and device can resume normal operation				1.5	ms
$T_{filter(STB)}$	Filter on STB pin to filter out any glitches		0.5	1	2	µs
Driver Switching Characteristics						
$t_{prop(TxD-busrec)}$	Propagation delay time, low-to-high TXD edge to driver recessive (dominant to recessive)	See Figure 9-2 , STB = 0 V, R_L = 60 Ω, C_L = 100 pF, V_{IO} = 4.5 V to 5.5 V		50	70	ns
		See Figure 9-2 STB = 0 V, R_L = 60 Ω, C_L = 100 pF, V_{IO} = 3 V to 3.6 V		50	70	ns
		See Figure 9-2 STB = 0 V, R_L = 60 Ω, C_L = 100 pF, V_{IO} = 2.25 V to 2.75 V		55	75	ns
		See Figure 9-2 STB = 0 V, R_L = 60 Ω, C_L = 100 pF, V_{IO} = 1.71 V to 1.89 V		55	80	ns
$t_{prop(TxD-busdom)}$	Propagation delay time, high-to-low TXD edge to driver dominant (recessive to dominant)	See Figure 9-2 , STB = 0 V, R_L = 60 Ω, C_L = 100 pF, V_{IO} = 4.5 V to 5.5 V		45	75	ns
		See Figure 9-2 STB = 0 V, R_L = 60 Ω, C_L = 100 pF, V_{IO} = 3 V to 3.6 V		50	75	ns
		See Figure 9-2 STB = 0 V, R_L = 60 Ω, C_L = 100 pF, V_{IO} = 2.25 V to 2.75 V		50	80	ns
		See Figure 9-2 STB = 0 V, R_L = 60 Ω, C_L = 100 pF, V_{IO} = 1.71 V to 1.89 V		55	80	ns
$t_{sk(p)}$	Pulse skew ($\lvert t_{prop(TxD-busrec)} - t_{prop(TxD-busdom)} \rvert$)	STB = 0 V, R_L = 60 Ω, C_L = 100 pF, See Figure 9-2		3.5	10	ns
t_R	Differential output signal rise time	See Figure 9-2 , STB = 0 V, R_L = 60 Ω, C_L = 100 pF		20	30	ns
t_F	Differential output signal fall time	See Figure 9-2 , STB = 0 V, R_L = 60 Ω, C_L = 100 pF		30	40	ns
t_{TXD_DTO}	Dominant timeout	See Figure 9-6 , R_L = 60 Ω, C_L = 100 pF, STB = 0 V	1.2		4.0	ms
Receiver Switching Characteristics						
$t_{prop(busrec-RXD)}$	Propagation delay time, bus recessive input to RXD high output (dominant to recessive)	See Figure 9-3 , STB = 0 V, $C_{L(RXD)}$ = 15 pF, V_{IO} = 4.5 V to 5.5 V		60	85	ns
		See Figure 9-3 STB = 0 V, $C_{L(RXD)}$ = 15 pF, V_{IO} = 3 V to 3.6 V		65	95	ns
		See Figure 9-3 STB = 0 V, $C_{L(RXD)}$ = 15 pF, V_{IO} = 2.25 V to 2.75 V		70	105	ns
		See Figure 9-3 STB = 0 V, $C_{L(RXD)}$ = 15 pF, V_{IO} = 1.71 V to 1.89 V		80	110	ns

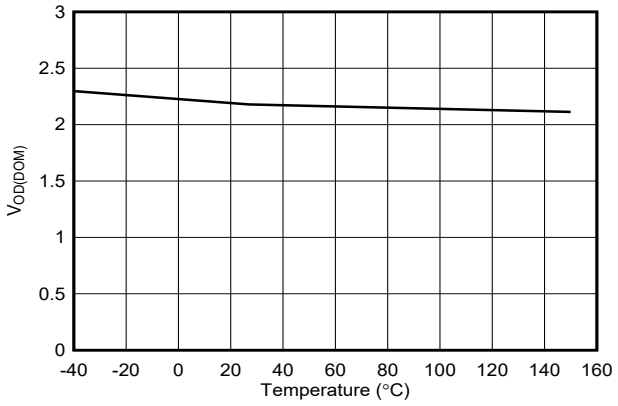
8.9 Switching Characteristics (continued)

parameters valid over recommended operating conditions with -40℃ ≤ T_J ≤ 150℃ (Typical values are at V_{CC} = 5 V, V_{IO} = 3.3 V, Device ambient maintained at 27℃) unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{prop(busdom-RXD)}$	Propagation delay time, bus dominant input to RXD low output (recessive to dominant)	See Figure 9-3 , STB = 0 V, $C_{L(RXD)}$ = 15 pF, V_{IO} = 4.5 V to 5.5 V		50	75	ns
		See Figure 9-3 STB = 0 V, $C_{L(RXD)}$ = 15 pF, V_{IO} = 3 V to 3.6 V		50	80	ns
		See Figure 9-3 STB = 0 V, $C_{L(RXD)}$ = 15 pF, V_{IO} = 2.25 V to 2.75 V		55	90	ns
		See Figure 9-3 STB = 0 V, $C_{L(RXD)}$ = 15 pF, V_{IO} = 1.71 V to 1.89 V		65	110	ns
t_R	RXD output signal rise time	See Figure 9-3 , STB = 0 V, $C_{L(RXD)}$ = 15 pF		8	20	ns
t_F	RXD output signal fall time			7	25	ns
Signal Improvement Timing Characteristics						
$t_{SIC\_TX\_base}$	Signal improvement time TX-based	Time from rising edge of the TXD signal to the end of the signal improvement phase	230	340	530	ns
$\Delta t_{Bit(Bus)}$	Transmitted bit width variation	TXD <= 5Mbps square wave, $\Delta t_{Bit(Bus)}$ = $t_{Bit(Bus)}$ - $t_{Bit(TxD)}$ STB = 0 V, R_L = 60 Ω, C_L = 100 pF, See Figure 9-4	–10		10	ns
$\Delta t_{BIT(RxD)}$	Received bit width variation	TXD <= 5Mbps square wave, $\Delta t_{Bit(RxD)}$ = $t_{Bit(RxD)}$ - $t_{Bit(TxD)}$ STB = 0 V, R_L = 60 Ω, C_L = 100 pF, $C_{L(RXD)}$ = 15 pF, See Figure 9-4	–30		20	ns
Δt_{REC}	Receiver timing symmetry	TXD <= 5Mbps square wave, Δt_{REC} = $t_{Bit(RxD)}$ - $t_{Bit(Bus)}$ STB = 0 V, $C_{L(RXD)}$ = 15 pF, See Figure 9-4	–20		15	ns
FD Timing Characteristics						
$t_{BIT(BUS)}$	Bit time on CAN bus output pins with $t_{BIT(TXD)}$ = 500 ns	See Figure 9-4 , STB = 0 V, R_L = 60 Ω, C_L = 100 pF, $C_{L(RXD)}$ = 15 pF	490		510	ns
	Bit time on CAN bus output pins with $t_{BIT(TXD)}$ = 200 ns		190		210	ns
	Bit time on CAN bus output pins with $t_{BIT(TXD)}$ = 125 ns(1)		115		135	ns
$t_{BIT(RXD)}$	Bit time on RXD output pins with $t_{BIT(TXD)}$ = 500 ns		470		520	ns
	Bit time on RXD output pins with $t_{BIT(TXD)}$ = 200 ns		170		220	ns
	Bit time on RXD output pins with $t_{BIT(TXD)}$ = 125 ns(1)		95		145	ns
Δt_{REC}	Receiver timing symmetry with $t_{BIT(TXD)}$ = 500 ns	See Figure 9-4 , R_L = 60 Ω, C_L = 100 pF, $C_{L(RXD)}$ = 15 pF Δt_{REC} = $t_{BIT(RXD)}$ - $t_{BIT(BUS)}$	-20		15	ns
	Receiver timing symmetry with $t_{BIT(TXD)}$ = 200 ns		-20		15	ns
	Receiver timing symmetry with $t_{BIT(TXD)}$ = 125 ns(1)		-20		15	ns

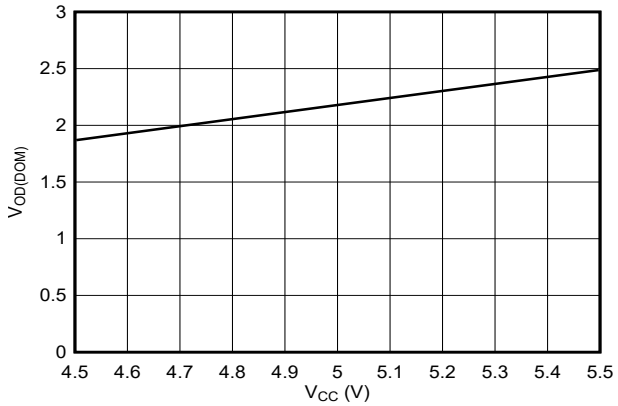
(1) Measured during characterization and not an ISO 11898-2:2016 parameter

8.10 Typical Characteristics



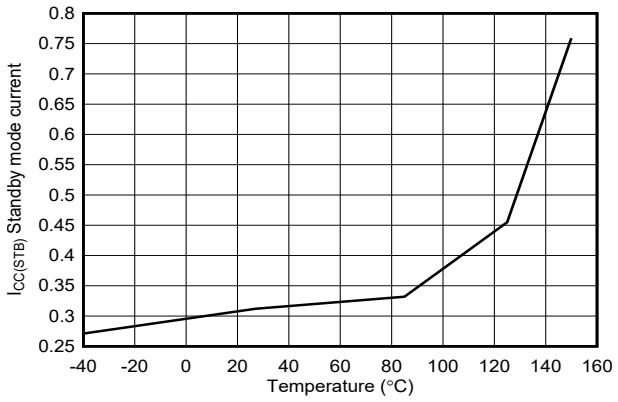
V_{CC} = 5 V V_{IO} = 3.3 V R_L = 60 Ω
C_L = Open STB = Low

Figure 8-1. $V_{OD(DOM)}$ Overtemperature



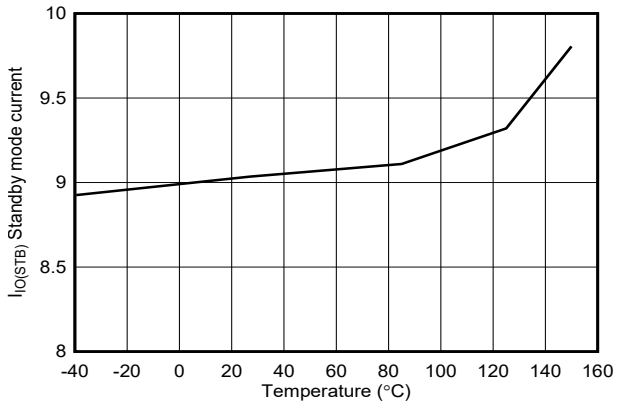
T_A = 25°C R_L = 60 Ω STB = Low
C_L = Open

Figure 8-2. $V_{OD(DOM)}$ over V_{CC}



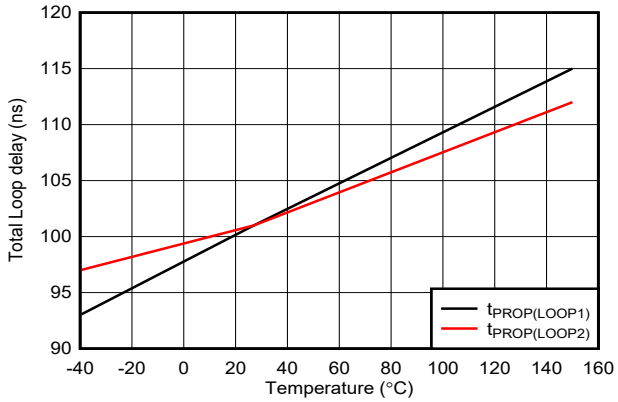
V_{CC} = 5 V V_{IO} = 3.3 V R_L = 50 Ω
STB = High

Figure 8-3. $I_{CC(standby)}$ vs Temperature



V_{CC} = 5 V V_{IO} = 3.3 V STB = High

Figure 8-4. $I_{IO(standby)}$ vs Temperature



V_{CC} = 5 V V_{IO} = 3.3 V R_L = 60 Ω
C_L = 100 pF C_{L_RXD} = 15 pF STB = Low

Figure 8-5. Total loop delay $t_{PROP(LOOP1)}$ and $t_{PROP(LOOP2)}$ vs Temperature

9 Parameter Measurement Information

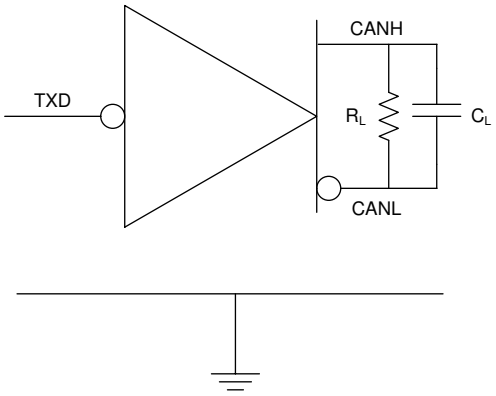


Figure 9-1. I_{CC} Test Circuit

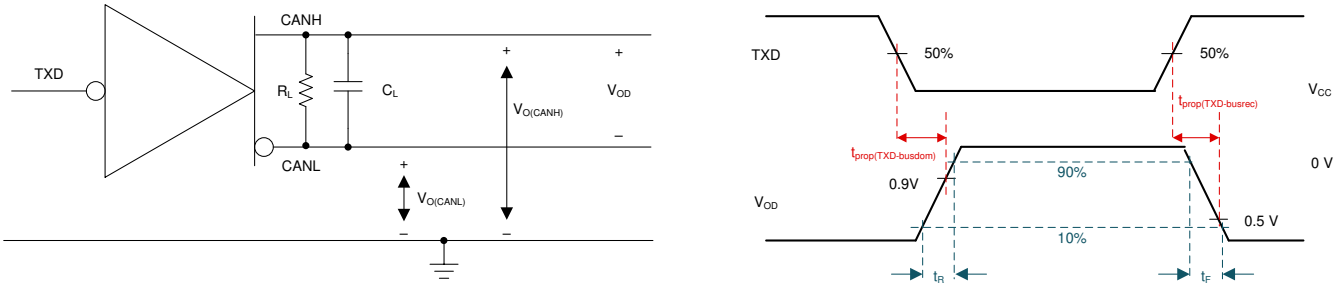


Figure 9-2. Driver Test Circuit and Measurement

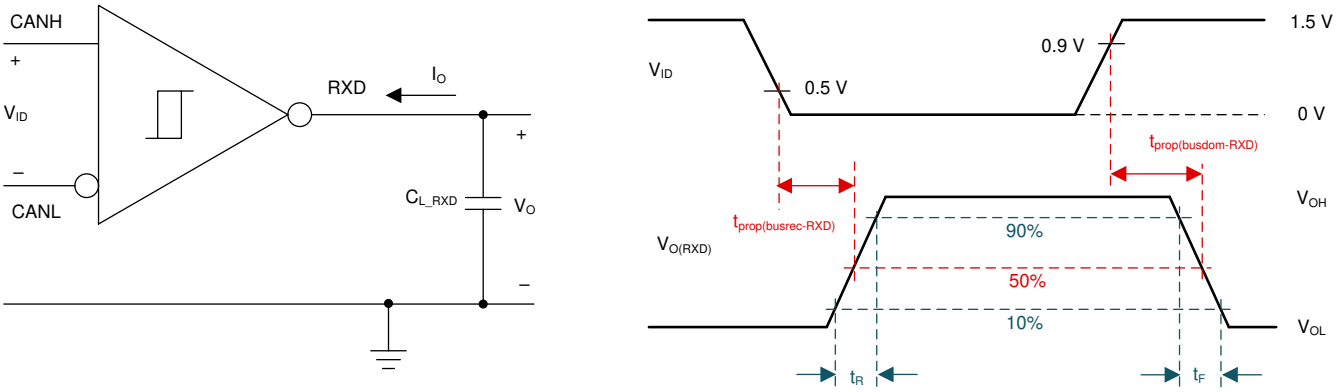
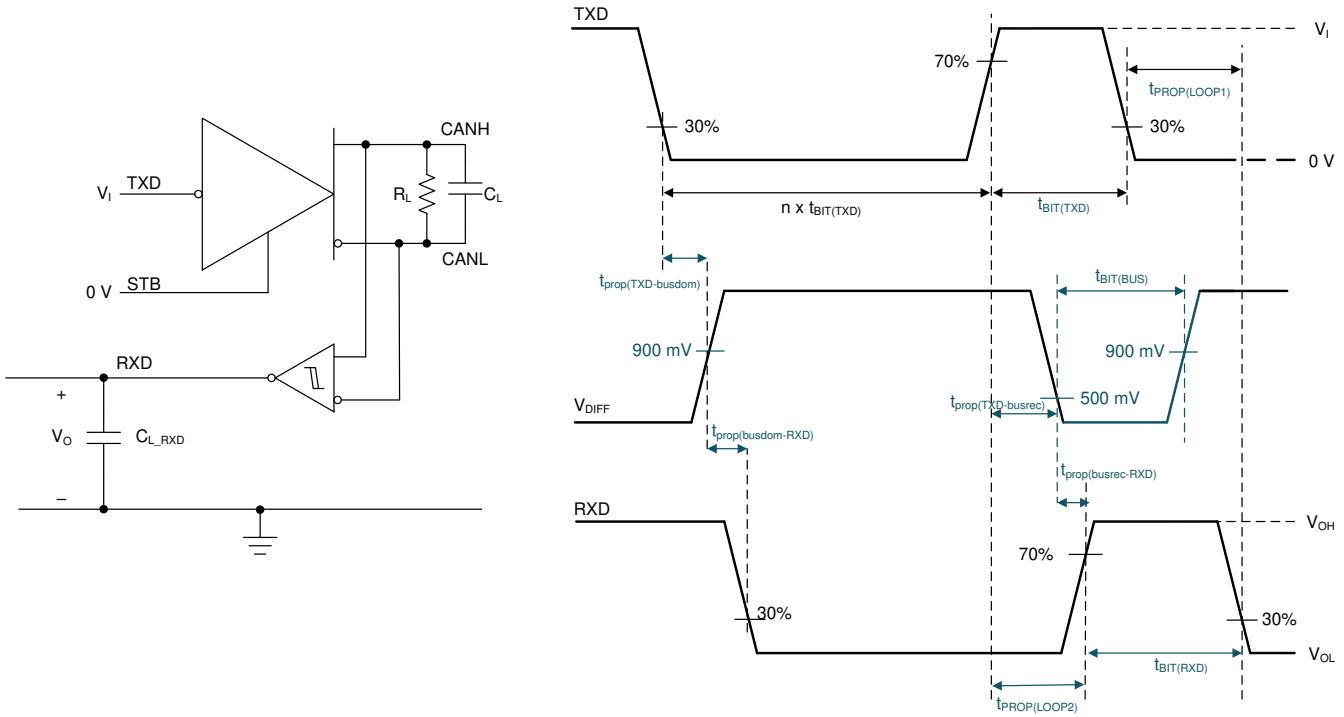


Figure 9-3. Receiver Test Circuit and Measurement



n = 1 to 5;
TXD rise/fall time < 10 ns

Figure 9-4. Transmitter and Receiver Timing Behavior Test Circuit and Measurement

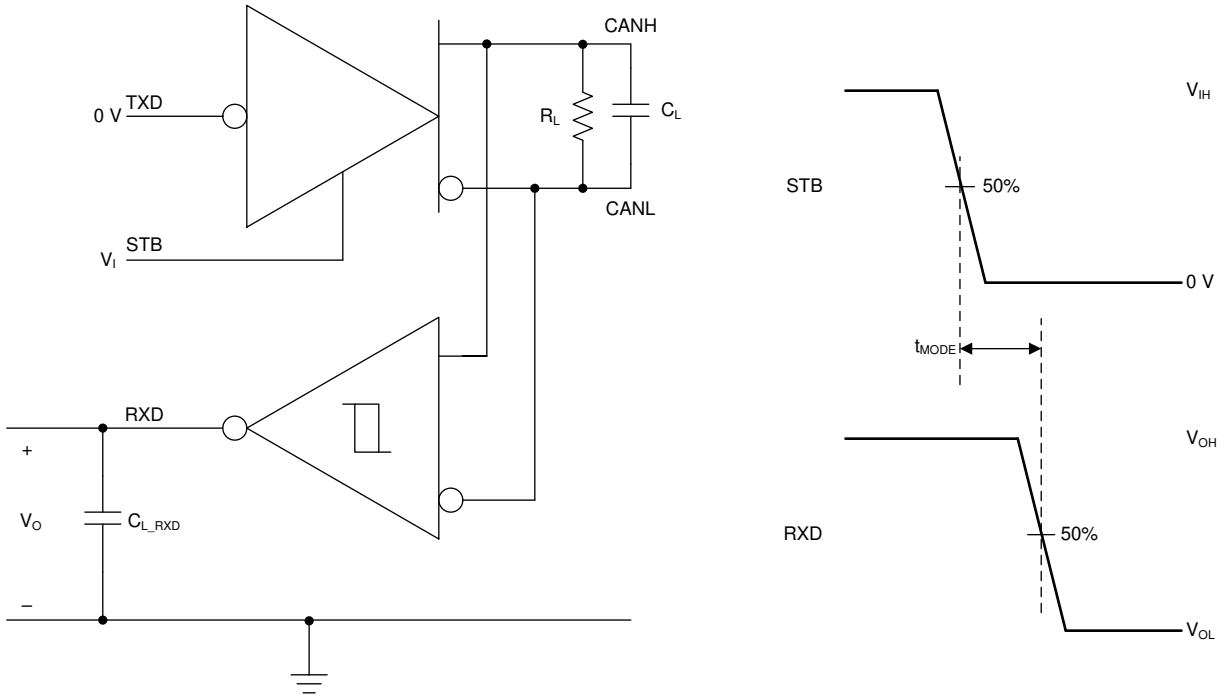


Figure 9-5. t_{MODE} Test Circuit and Measurement

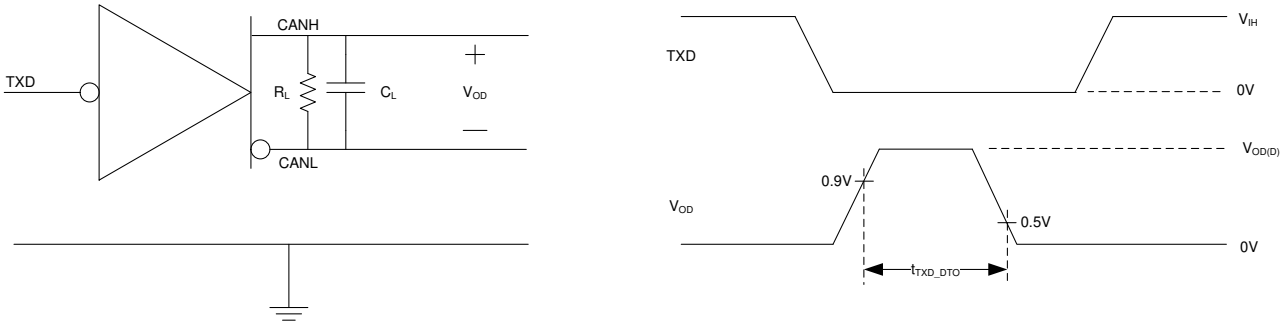


Figure 9-6. TXD Dominant Timeout Test Circuit and Measurement

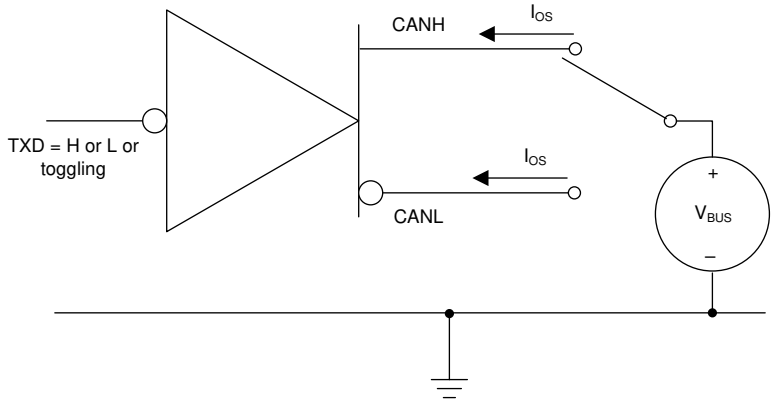


Figure 9-7. Driver Short-Circuit Current Test and Measurement

10 Detailed Description

10.1 Overview

The TCAN1462(V)-Q1 devices meet or exceed the specifications of the ISO 11898-2:2016 high speed CAN (Controller Area Network) physical layer standard and CiA 601-4 Signal Improvement capability (SIC) specification. The devices are data rate agnostic making them backward compatible for supporting classical CAN applications while also supporting CAN FD networks up to 8 Mbps. These devices have standby mode support which puts the transceiver in ultra-low current consumption mode. Upon receiving a valid wake-up pattern (WUP) on the CAN bus, the device signals to the microcontroller through the RXD pin. The MCU can then put the device into normal mode using the STB pin.

The TCAN1462V-Q1 has two separate supply rails, V_{CC} bus-side supply and V_{IO} logic supply for logic-level translation for interfacing directly to 1.8 V, 2.5 V, 3.3 V, or 5 V controllers.

10.1.1 Signal Improvement

Signal improvement is an additional capability added to CAN FD transceiver that enhances the maximum data rate achievable in complex star topologies by minimizing signal ringing. Signal ringing is the result of reflections caused by impedance mismatch at various points in a CAN network due to the nodes that act as stubs.

An example of a complex network is shown in Figure 10-1.

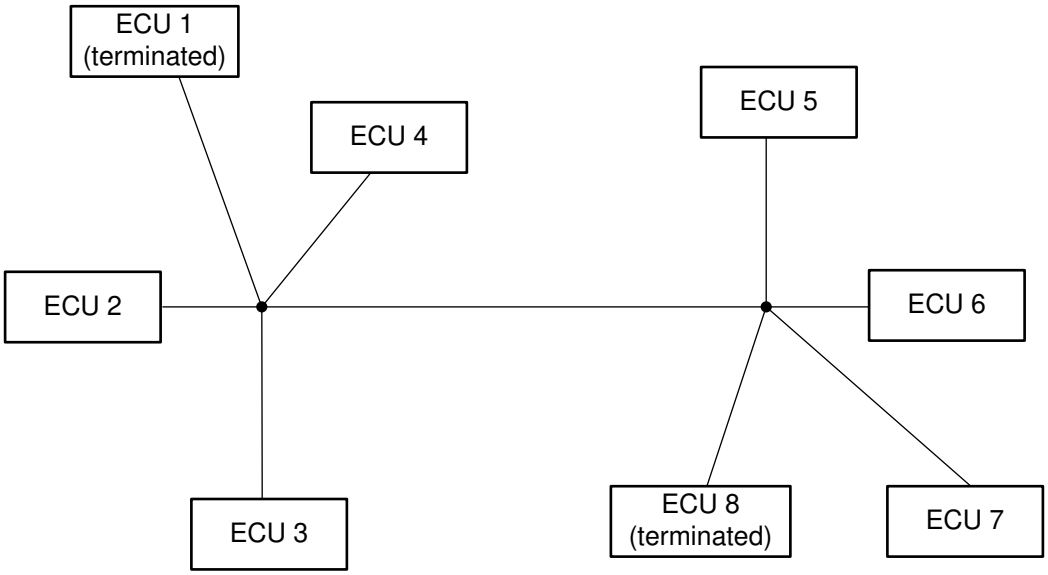


Figure 10-1. CAN Network: Star topology

Recessive-to-dominant signal edge is usually clean as it is strongly driven by the transmitter. Transmitter output impedance of CAN transceiver is ~50 Ω and matches to the network characteristic impedance. For a regular CAN FD transceiver, dominant-to-recessive edge is when the driver output impedance goes to ~60 kΩ and signal reflected back experiences impedance mismatch which causes ringing. TCAN1462-Q1 resolves this issue by TX-based Signal improvement capability (SIC). The device continues to drive the bus recessive until $t_{SIC\_TX\_base}$ so that reflections die down and recessive bit is clean at sampling point. In the active recessive phase, transmitter output impedance is low (~100 Ω). After this phase is over and device goes to passive recessive phase, driver output impedance goes to high-Z. This phenomenon is explained with Figure 10-2.

For more information on TI's signal improvement technology, and how it compares with similar devices in market, please refer to the white paper How Signal Improvement Capability Unlocks the Real Potential of CAN-FD Transceivers.

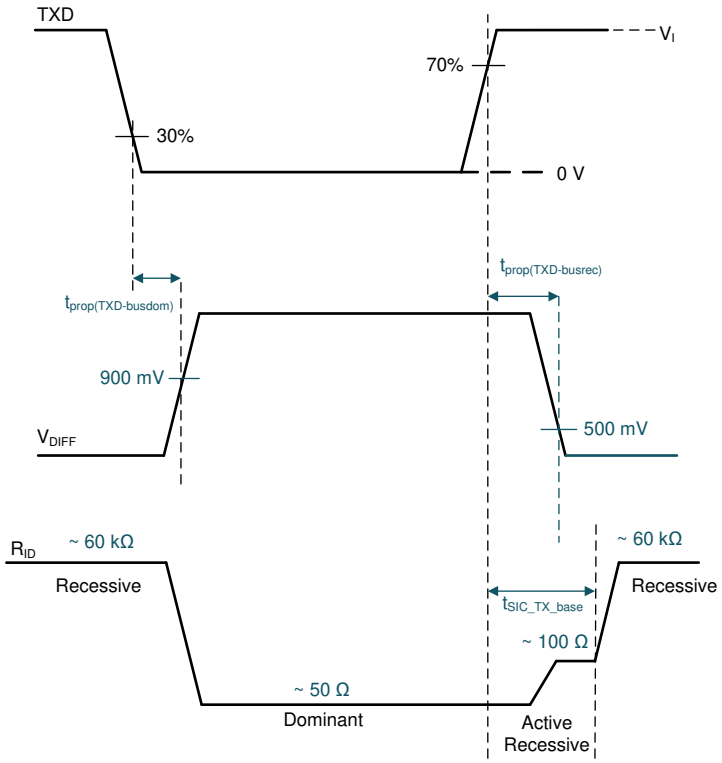


Figure 10-2. TX based SIC

10.2 Functional Block Diagram

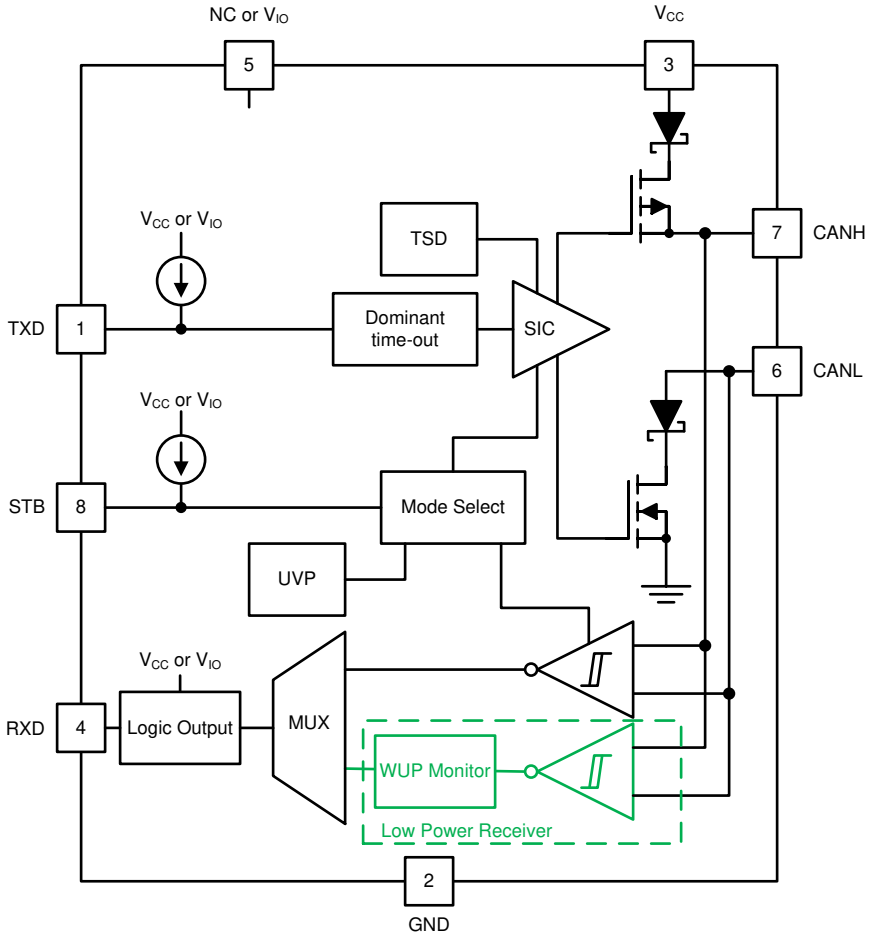


Figure 10-3. Block Diagram

10.3 Feature Description

10.3.1 Pin Description

10.3.1.1 TXD

The TXD input is a logic-level signal from a CAN controller to the transceiver. It is referenced to V_{CC} for TCAN1462-Q1 or to V_{IO} for TCAN1462V-Q1 devices.

10.3.1.2 GND

GND is the ground pin of the transceiver, it must be connected to the PCB ground.

10.3.1.3 V_{CC}

V_{CC} provides the 5-V power supply to the CAN transceiver.

10.3.1.4 RXD

The RXD output is a logic-level signal from the CAN transceiver to the CAN controller. It is referenced to V_{CC} for TCAN1462-Q1 and V_{IO} for TCAN1462V-Q1 devices. For TCAN1462V-Q1, RXD is only driven once V_{IO} is present.

When a wake event takes place, RXD is driven low.

10.3.1.5 V_{IO} (only for TCAN1462V-Q1)

The V_{IO} pin provides the digital I/O voltage to match the CAN controller voltage thus avoiding the requirement for a level shifter. It supports wide range of controller interface voltage levels from 1.7 V to 5.5 V.

10.3.1.6 CANH and CANL

These are the CAN high and CAN low differential bus pins. These pins are connected to the CAN transceiver and the low-voltage WUP CAN receiver.

10.3.1.7 STB (Standby)

The STB pin is an input pin used for mode control of the transceiver. The STB pin can be supplied from either the system processor or from a static system voltage source. If normal mode is the only intended mode of operation, then the STB pin can be tied directly to GND.

10.3.2 CAN Bus States

The CAN bus has two logical states during operation: recessive and dominant. See Figure 10-4 and Figure 10-5.

A dominant bus state occurs when the bus is driven differentially and corresponds to a logic low on the TXD and RXD pins. A recessive bus state occurs when the bus is biased to $V_{CC}/2$ via the high-resistance internal input resistors R_{IN}) of the receiver and corresponds to a logic high on the TXD and RXD pins.

A dominant state overwrites the recessive state during arbitration. Multiple CAN nodes may be transmitting a dominant bit at the same time during arbitration, and in this case the differential voltage of the bus is greater than the differential voltage of a single driver.

The TCAN1462-Q1 transceiver implements a low-power standby (STB) mode which enables a third bus state where the bus pins are weakly biased to ground via the high resistance internal resistors of the receiver. See Figure 10-4 and Figure 10-5.

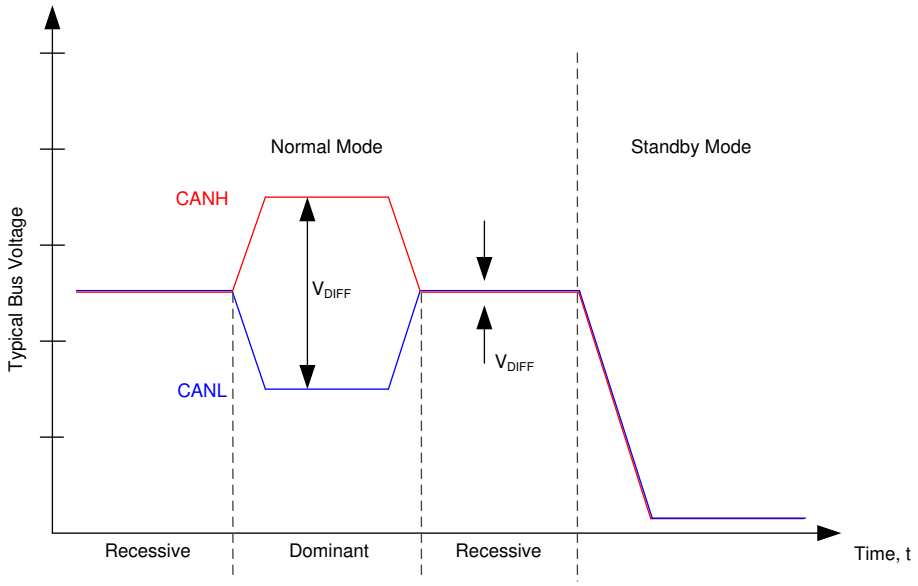
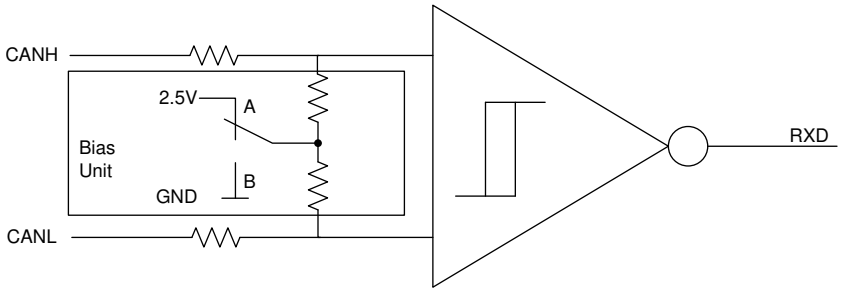


Figure 10-4. Bus States



A. Normal Mode
B. Standby Mode

Figure 10-5. Simplified Recessive Common Mode Bias Unit and Receiver

10.3.3 TXD Dominant Timeout (DTO)

During normal mode, the only mode where the CAN driver is active, the TXD DTO circuit prevents the local node from blocking network communication in the event of a hardware or software failure where TXD is held dominant longer than the timeout period t_{TXD_DTO}. The TXD DTO circuit is triggered by a falling edge on TXD. If no rising edge is seen before the timeout period of the circuit, t_{TXD_DTO}, the CAN driver is disabled. This frees the bus for communication between other nodes on the network. The CAN driver is reactivated when a recessive signal is seen on the TXD pin, thus clearing the dominant time out. The receiver remains active and biased to $V_{CC}/2$ and the RXD output reflects the activity on the CAN bus during the TXD DTO fault.

The minimum dominant TXD time allowed by the TXD DTO circuit limits the minimum possible transmitted data rate of the device. The CAN protocol allows a maximum of eleven successive dominant bits (on TXD) for the worst case, where five successive dominant bits are followed immediately by an error frame. The minimum transmitted data rate may be calculated using Equation 1.

$$\text{Minimum Data Rate} = 11 \text{ bits} / t_{TXD\_DTO} = 11 \text{ bits} / 1.2 \text{ ms} = 9.2 \text{ kbps} \quad (1)$$

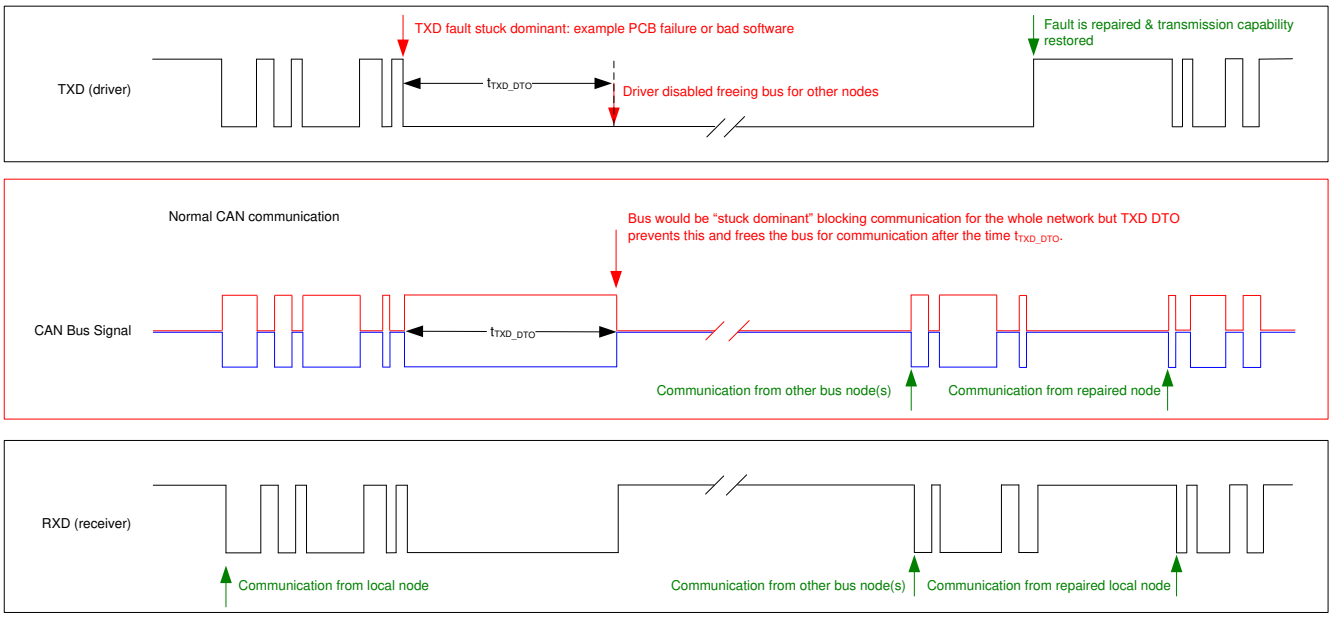


Figure 10-6. Example Timing Diagram for TXD Dominant Timeout

10.3.4 CAN Bus Short-circuit Current Limiting

The TCAN1462-Q1 has several protection features that limit the short-circuit current when a CAN bus line is shorted. These include CAN driver current limiting in the dominant and recessive states and TXD dominant state timeout which prevents permanently having the higher short-circuit current of a dominant state in case of a system fault. During CAN communication the bus switches between the dominant and recessive states; thus, the short-circuit current may be viewed as either the current during each bus state or as a DC average current. When selecting termination resistors or a common mode choke for the CAN design the average power rating, $I_{OS(AVG)}$, should be used. The percentage dominant is limited by the TXD DTO and the CAN protocol which has forced state changes and recessive bits due to bit stuffing, control fields, and inter frame space. These make sure there is a minimum amount of recessive time on the bus even if the data field contains a high percentage of dominant bits.

The average short-circuit current of the bus depends on the ratio of recessive to dominant bits and their respective short-circuit currents. The average short-circuit current may be calculated using Equation 2.

$$I_{OS(AVG)} = \%\ \text{Transmit} \times [(\%\ \text{REC\_Bits} \times I_{OS(SS)\_REC}) + (\%\ \text{DOM\_Bits} \times I_{OS(SS)\_DOM})] + [\%\ \text{Receive} \times I_{OS(SS)\_REC}] \quad (2)$$

Where:

- $I_{OS(AVG)}$ is the average short-circuit current
- % Transmit is the percentage the node is transmitting CAN messages
- % Receive is the percentage the node is receiving CAN messages
- % REC_Bits is the percentage of recessive bits in the transmitted CAN messages
- % DOM_Bits is the percentage of dominant bits in the transmitted CAN messages
- $I_{OS(SS)\_REC}$ is the recessive steady state short-circuit current
- $I_{OS(SS)\_DOM}$ is the dominant steady state short-circuit current

This short-circuit current and the possible fault cases of the network should be taken into consideration when sizing the power supply used to generate the transceivers V_{CC} supply.

10.3.5 Thermal Shutdown (TSD)

If the junction temperature of the TCAN1462-Q1 exceeds the thermal shutdown threshold, T_{TSD}, the device turns off the CAN driver circuitry and blocks the TXD to bus transmission path. The shutdown condition is cleared when the junction temperature of the device drops below T_{TSD}. The CAN bus pins are biased to $V_{CC}/2$ during a TSD fault and the receiver to RXD path remains operational. The TCAN1462-Q1 TSD circuit includes hysteresis which prevents the CAN driver output from oscillating during a TSD fault.

10.3.6 Undervoltage Lockout

The supply pins, V_{CC} and V_{IO}, have undervoltage detection that places the device into a protected state. This protects the bus during an undervoltage event on either supply pin.

Table 10-1. Undervoltage Lockout - TCAN1462-Q1

V_{CC}	DEVICE STATE	BUS	RXD PIN
> UV_{VCC}	Normal	Per TXD	Mirrors bus
< UV_{VCC}	Protected	High impedance	High impedance

Table 10-2. Undervoltage Lockout - TCAN1462V-Q1

V_{CC}	V_{IO}	DEVICE STATE	BUS	RXD PIN
> UV_{VCC}	> UV_{VIO}	Normal	Per TXD	Mirrors bus
< UV_{VCC}	> UV_{VIO}	STB = V_{IO}: standby mode	High impedance	V_{IO}: Remote wake request(1)
		STB = GND: Protected		Recessive
> UV_{VCC}	< UV_{VIO}	Protected		High impedance
< UV_{VCC}	< UV_{VIO}	Protected		High impedance

(1) See Remote Wake Request via Wake-Up Pattern (WUP) in Standby Mode

Once the undervoltage condition is cleared and t_{MODE} has expired, the TCAN1462-Q1 transitions to normal mode and the host controller can send and receive CAN traffic again.

10.3.7 Unpowered Device

The TCAN1462-Q1 is designed to be an ideal passive or no load to the CAN bus if the device is unpowered. The bus pins were designed to have low leakage currents when the device is unpowered, so they do not load the bus. This is critical if some nodes of the network are unpowered while the rest of the of network remains operational.

The logic pins also have low leakage currents when the device is unpowered, so they do not load other circuits which may remain powered.

10.3.8 Floating pins

The TCAN1462-Q1 has internal pull-ups on critical pins which place the device into known states if the pin floats. This internal bias should not be relied upon by design though, especially in noisy environments, but instead should be considered a failsafe protection feature.

When a CAN controller supporting open-drain outputs is used, an adequate external pull-up resistor must be chosen. This make sures the TXD output of the CAN controller maintains acceptable bit time to the input of the CAN transceiver. See Table 10-3 for details on pin bias conditions.

Table 10-3. Pin Bias

Pin	Pull-up or Pull-down	Comment
TXD	Pull-up	Weakly biases TXD towards recessive to prevent bus blockage or TXD DTO triggering
STB	Pull-up	Weakly biases STB towards low-power standby mode to prevent excessive system power

10.4 Device Functional Modes

10.4.1 Operating Modes

The TCAN1462-Q1 has two main operating modes; normal mode and standby mode. Operating mode selection is made by applying a high or low level to the STB pin on the TCAN1462-Q1.

Table 10-4. Operating Modes

STB	Device Mode	Driver	Receiver	RXD Pin
High	Low current standby mode with bus wake-up	Disabled	Low-power receiver and bus monitor enable	High (recessive) until valid WUP is received See (1)
Low	Normal Mode	Enabled	Enabled	Mirrors bus state

(1) See Remote Wake Request via Wake-Up Pattern (WUP) in Standby Mode

10.4.2 Normal Mode

This is the normal operating mode of the TCAN1462-Q1. The CAN driver and receiver are fully operational and CAN communication is bi-directional. The driver is translating a digital input on the TXD input to a differential output on the CANH and CANL bus pins. The receiver is translating the differential signal from CANH and CANL to a digital output on the RXD output.

10.4.3 Standby Mode

This is the low-power mode of the TCAN1462-Q1. The CAN driver and main receiver are switched off and bi-directional CAN communication is not possible. The low-power receiver and bus monitor circuits are enabled to allow for RXD wake-up requests via the CAN bus. A wake-up request is output to RXD as shown in Figure 10-7. The local CAN protocol controller should monitor RXD for transitions (high-to-low) and reactivate the device to normal mode by pulling the STB pin low. The CAN bus pins are weakly pulled to GND in this mode; see Figure 10-4 and Figure 10-5.

In standby mode, only the V_{IO} supply is required therefore the V_{CC} may be switched off for additional system level current savings.

10.4.3.1 Remote Wake Request via Wake-Up Pattern (WUP) in Standby Mode

The TCAN1462-Q1 supports a remote wake-up request that is used to indicate to the host controller that the bus is active and the node should return to normal operation.

The device uses the multiple filtered dominant wake-up pattern (WUP) from the ISO 11898-2:2016 standard to qualify bus activity. Once a valid WUP has been received, the wake request is indicated to the controller by a falling edge and low period corresponding to a filtered dominant on the RXD output of the TCAN1462-Q1.

The WUP consists of a filtered dominant pulse, followed by a filtered recessive pulse, and finally by a second filtered dominant pulse. The first filtered dominant initiates the WUP, and the bus monitor then waits on a filtered recessive; other bus traffic does not reset the bus monitor. Once a filtered recessive is received the bus monitor is waiting for a filtered dominant and again, other bus traffic does not reset the bus monitor. Immediately upon reception of the second filtered dominant the bus monitor recognizes the WUP and drives the RXD output low every time an additional filtered dominant signal is received from the bus.

For a dominant or recessive to be considered filtered, the bus must be in that state for more than the t_{WK_FILTER} time. Due to variability in t_{WK_FILTER} the following scenarios are applicable. Bus state times less than $t_{WK\_FILTER(MIN)}$ are never detected as part of a WUP and thus no wake request is generated. Bus state times between $t_{WK\_FILTER(MIN)}$ and $t_{WK\_FILTER(MAX)}$ may be detected as part of a WUP and a wake-up request may be generated. Bus state times greater than $t_{WK\_FILTER(MAX)}$ are always detected as part of a WUP, and thus a wake request is always generated. See Figure 10-7 for the timing diagram of the wake-up pattern.

The pattern and t_{WK_FILTER} time used for the WUP prevents noise and bus stuck dominant faults from causing false wake-up requests while allowing any valid message to initiate a wake-up request.

The ISO 11898-2:2016 standard has defined times for a short and long wake-up filter time. The t_{WK_FILTER} timing for the device has been picked to be within the minimum and maximum values of both filter ranges. This timing

has been chosen such that a single bit time at 500 kbps, or two back-to-back bit times at 1 Mbps triggers the filter in either bus state. Any CAN frame at 500 kbps or less would contain a valid WUP.

For an additional layer of robustness and to prevent false wake-ups, the device implements a wake-up timeout feature. For a remote wake-up event to successfully occur, the entire WUP must be received within the timeout value $t \leq t_{WK\_TIMEOUT}$. If not, the internal logic is reset and the transceiver remains in its current state without waking up. The full pattern must then be transmitted again, conforming to the constraints mentioned in this section. See Figure 10-7 for the timing diagram of the wake-up pattern with wake timeout feature.

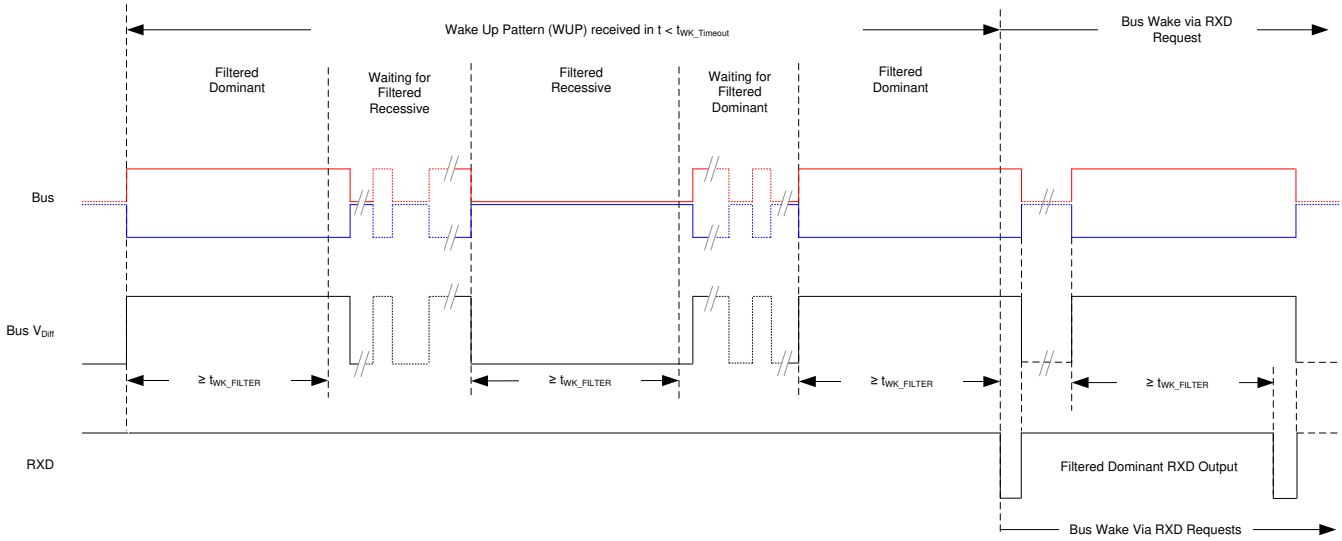


Figure 10-7. Wake-Up Pattern (WUP) with $t_{WK\_TIMEOUT}$

10.4.4 Driver and Receiver Function

The digital logic input and output levels for the TCAN1462-Q1 are CMOS levels with respect to V_{CC}. For TCAN1462V-Q1, these are referred to V_{IO} for compatibility with MCUs having 1.8 V, 2.5 V, 3.3 V, or 5 V supply.

Table 10-5. Driver Function Table

Device Mode	TXD Input(1)	Bus Outputs		Driven Bus State(2)
		CANH	CANL	
Normal	Low	High	Low	Dominant
	High or open	High impedance	High impedance	Biased recessive
Standby	X	High impedance	High impedance	Biased to ground

(1) X = irrelevant
(2) For bus state and bias see Figure 10-4 and Figure 10-5

Table 10-6. Receiver Function Table Normal and Standby Mode

Device Mode	CAN Differential Inputs $V_{ID} = V_{CANH} - V_{CANL}$	Bus State	RXD Pin
Normal	$V_{ID} \geq 0.9$ V	Dominant	Low
	0.5 V < V_{ID} < 0.9 V	Undefined	Undefined
	$V_{ID} \leq 0.5$ V	Recessive	High
Standby	$V_{ID} \geq 1.15$ V	Dominant	High Low if a remote wake event occurred See Figure 10-7
	0.4 V < V_{ID} < 1.15 V	Undefined	
	$V_{ID} \leq 0.4$ V	Recessive	
Any	Open ($V_{ID} \approx 0$ V)	Open	High

11 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

11.1 Application Information

11.2 Typical Application

The TCAN1462-Q1 transceiver can be used in applications with a host controller or FPGA that includes the link layer portion of the CAN protocol. Figure 11-1 shows a typical configuration for 5 V controller applications. The bus termination is shown for illustrative purposes.

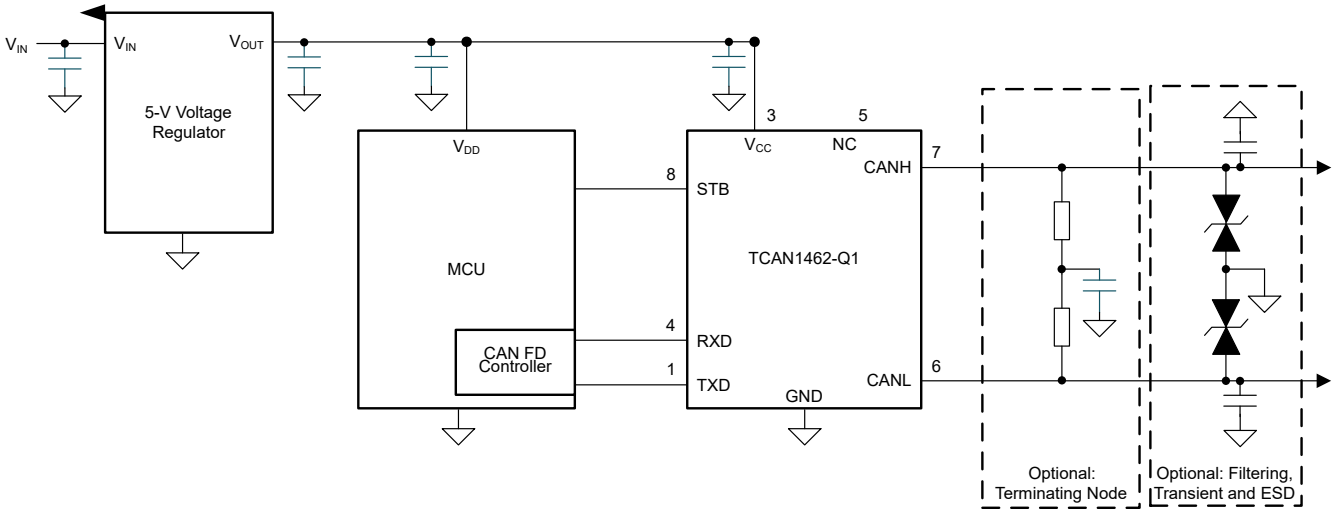


Figure 11-1. Transceiver Application Using 5 V I/O Connections

11.2.1 Design Requirements

11.2.1.1 CAN Termination

Termination may be a single 120-Ω resistor at each end of the bus, either on the cable or in a terminating node. If filtering and stabilization of the common-mode voltage of the bus is desired then split termination may be used, see Figure 11-2. Split termination improves the electromagnetic emissions behavior of the network by filtering higher-frequency common-mode noise that may be present on the differential signal lines.

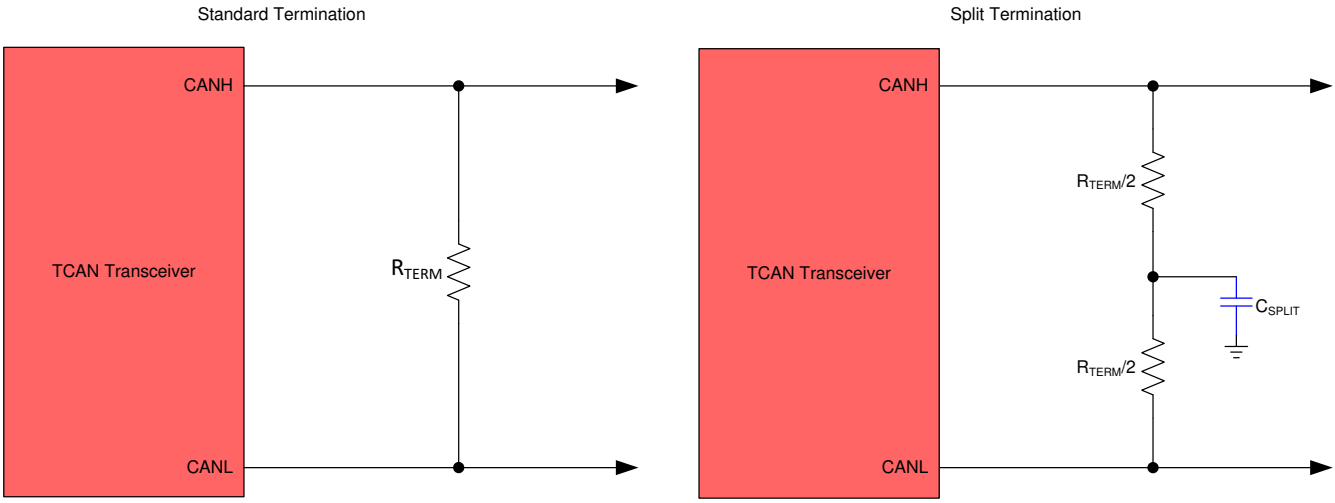


Figure 11-2. CAN Bus Termination Concepts

11.2.2 Detailed Design Procedures

11.2.2.1 Bus Loading, Length and Number of Nodes

A typical CAN application may have a maximum bus length of 40 meters and maximum stub length of 0.3 m. However, with careful design, users can have longer cables, longer stub lengths, and many more nodes to a bus. A high number of nodes requires a transceiver with high input impedance such as the TCAN1462-Q1. Additionally, since TCAN1462(V)-Q1 has SIC, in a given network size, higher data rate can be achieved because signal ringing is attenuated.

Many CAN organizations and standards have scaled the use of CAN for applications outside the original ISO 11898-2 standard. They made system level trade off decisions for data rate, cable length, and parasitic loading of the bus. Examples of these CAN systems level specifications are ARINC 825, CANopen, DeviceNet, SAE J2284, SAE J1939, and NMEA 2000.

A CAN network system design is a series of tradeoffs. In the ISO 11898-2:2016 specification, the driver differential output is specified with a bus load that can range from 50 Ω to 65 Ω where the differential output must be greater than 1.5 V. The TCAN1462-Q1 family is specified to meet the 1.5-V requirement down to 50 Ω and is specified to meet 1.4-V differential output at 45Ω bus load. The differential input resistance of the TCAN1462-Q1 is a minimum of 40 kΩ. If 100 TCAN1462-Q1 transceivers are in parallel on a bus, this is equivalent to a 400-Ω differential load in parallel with the nominal 60 Ω bus termination which gives a total bus load of approximately 52 Ω. Therefore, the TCAN1462-Q1 family theoretically supports over 100 transceivers on a single bus segment. However, for a CAN network design margin must be given for signal loss across the system and cabling, parasitic loadings, timing, network imbalances, ground offsets and signal integrity thus a practical maximum number of nodes is often lower. Bus length may also be extended beyond 40 meters by careful system design and data rate tradeoffs. For example, CANopen network design guidelines allow the network to be up to 1 km with changes in the termination resistance, cabling, less than 64 nodes and significantly lowered data rate.

This flexibility in CAN network design is one of the key strengths of the various extensions and additional standards that have been built on the original ISO 11898-2 CAN standard. However, when using this flexibility the CAN network system, the designer must take the responsibility of good network design for a robust network operation.

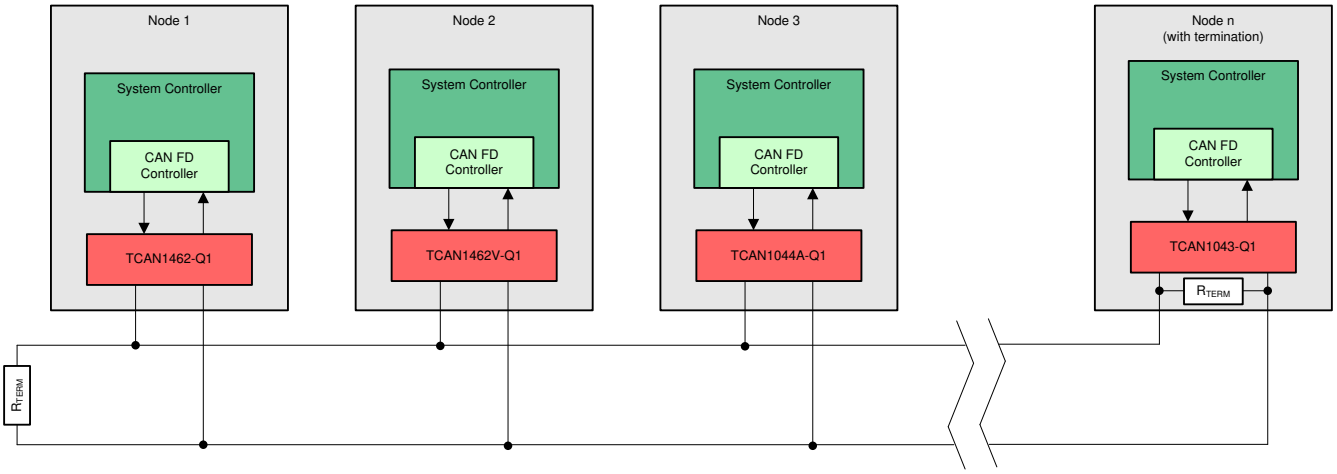
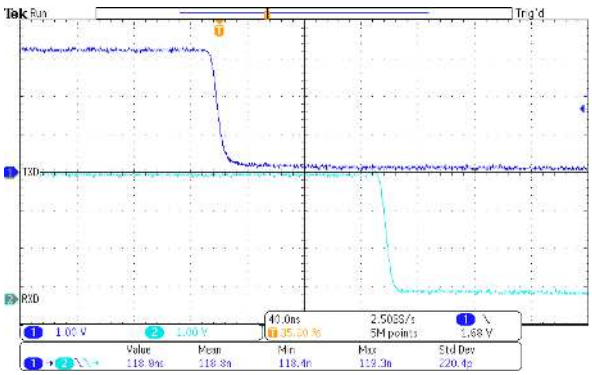


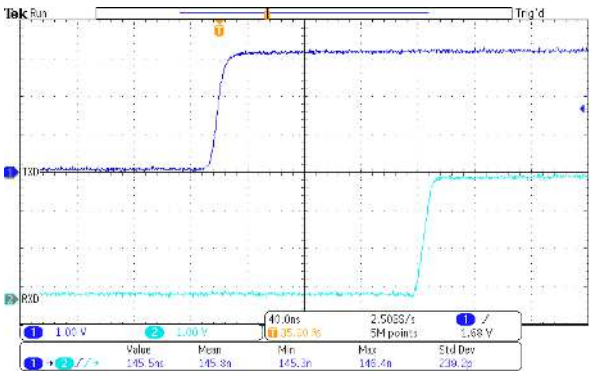
Figure 11-3. Typical CAN Bus

11.2.3 Application Curves



V_{CC} = 5 V V_{IO} = 3.3 V R_L = 60 Ω

Figure 11-4. $t_{PROP(LOOP1)}$



V_{CC} = 5 V V_{IO} = 3.3 V R_L = 60 Ω

Figure 11-5. $t_{PROP(LOOP2)}$

11.3 System Examples

The TCAN1462V-Q1 CAN transceiver is typically used in applications with a host controller or FPGA that includes the link layer portion of the CAN protocol. A 1.8 V, 2.5 V, or 3.3 V application is shown in Figure 11-6. The bus termination is shown for illustrative purposes.

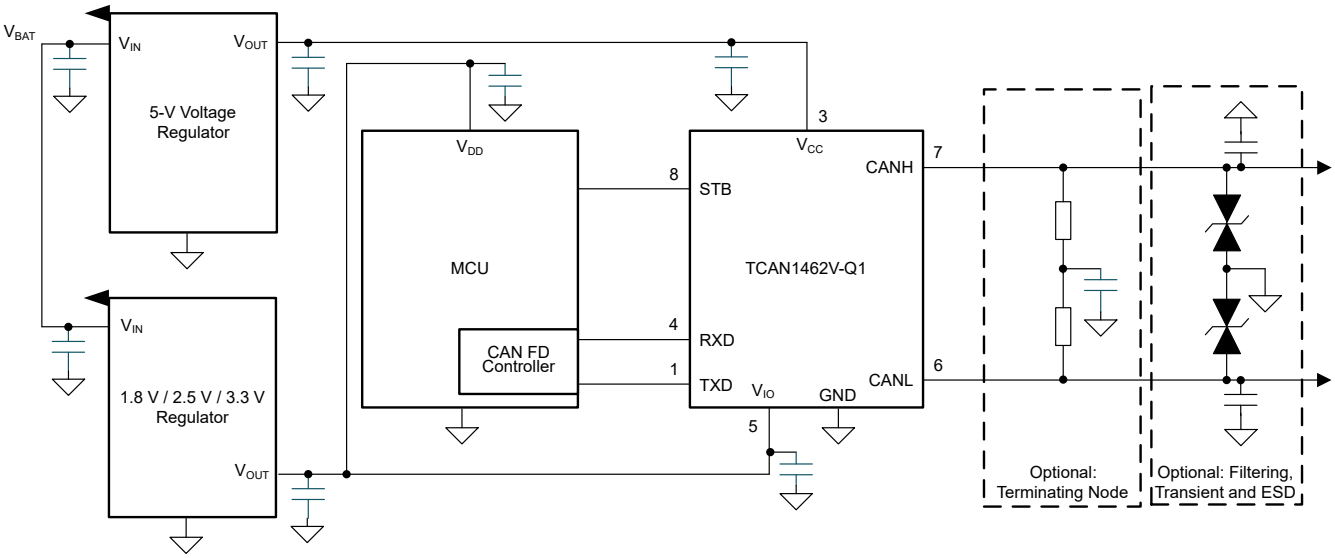


Figure 11-6. Typical Transceiver Application Using 1.8 V, 2.5 V, 3.3 V IO Connections

11.4 Power Supply Recommendations

The TCAN1462-Q1 transceiver is designed to operate with a main V_{CC} input voltage supply range between 4.5 V and 5.5 V. The TCAN1462V-Q1 implements an I/O level shifting supply input, V_{IO}, designed for a range between 1.8 V and 5.5 V. Both supply inputs must be well regulated. A decoupling capacitance, typically 100 nF, should be placed near the CAN transceiver main V_{CC} supply pin in addition to bypass capacitors. A decoupling capacitor, typically 100 nF, should be placed near the CAN transceiver V_{IO} supply pin in addition to bypass capacitors.

11.5 Layout

11.5.1 Layout Guidelines

- Place the protection and filtering circuitry close to the bus connector, J1, to prevent transients, ESD, and noise from propagating onto the board. This layout example shows an optional transient voltage suppression (TVS) diode, D1, which may be implemented if the system-level requirements exceed the specified rating of the transceiver. This example also shows optional bus filter capacitors C4 and C5.
- Design the bus protection components in the direction of the signal path. Do not force the transient current to divert from the signal path to reach the protection device.
- Decoupling capacitors should be placed as close as possible to the supply pins V_{CC} and V_{IO} of transceiver.
- Use at least two vias for supply and ground connections of bypass capacitors and protection devices to minimize trace and via inductance.

Note

High frequency current follows the path of least impedance and not the path of least resistance.

- This layout example shows how split termination could be implemented on the CAN node. The termination is split into two resistors, R4 and R5, with the center or split tap of the termination connected to ground via capacitor C3. Split termination provides common mode filtering for the bus. See CAN Termination, and CAN Bus Short Circuit Current Limiting for information on termination concepts and power ratings needed for the termination resistor(s).

11.5.2 Layout Example

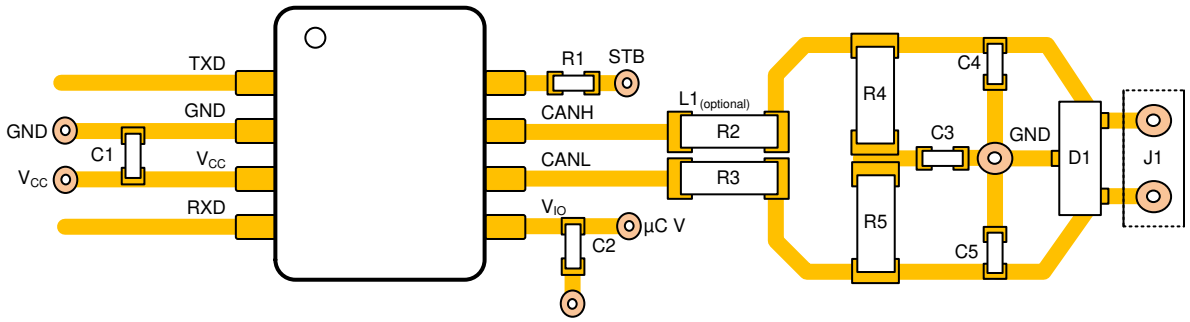


Figure 11-7. Layout Example

12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTCAN1462DDFRQ1	ACTIVE	SOT-23-THIN	DDF	8	3000	TBD	Call TI	Call TI	-40 to 125		Samples
PTCAN1462VDDFRQ1	ACTIVE	SOT-23-THIN	DDF	8	3000	TBD	Call TI	Call TI	-40 to 125		Samples
TCAN1462DRBRQ1	ACTIVE	SON	DRB	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1462	Samples
TCAN1462DRQ1	ACTIVE	SOIC	D	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1462	Samples
TCAN1462VDRBRQ1	ACTIVE	SON	DRB	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1462V	Samples
TCAN1462VDRQ1	ACTIVE	SOIC	D	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1462V	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

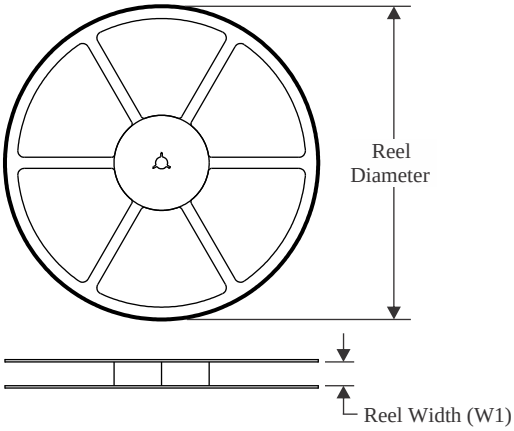
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

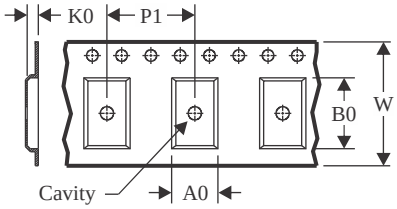
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

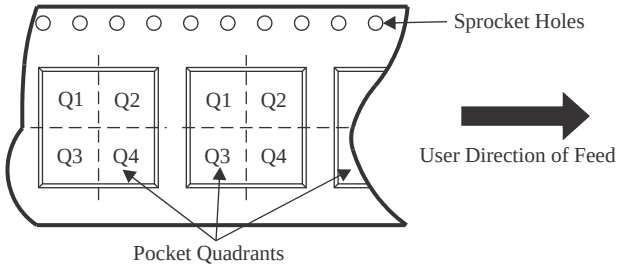


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

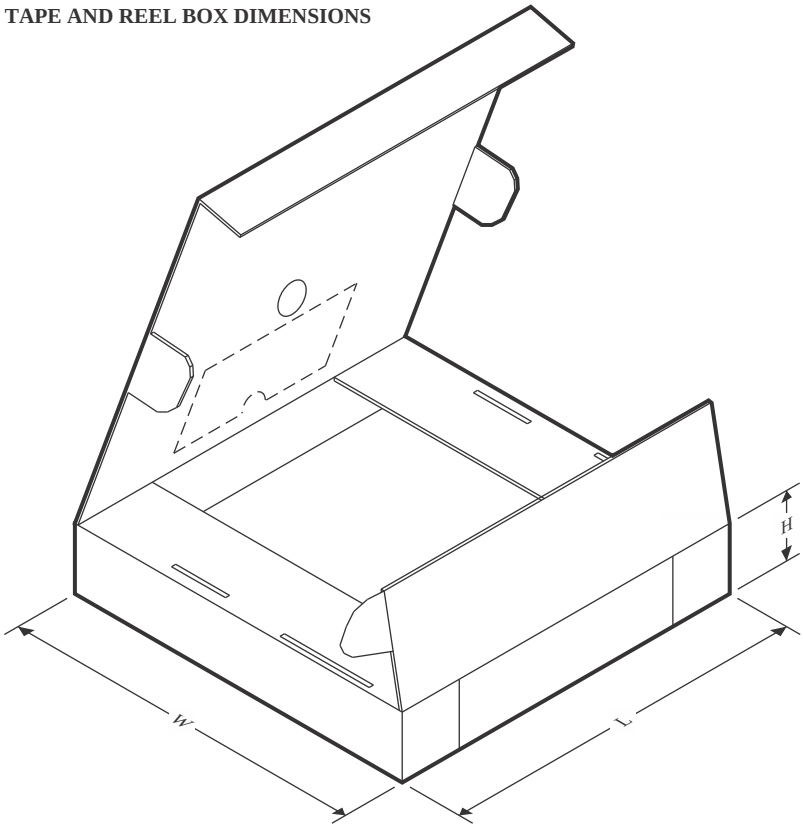
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

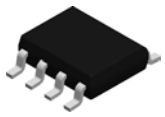
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TCAN1462DRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q1
TCAN1462DRQ1	SOIC	D	8	3000	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TCAN1462VDRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q1
TCAN1462VDRQ1	SOIC	D	8	3000	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TCAN1462DRBRQ1	SON	DRB	8	3000	367.0	367.0	35.0
TCAN1462DRQ1	SOIC	D	8	3000	356.0	356.0	35.0
TCAN1462VDRBRQ1	SON	DRB	8	3000	367.0	367.0	35.0
TCAN1462VDRQ1	SOIC	D	8	3000	356.0	356.0	35.0

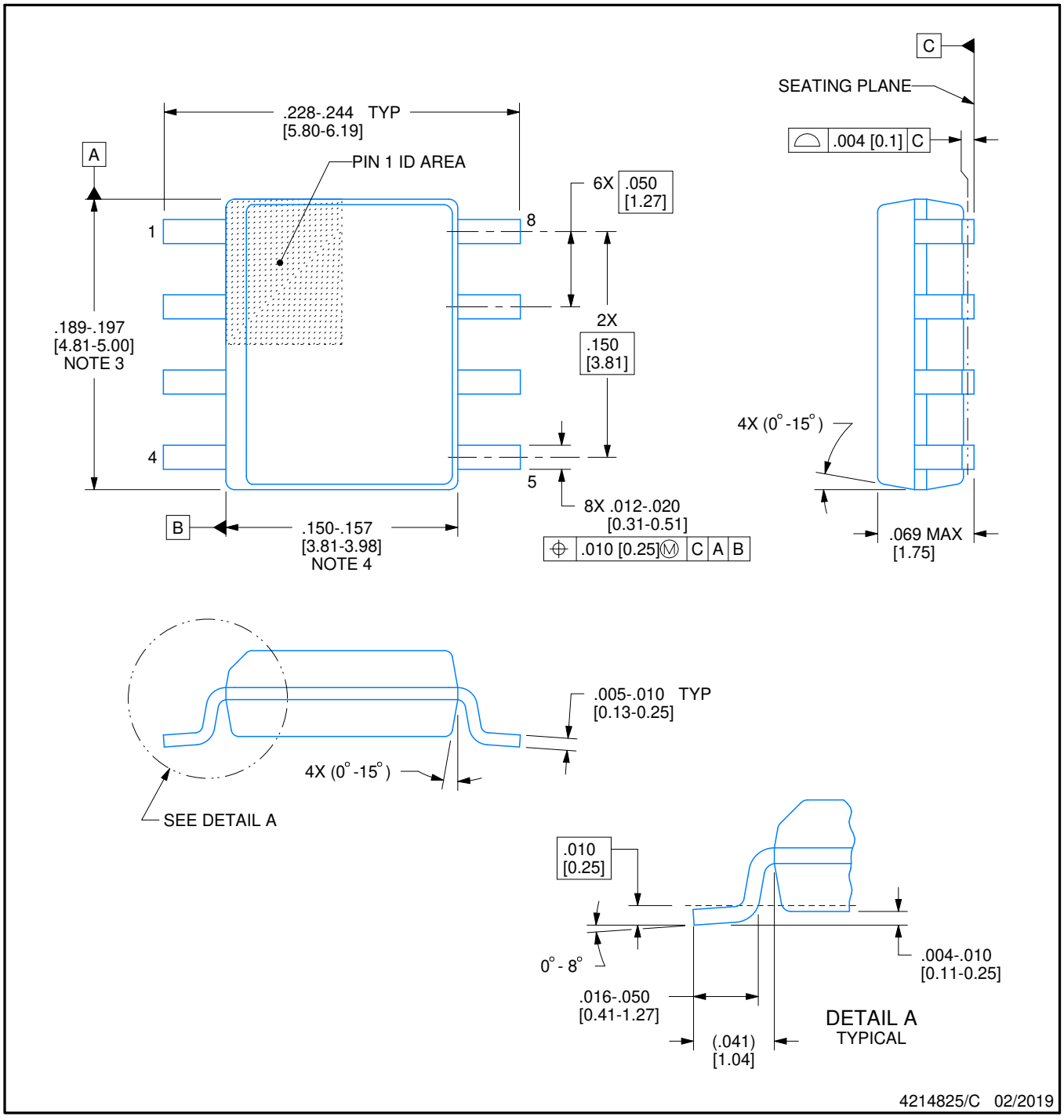


PACKAGE OUTLINE

D0008A

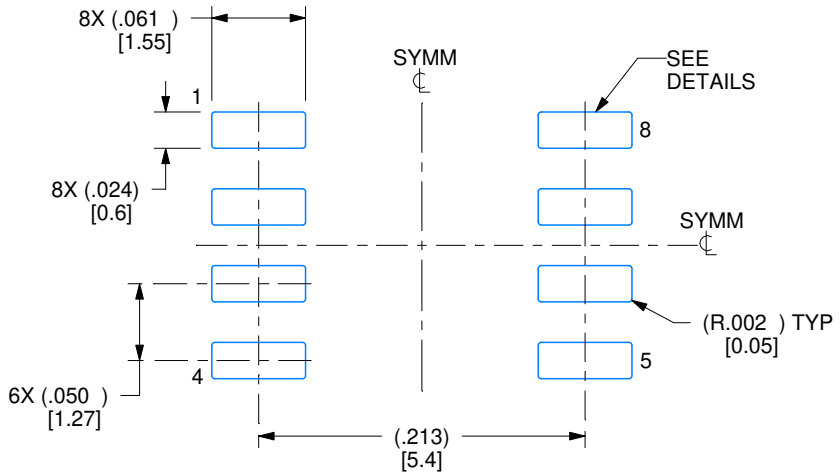
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

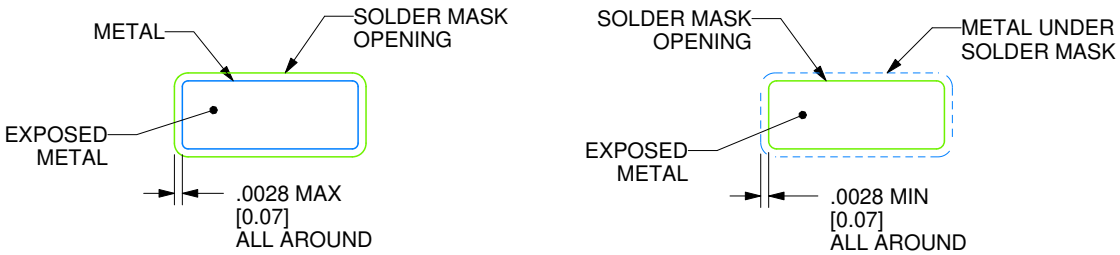


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

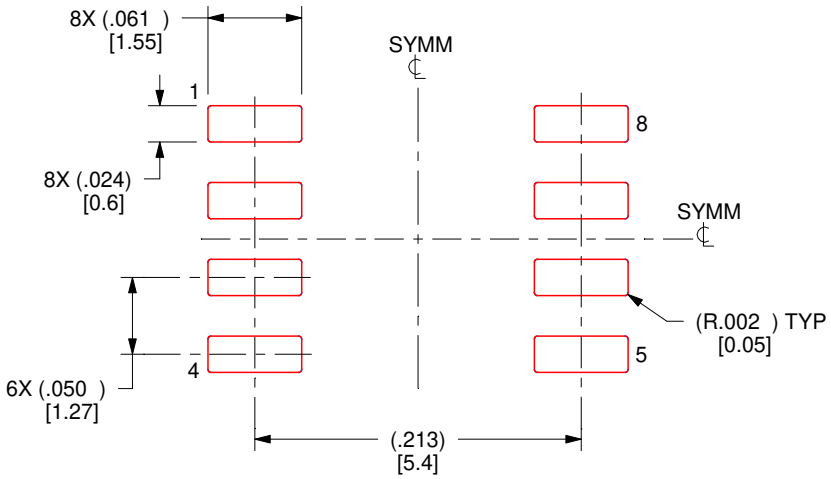
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

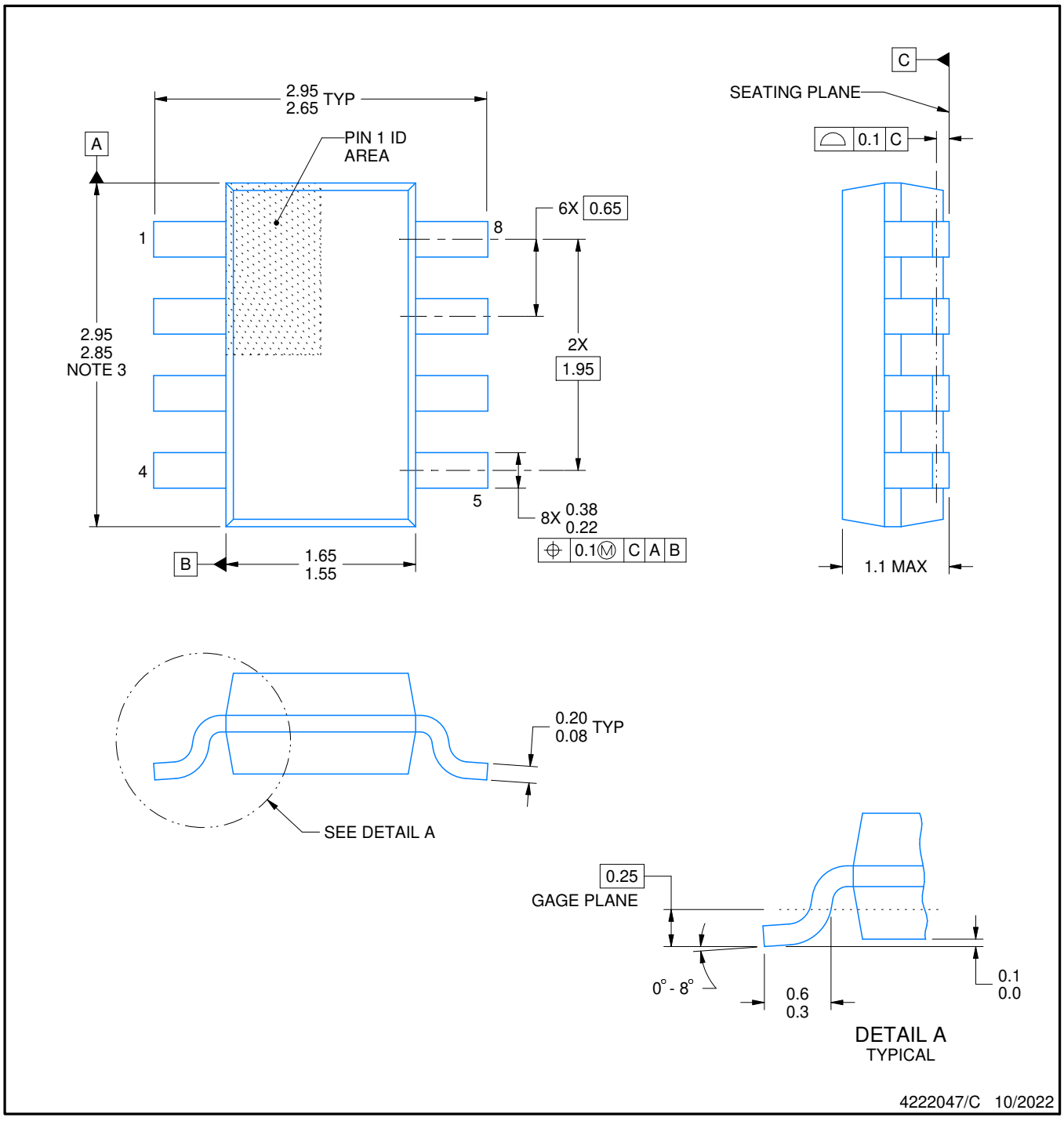
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DDF0008A

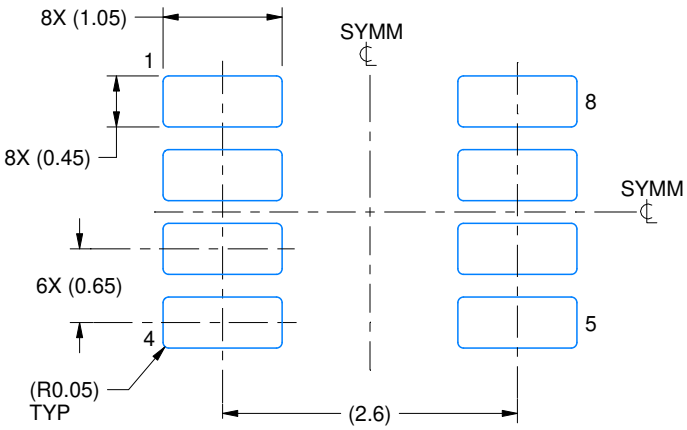
SOT-23 - 1.1 mm max height

PLASTIC SMALL OUTLINE

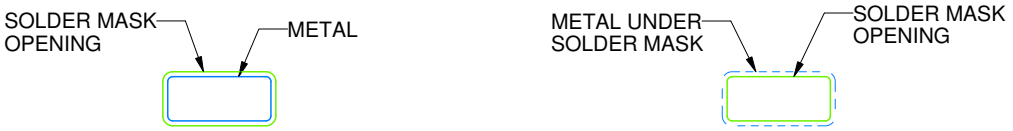


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
SCALE:15X



NON SOLDER MASK
DEFINED

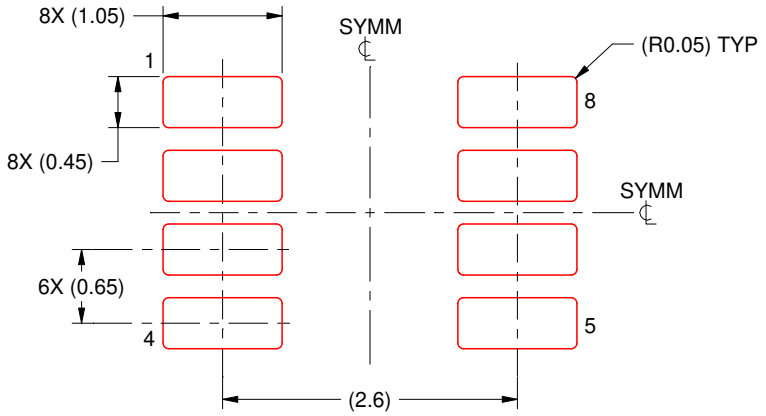
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4222047/C 10/2022

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4222047/C 10/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

DRB 8 VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

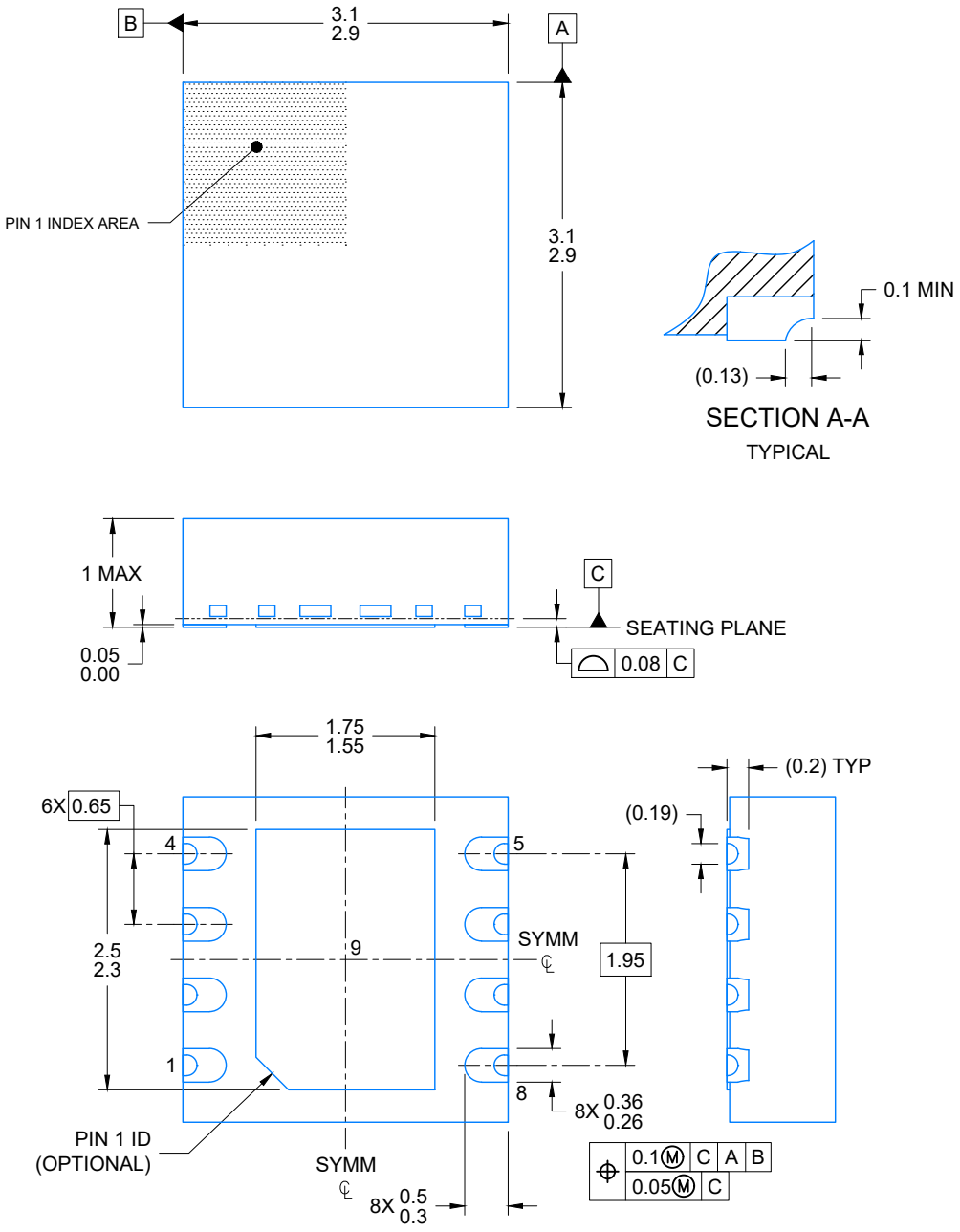
4203482/L

PACKAGE OUTLINE

DRB0008J

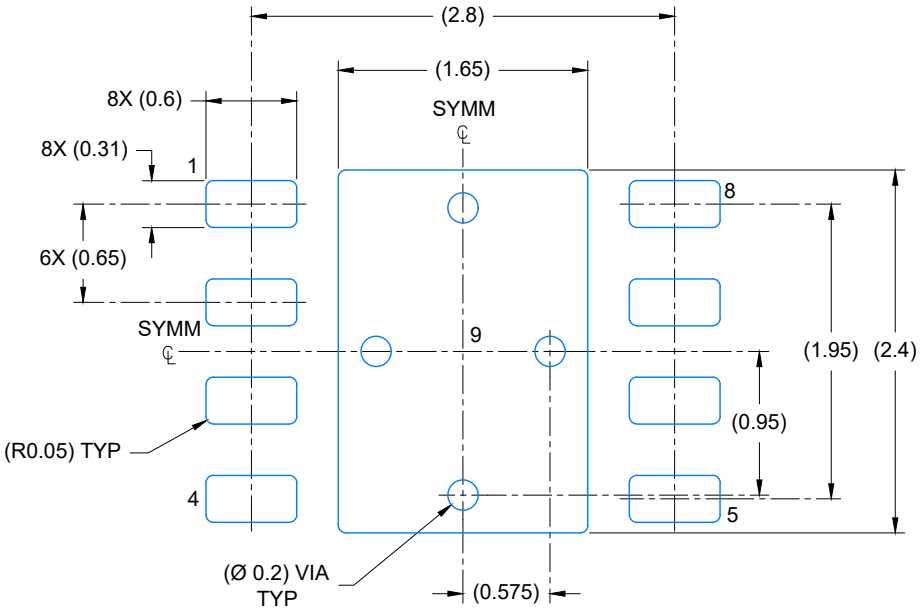
VSON - 1 mm max height

PLASTIC QUAD FLAT PACK- NO LEAD

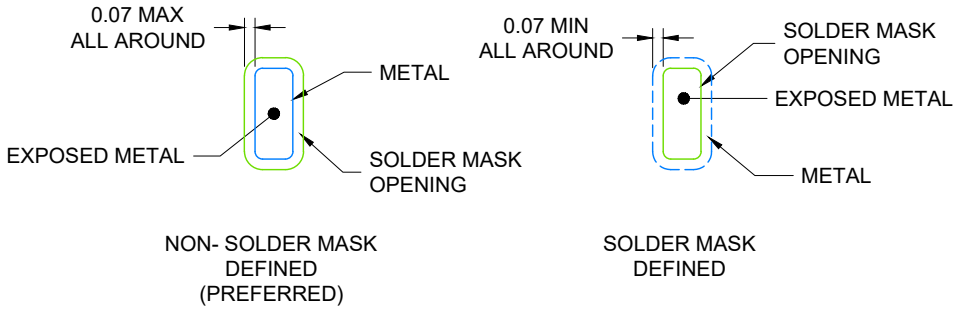


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



SOLDER MASK DETAILS

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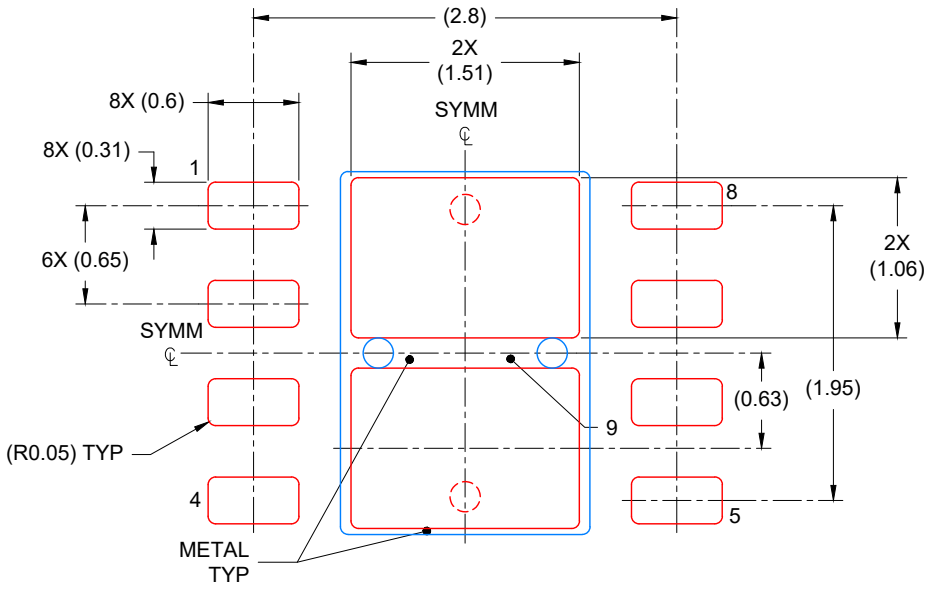
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
81% PRINTED COVERAGE BY AREA
SCALE: 20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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