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MC14067B

Analog Multiplexers / Demultiplexers

The MC14067 multiplexer/demultiplexer is a digitally controlled analog switch featuring low ON resistance and very low leakage current. This device can be used in either digital or analog applications.

The MC14067 is a 16−channel multiplexer/demultiplexer with an inhibit and four binary control inputs A, B, C, and D. These control inputs select 1−of−16 channels by turning ON the appropriate analog switch (see MC14067 truth table.)

Features

- Low OFF Leakage Current
- Matched Channel Resistance
- Low Quiescent Power Consumption
- Low Crosstalk Between Channels
- Wide Operating Voltage Range: 3 to 18 V
- Low Noise
- Pin for Pin Replacement for CD4067B
- These Devices are Pb−Free and are RoHS Compliant
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable

MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	− 0.5 to + 18.0	V
V_{in}, V_{out}	Input or Output Voltage Range (DC or Transient)	− 0.5 to V_{DD} + 0.5	V
I_{in}	Input Current (DC or Transient), per Control Pin	±10	mA
I_{sw}	Switch Through Current	±25	mA
P_D	Power Dissipation, per Package (Note 1)	500	mW
T_A	Ambient Temperature Range	− 55 to + 125	°C
T_{stg}	Storage Temperature Range	− 65 to + 150	°C
T_L	Lead Temperature (8−Second Soldering)	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Temperature Derating:
   Plastic “P and D/DW” Packages: − 7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

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SOIC−24
DW SUFFIX
CASE 751E

MARKING DIAGRAM

A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

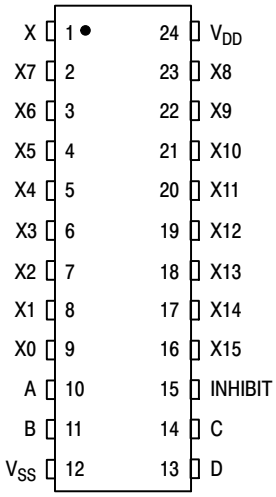
ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

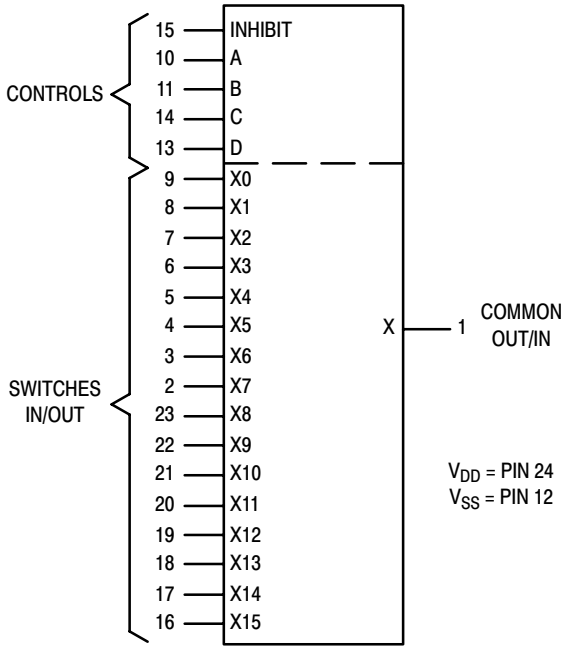
TRUTH TABLE

Control Inputs					Selected Channel
A	B	C	D	Inh	
X	X	X	X	1	None
0	0	0	0	0	X0
1	0	0	0	0	X1
0	1	0	0	0	X2
1	1	0	0	0	X3
0	0	1	0	0	X4
1	0	1	0	0	X5
0	1	1	0	0	X6
1	1	1	0	0	X7
0	0	0	1	0	X8
1	0	0	1	0	X9
0	1	0	1	0	X10
1	1	0	1	0	X11
0	0	1	1	0	X12
1	0	1	1	0	X13
0	1	1	1	0	X14
1	1	1	1	0	X15

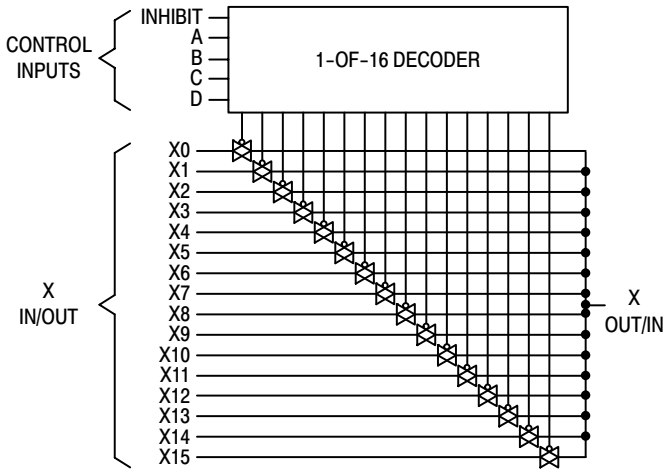
PIN ASSIGNMENT



16−Channel Analog Multiplexer/Demultiplexer



FUNCTIONAL DIAGRAM



ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD}	Test Conditions	– 55°C Min	– 55°C Max	25°C Min	25°C Typ (2)	25°C Max	125°C Min	125°C Max	Unit
SUPPLY REQUIREMENTS (Voltages Referenced to V_{SS})											
Power Supply Voltage Range	V_{DD}	–		3.0	18	3.0	–	18	3.0	18	V
Quiescent Current Per Package	I_{DD}	5.0 10 15	Control Inputs: V_{in} = V_{SS} or V_{DD}, Switch I/O: $V_{SS} \le V_{I/O} \le V_{DD}$, and $\Delta V_{switch} \le 500$ mV (3)	– – –	5.0 10 20	– – –	0.005 0.010 0.015	5.0 10 20	– – –	150 300 600	μA
Total Supply Current (Dynamic Plus Quiescent, Per Package	$I_{D(AV)}$	5.0 10 15	T_A = 25°C only (The channel component, $(V_{in} - V_{out})/R_{on}$, is not included.)	Typical			(0.07 μA/kHz) f + I_{DD} (0.20 μA/kHz) f + I_{DD} (0.36 μA/kHz) f + I_{DD}				μA
CONTROL INPUTS — INHIBIT, A, B, C, D (Voltages Referenced to V_{SS})											
Low−Level Input Voltage	V_{IL}	5.0 10 15	R_{on} = per spec, I_{off} = per spec	– – –	1.5 3.0 4.0	– – –	2.25 4.50 6.75	1.5 3.0 4.0	– – –	1.5 3.0 4.0	V
High−Level Input Voltage	V_{IH}	5.0 10 15	R_{on} = per spec, I_{off} = per spec	3.5 7.0 11	– – –	3.5 7.0 11	2.75 5.50 8.25	– – –	3.5 7.0 11	– – –	V
Input Leakage Current	I_{in}	15	V_{in} = 0 or V_{DD}	–	± 0.1	–	±0.00001	± 0.1	–	1.0	μA
Input Capacitance	C_{in}	—		–	–	–	5.0	7.5	–	–	pF
SWITCHES IN/OUT AND COMMONS OUT/IN — X, Y (Voltages Referenced to V_{SS})											
Recommended Peak−to−Peak Voltage Into or Out of the Switch	$V_{I/O}$	–	Channel On or Off	0	V_{DD}	0	–	V_{DD}	0	V_{DD}	V_{p-p}
Recommended Static or Dynamic Voltage Across the Switch (3) (Figure 1)	ΔV_{switch}	–	Channel On	0	600	0	–	600	0	300	mV
Output Offset Voltage	V_{OO}	–	V_{in} = 0 V, No Load	–	–	–	10	–	–	–	μV
ON Resistance	R_{on}	5.0 10 15	$\Delta V_{switch} \le 500$ mV (3), $V_{in} = V_{IL}$ or V_{IH} (Control), and V_{in} 0 to V_{DD} (Switch)	– – –	800 400 220	– – –	250 120 80	1050 500 280	– – –	1300 550 320	Ω
ΔON Resistance Between Any Two Channels in the Same Package	ΔR_{on}	5.0 10 15		– – –	70 50 45	– – –	25 10 10	70 50 45	– – –	135 95 65	Ω
Off−Channel Leakage Current (Figure 2)	I_{off}	15	$V_{in} = V_{IL}$ or V_{IH} (Control) Channel to Channel or Any One Channel	–	± 100	–	± 0.05	±100	–	±1000	nA
Capacitance, Switch I/O	$C_{I/O}$	–	Inhibit = V_{DD}	–	—	—	10	–	–	–	pF
Capacitance, Common O/I	$C_{O/I}$	–	Inhibit = V_{DD} (MC14067B) (MC14097B)	 – –	 – –	 – –	 100 60	 – –	 – –	 – –	pF
Capacitance, Feedthrough (Channel Off)	$C_{I/O}$	– –	Pins Not Adjacent Pins Adjacent	–	–	–	0.47	–	–	–	pF

2. Data labeled “Typ” is not to be used for design purposes, but is intended as an indication of the IC’s potential performance.
3. For voltage drops across the switch (ΔV_{switch}) > 600 mV (> 300 mV at high temperature), excessive V_{DD} current may be drawn; i.e. the current out of the switch may contain both V_{DD} and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded. (See first page of this data sheet.)

ELECTRICAL CHARACTERISTICS (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	$V_{DD} - V_{SS}$ Vdc	Typ (4)	Max	Unit
Propagation Delay Times Channel Input–to–Channel Output (R_L = 200 kΩ) MC14067B	t_{PLH}, t_{PHL} (Figure 3)	5.0 10 15	35 15 12	90 40 30	ns
Propagation Delay Times Channel Input–to–Channel Output (R_L = 1.0 kΩ) MC14067B	t_{PLH}, t_{PHL} (Figure 3)	5.0 10 15		50 30 20	ns
Control Input–to–Channel Output Channel Turn–On Time (R_L = 10 kΩ) MC14067B	t_{PZH}, t_{PZL} (Figure 4)	5.0 10 15	240 115 75	600 290 190	ns
Channel Turn–Off Time (R_L = 300 kΩ) MC14067B	t_{PHZ}, t_{PLZ} (Figure 4)	5.0 10 15	250 120 75	625 300 190	ns
Channel Turn–Off Time (R_L = 10 kΩ) MC14067B	(Figure 4)	5.0 10 15		625 450 350	ns
Any Pair of Address Inputs to Output MC14067B	t_{PLH}, t_{PHL}	5.0 10 15	280 115 85	700 290 215	ns
Second Harmonic Distortion (R_L = 10 kΩ, f = 1 kHz, V_{in} = 5 V_{p-p})	–	10	0.3	–	%
ON Channel Bandwidth [R_L = 50 Ω, V_{in} = 1/2 ($V_{DD} - V_{SS}$) $_{p-p}$(sine–wave)] 20 Log10 (V_{out}/V_{in}) = – 3 dB MC14067B	BW (Figure 5)	10	15	–	MHz
Off Channel Feedthrough Attenuation [R_L = 50 Ω, V_{in} = 1/2 (V_{DD}–V_{SS}) $_{p-p}$(sine–wave)] f_{in} = 20 MHz – MC14067B	– (Figure 5)	10	– 40	–	dB
Channel Separation [R_L = 1 kΩ, V_{in} = 1/2 (V_{DD}–V_{SS}) $_{p-p}$ (sine–wave)] f_{in} = 20 MHz	– (Figure 6)	10	– 40	–	dB
Crosstalk, Control Inputs–to–Common O/I (R1 = 1 kΩ, R_L = 10 kΩ, Control t_r = t_f = 20 ns, Inhibit = V_{SS})	– (Figure 7)	10	30	–	mV

4. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.

ORDERING INFORMATION

Device	Package	Shipping†
MC14067BDWG	SOIC−24 (Pb−Free)	30 Units / Rail
NLV14067BDWG*		
MC14067BDWR2G	SOIC−24 (Pb−Free)	1000 Units / Tape & Reel
NLV14067BDWR2G*		

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

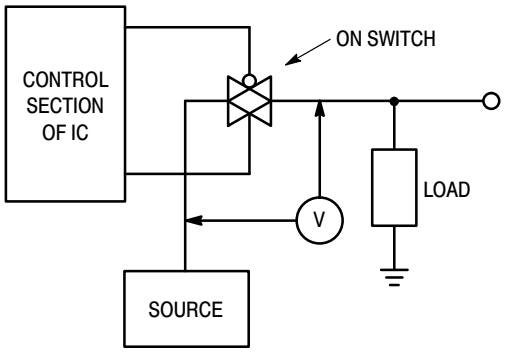


Figure 1. ΔV Across Switch

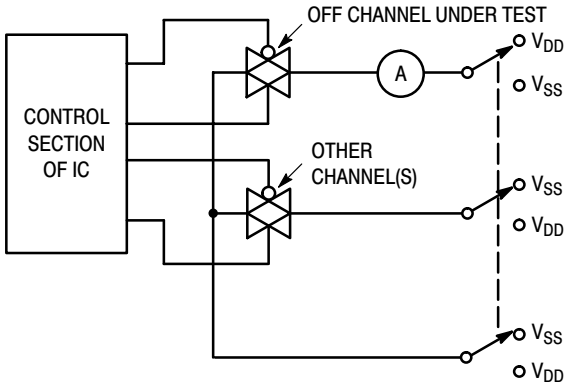


Figure 2. Off Channel Leakage

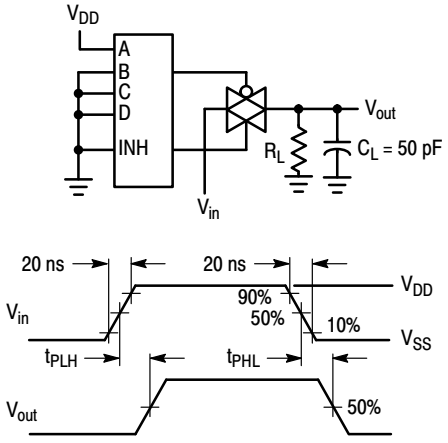


Figure 3. Propagation Delay Test Circuit and Waveforms V_{in} to V_{out}

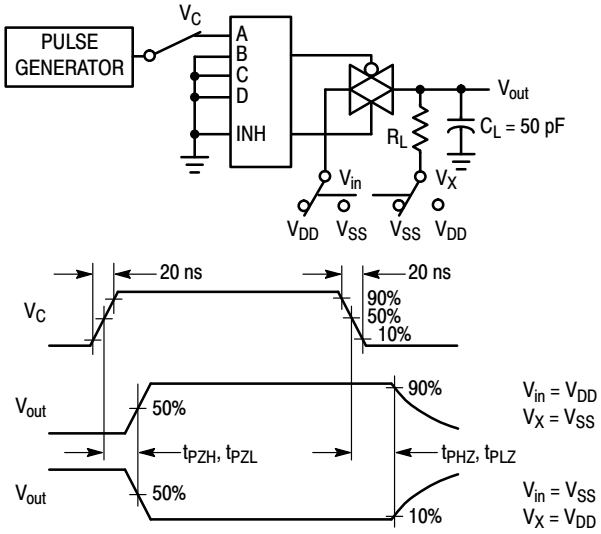


Figure 4. Turn−On and Delay Turn−Off Test Circuit and Waveforms

A, B, and C inputs used to turn ON or OFF the switch under test.

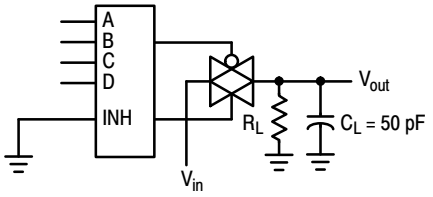


Figure 5. Bandwidth and Off−Channel Feedthrough Attenuation

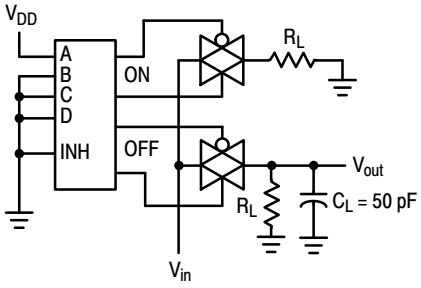


Figure 6. Channel Separation (Adjacent Channels Used for Setup)

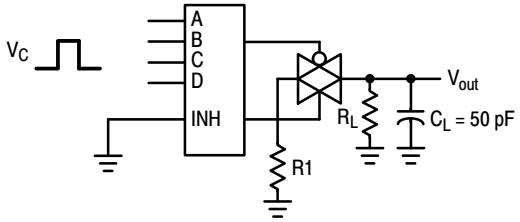


Figure 7. Crosstalk, Control to Common O/I

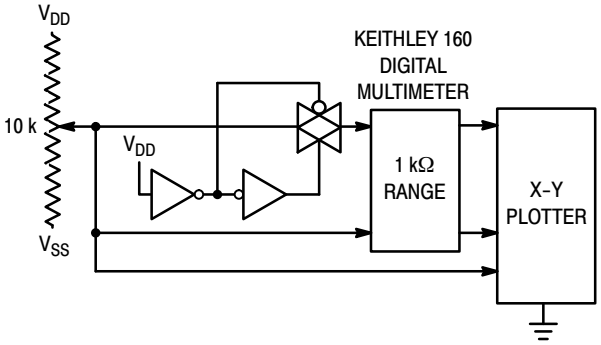


Figure 8. Channel Resistance (R_{ON}) Test Circuit

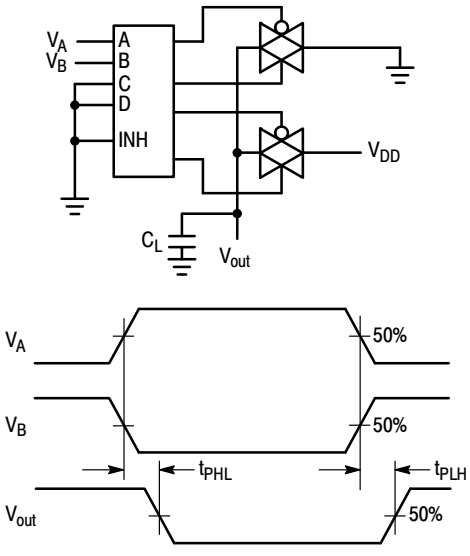


Figure 9. Propagation Delay, Any Pair of Address Inputs to Output

TYPICAL RESISTANCE CHARACTERISTICS

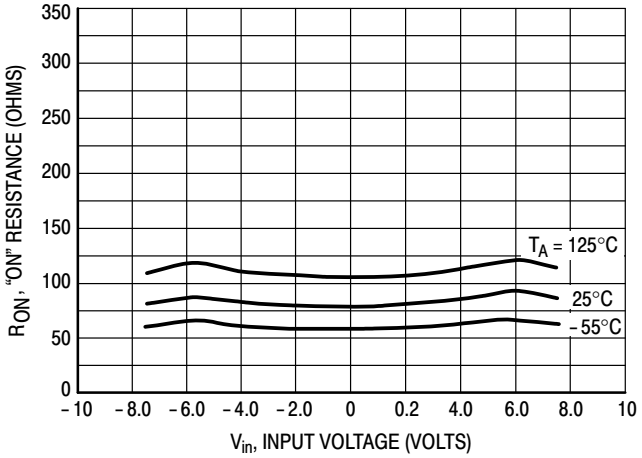


Figure 10. V_{DD} = 7.5 V, V_{SS} = − 7.5 V

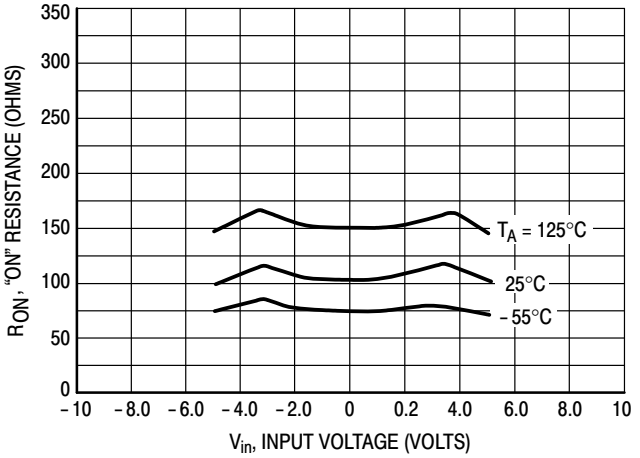


Figure 11. V_{DD} = 5.0 V, V_{SS} = − 5.0 V

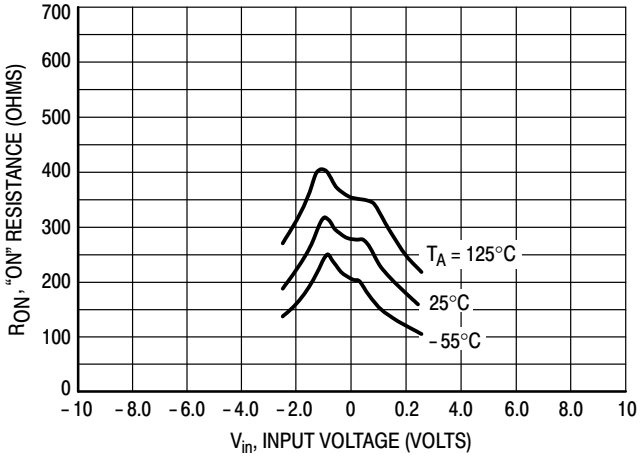


Figure 12. V_{DD} = 2.5 V, V_{SS} = − 2.5 V

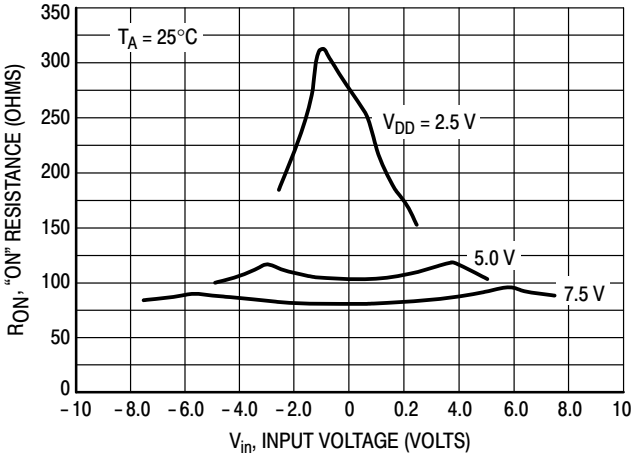


Figure 13. Comparison at 25°C, $V_{DD} = -V_{SS}$

APPLICATIONS INFORMATION

Figure A illustrates use of the Analog Multiplexer / Demultiplexer. The 0−to−5 V Digital Control signal is used to directly control a 5 V_{p-p} analog signal.

The digital control logic levels are determined by V_{DD} and V_{SS}. The V_{DD} voltage is the logic high voltage; the V_{SS} voltage is logic low. For the example. V_{DD} = + 5 V = logic high at the control inputs; V_{SS} = GND = 0 V = logic low.

The maximum analog signal level is determined by V_{DD} and V_{SS}. The analog voltage must swing neither higher than V_{DD} nor lower than V_{SS}. The example shows a 5 V_{p-p} signal which allows no margin at either peak. If voltage transients above V_{DD} and/or below V_{SS} are anticipated on the analog channels, external diodes (D_x) are recommended as shown in Figure B. These diodes should be small signal types able to absorb the maximum anticipated current surges during clipping.

The absolute maximum potential difference between V_{DD} and V_{SS} is 18.0 volts. Most parameters are specified up to 15 V which is the recommended maximum difference between V_{DD} and V_{SS}.

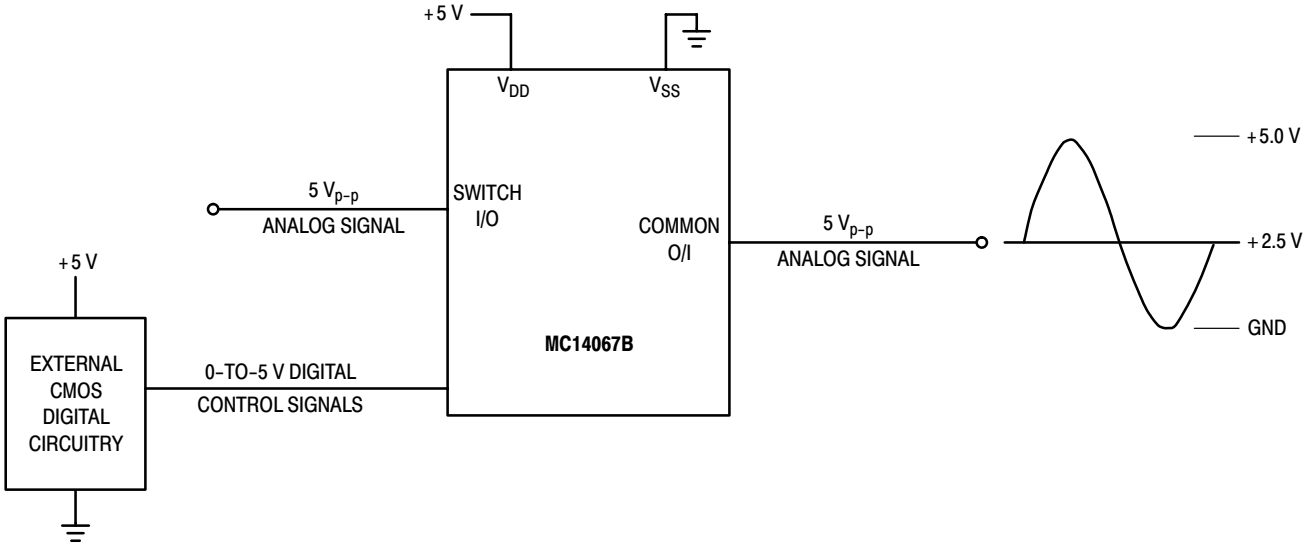


Figure A. Application Example

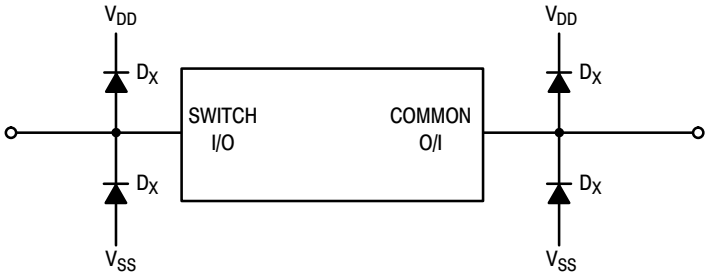
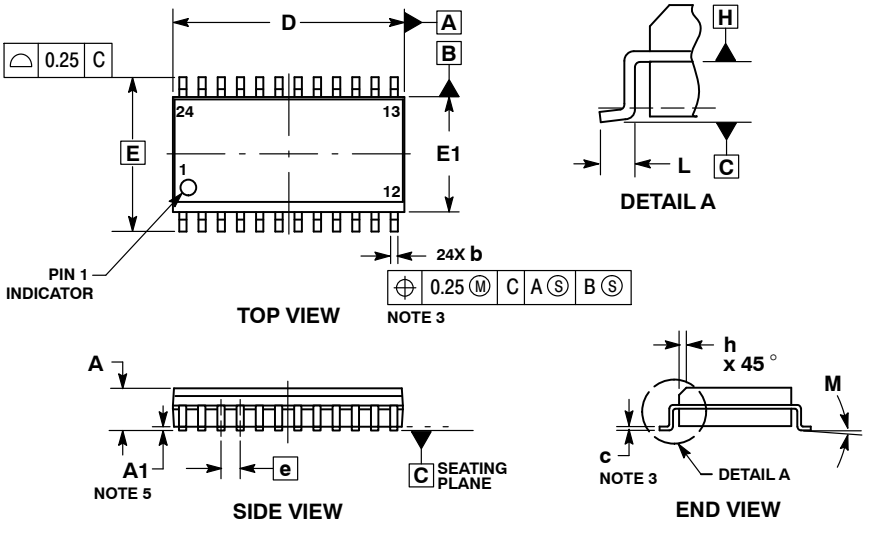


Figure B. External Germanium or Schottky Clipping Diodes

PACKAGE DIMENSIONS

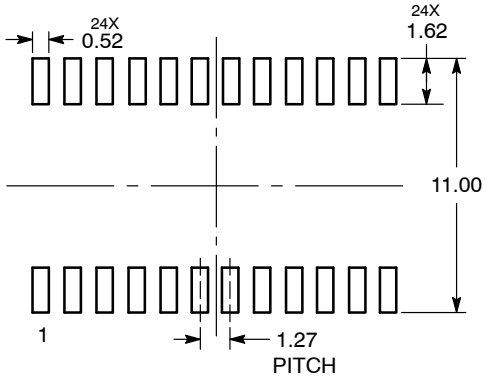
SOIC−24 WB
CASE 751E−04
ISSUE F



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD AND ARE MEASURED BETWEEN 0.10 AND 0.25 FROM THE LEAD TIP.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER SIDE. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
5. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

	MILLIMETERS	
DIM	MIN	MAX
A	2.35	2.65
A1	0.13	0.29
b	0.35	0.49
c	0.23	0.32
D	15.25	15.54
E	10.30 BSC	
E1	7.40	7.60
e	1.27 BSC	
h	0.25	0.75
L	0.41	0.90
M	0 °	8 °

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
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P.O. Box 5163, Denver, Colorado 80217 USA
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Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
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