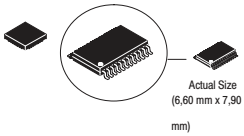


MULTICHEMISTRY BATTERY CHARGER CONTROLLER AND SYSTEM POWER SELECTOR

FEATURES

- **Dynamic Power Management, DPM Minimizes Battery Charge Time**
- **Integrated Selector Supports Battery Conditioning and Smart Battery Learn Cycle**
- **Zero Volt Operation**
- **Selector Feedback Circuit Ensures Break-Before-Make Transition**
- **±0.4% Charge Voltage Accuracy, Suitable for Charging Li-Ion Cells**
- **±4% Charge Current Accuracy**
- **300-kHz Integrated PWM Controller for High-Efficiency Buck Regulation**
- **Depleted Battery Detection and Indication to Protect Battery From Over Discharge**
- **20-µA Sleep Mode Current for Low Battery Drain**
- **24-Pin TSSOP Package and 5 mm × 5 mm QFN package (bq24703 only)**

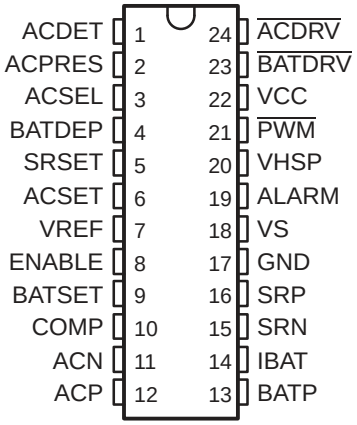
DESCRIPTION

The bq24702/bq24703 is a highly integrated battery charge controller and selector tailored for notebook and sub-notebook PC applications.

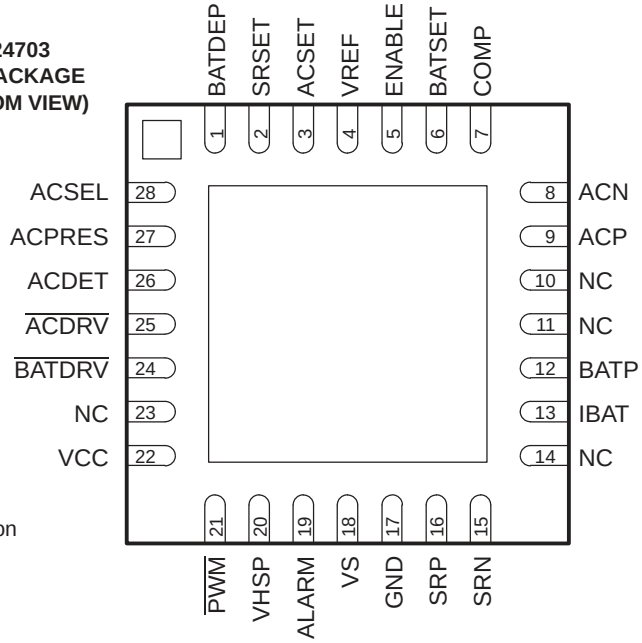
The bq24702/bq24703 uses dynamic power management (DPM) to minimize battery charge time by maximizing use of available wall-adapter power. This is achieved by dynamically adjusting the battery charge current based on the total system (adapter) current.

The bq24702/bq24703 uses a fixed frequency, pulse width modulator (PWM) to accurately control battery charge current and voltage. Charge current limits can be programmed from a keyboard controller DAC or by external resistor dividers from the precision 5-V, ±0.6%, externally bypassed voltage reference (VREF), supplied by the bq24702/bq24703.

bq24702, bq24703
PW PACKAGE
(TOP VIEW)



bq24703
RHD PACKAGE
(BOTTOM VIEW)



NC - No internal connection

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION (CONTINUED)

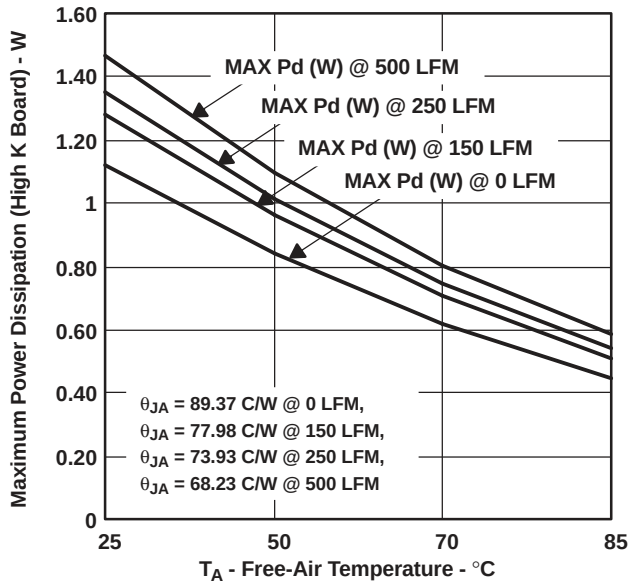
The battery voltage limit can be programmed by using the internal 1.196-V, ±0.5% precision reference, making it suitable for the critical charging demands of lithium-ion cells. Also, the bq24702/bq24703 provides an option to override the precision reference and drive the error amplifier either directly from an external reference or from a resistor divider off the 5 V supplied by the integrated circuit.

The selector function allows the manual selection of the system power source, battery or wall-adapter power. The bq24702/bq24703 supports battery-conditioning and battery-learn cycles through the ACSEL function. The ACSEL function allows manual selection of the battery or wall power as the main system power. It also provides autonomous switching to the remaining source (battery or ac power) should the selected system power source terminate (refer to Available Options table for the differences between the bq24702 and the bq24703). The bq24702/bq24703 also provides an alarm function to indicate a depleted battery condition.

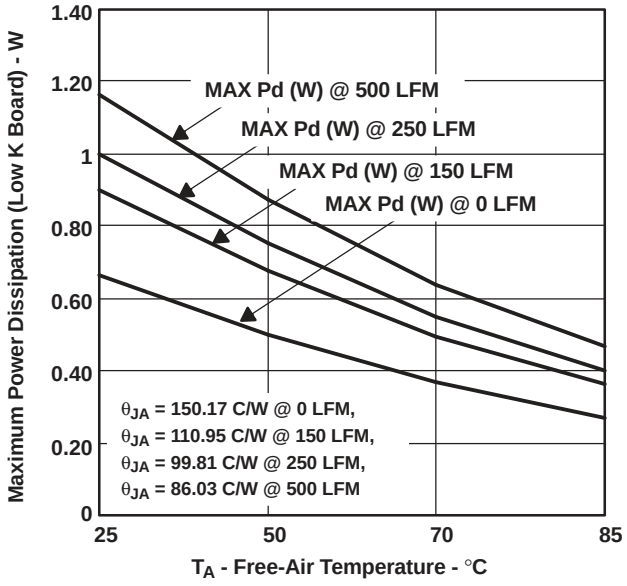
The bq24702/bq24703 PWM controller is ideally suited for operation in a buck converter for applications when the wall-adapter voltage is greater than the battery voltage.

DISSIPATION RATINGS

MAXIMUM POWER DISSIPATION (HIGH K BOARD) vs FREE-AIR TEMPERATURE



MAXIMUM POWER DISSIPATION (LOW K BOARD) vs FREE-AIR TEMPERATURE



A. The JEDEC low K (1s) board design used to derive this data was a 3-inch × 3-inch, two layer board with 2 ounce copper traces on top of the board.

B. The JEDEC high K (1s) board design used to derive this data was a 3-inch × 3-inch, multilayer board with 1 ounce internal power and ground planes and 2 ounce copper traces on top and bottom of the board.

AVAILABLE OPTIONS

CONDITION $20°C \le T_J \le 125°C$	SELECTOR OPERATION	
	bq24702PW	**bq24703RHD**
BATTERY AS POWER SOURCE		
Battery removal	Automatically selects ac + alarm	Automatically selects ac + alarm
Battery reinserted	Selection based on selector inputs	Adapter latched until adapter is removed or ac select toggles.
AC AS POWER SOURCE		
AC removal	Automatically selects battery	Automatically selects battery
AC reinserted	Selection based on selector inputs	Selection based on selector inputs
DEPLETED BATTERY CONDITION		
Battery as power source	Sends ALARM signal	**Automatically selects ac** Sends ALARM signal
AC as power source	Sends ALARM signal	Sends ALARM signal
ALARM SIGNAL ACTIVE		
	Depleted battery condition	Depleted battery condition
	When selector input is not equal to selector output (single pulse alarm)	

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1) (2)

		VALUE	UNIT
V_{CC}	Supply voltage range	–0.3 to 30	V
	Battery voltage range: SRP, SRN	–0.3 to 30	V
	Input voltage: ACN, ACP	–0.3 to 30	V
T_J	Virtual junction temperature range	–40 to 125	°C
	Maximum source/sink current VHSP	50	mA
	Maximum ramp rate for V_{CC}	10	V/µs
	Maximum sink current ACPRES, COMP, ALARM	2.5	mA
	Maximum ramp rate for $V_{(BAT)}$	10	V/µs
	Maximum source/sink current $\overline{\text{BATDRV}}$	10	mA
	Maximum source/sink current $\overline{\text{ACDRV}}$	10	mA
	Maximum source/sink current $\overline{\text{PWM}}$	50	mA
	Maximum source/sink current pulsed $\overline{\text{ACDRV}}$, (10-µs rise time, 10-µs fall time, 1-ms pulse width, single pulse)	50	mA
	Maximum source current VREF	30	mA
	Maximum source current SRP	100	mA
	Maximum difference voltage SRP–SRN	30	V
T_{stg}	Storage temperature range	–65 to 150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to ground. Currents are positive into and negative out of the specified terminals. Consult the *Packaging* section of the data book for thermal limitations and considerations of the package.

RECOMMENDED OPERATING CONDITIONS

($T_A = T_{OPR}$) all voltages relative to V_{SS}

		MIN	MAX	UNIT
Supply voltage, (VCC)	Analog and PWM operation	7	28	V
	Selector operation	4.5	28	
Negative ac current sense, (ACN)		7	28	V
Positive ac current sense, (ACP)		7	28	V
Negative battery current sense, (SRN)		5	28	V
Positive battery current sense, (SRP)		5	28	V
AC or adapter power detection (ACDET)		0	5	V
AC power indicator (ACPRES)		0	5	V
AC adapter power select (ACSEL)		0	5	V
Depleted battery level (BATDEP)		0	5	V
Battery charge current programming voltage (SRSET)		0	2.5	V
Charge enable (ENABLE)		0	5	V
External override to an internal 0.5% precision reference (BATSET)		0	2.5	V
Inverting input to the PWM comparator (COMP)		0	5	V
Battery charge regulation voltage measurement input to the battery—voltage g_m amplifier (BATP)		0	5	V
Battery current differential amplifier output (IBAT)		0	5	V
System load voltage input pin (VS)		0	2.5	V
Depleted battery alarm output (ALARM)		0	5	V
Gate drive output ($\overline{PWM}$)		VHSP	VCC	V
Battery power source select output ($\overline{BATDRV}$)		0	28	V
AC or adapter power source selection output ($\overline{ACDRV}$)		VHSP	VCC	V
ACSET		0	2.5	V
Operating free-air temperature, T_A		-40	85	°C

ELECTRICAL CHARACTERISTICS

–40°C ≤ T_J ≤ 125°C, 7 V_{DC} ≤ V_{CC} ≤ 28 V_{DC}, all voltages relative to V_{SS} (unless otherwise specified)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
QUIESCENT CURRENT						
$I_{DD(OP)}$	Total chip operating current	ACPRES = High, EN = 0	1	1.6	6	mA
$I_{DD(SLEEP)}$	Total battery sleep current, ac not present	ACPRES = Low		22	28	µA
LOGIC INTERFACE DC CHARACTERISTICS						
V_{OL}	Low-level output voltage (ACPRES, ALARM)	I_{OL} = 1 mA			0.4	V
V_{IL}	Low-level input voltage (ACSEL, ENABLE)				0.6	V
V_{IH}	High-level input voltage (ACSEL, ENABLE)		1.8			V
$I_{(SINK1)}$	Sink current (ACPRES)	V_{OL} = 0.4	1.5	2	2.5	mA
$I_{(SINK2)}$	Sink current (ALARM)	V_{OL} = 0.4	1.5	2	2.5	mA
PWM OSCILLATOR						
$f_{OSC(PWM)}$	Oscillator frequency	0°C ≤ T_J ≤ 85°C	280	300	340	kHz
		–40°C ≤ T_J ≤ 125°C	240	300	350	
	Maximum duty cycle		100%			
	Input voltage for maximum dc (COMP)		3.8			V
	Minimum duty cycle				0%	
	Input voltage for minimum dc (COMP)				0.8	V
$V_{(RAMP)}$	Oscillator ramp voltage (peak-to-peak)		1.85	2.15	2.30	
$V_{IK(COMP)}$	Internal input clamp voltage (tracks COMP voltage for maximum dc)			3.8	4.5	
$I_{S(COMP)}$	Internal source current (COMP)	Error amplifier = OFF, $V_{(COMP)}$ = 1 V	70	110	140	µA
LEAKAGE CURRENT						
$I_{L(\overline{ACDET})}$	Leakage current, $\overline{ACDET}$	$V_{(ACDET)}$ = 5 V			0.2	µA
$I_{L(SRSET)}$	Leakage current, SRSET	$V_{(SRSET)}$ = 2.5 V			0.2	µA
$I_{L(ACSET)}$	Leakage current, ACSET	$V_{(ACSET)}$ = 2.5 V			0.2	µA
$I_{L(BATDEP)}$	Leakage current, BATDEP	$V_{(BATDEP)}$ = 5 V			0.2	µA
$I_{L(VS)}$	Leakage current, VS	$V_{(VS)}$ = 5 V			0.2	µA
$I_{L(ALARM)}$	Leakage current, ALARM	$V_{(ALARM)}$ = 5 V			0.2	µA
$I_{L(ACSEL)}$	Leakage current, ACSEL	$V_{(ACSEL)}$ = 5 V			0.2	µA
$I_{L(ENABLE)}$	Leakage current, ENABLE	$V_{(ENABLE)}$ = 5 V			0.2	µA
$I_{L(ACPRES)}$	Leakage current, ACPRES	$V_{(ACPRES)}$ = 5 V			0.2	µA
$I_{L(BATP)}$	Leakage current, BATP	$V_{(BATP)}$ = 5 V			0.2	µA
$I_{L(BATSET)}$	Leakage current, BATSET	$V_{(BATSET)}$ = 2.5 V			0.2	µA

ELECTRICAL CHARACTERISTICS (Continued)

–40°C ≤ T_J ≤ 125°C, 7 V_{DC} ≤ V_{CC} ≤ 28 V_{DC}, all voltages relative to V_{SS} (unless otherwise specified)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BATTERY CURRENT-SENSE AMPLIFIER						
g_m	Transconductance gain		75	120	175	mA/V
CMRR	Common-mode rejection ratio	See (1)		90		dB
V_{ICR}	Common-mode input (SRP, SRN) voltage range	VCC = SRN, SRP + 2 V	5		30	V
$I_{(SINK)}$	Sink current (COMP)	COMP = 1 V, (SRP–SRN) = 10 mV	0.5	1.5	2.5	mA
I_{IB}	Input bias current (SRP) (2)	$V_{(SRP)}$ = 16 V, (SRP–SRN) = 100 mV, SRSET = 2.5 V, VCC = 28	70	85	110	µA
	Input bias current accuracy ($I_{SRP} – I_{SRN}$)	(SRP - SRN) = 100 mV, SRSET= 2.5 V, VCC = 28 V, 0 ≤ T_J ≤ 125°C	–3	0	3	
$V_{(SET)}$	Battery current programming voltage (SRSET)		0		2.5	V
A_V	Battery current set gain	0.65 V ≤ SRSET ≤ 2.5 V, 8 V ≤ SRN ≤ 16 V (3)	24	25	26	V/V
	Total battery current-sense mid-scale accuracy	SRSET = 1.25 V, T_J = 25°C (4)	–5%		5%	
		SRSET = 1.25 V (4)	–6%		6%	
	Total battery current-sense full-scale accuracy	SRSET = 2.5 V, T_J = 25°C (4)	–3%		3%	
		SRSET = 2.5 V (4)	–4%		4%	

(1) Specified by design. Not production tested.

(2) $I_{(SRP)} = I_{(SRN)} = (V_{(SRSET)} / 50\ k\Omega) + ((V_{(SRP)} - V_{(SRN)} / 3\ k\Omega)$
example: If ($V_{(SRSET)}$ = 2.5 V) , ($V_{(SRP)}$ - $V_{(SRN)}$ = 100 mV) Then $I_{(SRP)} = I_{(SRN)}$ = 83 A

(3) $I_{BAT} = \frac{SRSET}{R_{SENSE}} \times \frac{1}{A_V}$

(4) Total battery-current set is based on the measured value of (SRP–SRN) = Δm, and the calculated value of (SRP–SRN) = ΔC, using the measured gain, A_V.

$$\Delta c = \frac{SRSET}{A_V}, \text{ Total accuracy in } \% = \frac{(\Delta m - \Delta c)}{\Delta c} \times 100, I_{(SRP)} - I_{(SRN)} = 0$$

ELECTRICAL CHARACTERISTICS (Continued)

–40°C ≤ T_J ≤ 125°C, 7 V_{DC} ≤ V_{CC} ≤ 28 V_{DC}, all voltages relative to V_{SS}, (unless otherwise specified)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADAPTER CURRENT-SENSE AMPLIFIER						
g_m	Transconductance gain		75	130	175	mA/V
CMRR	Common-mode rejection ratio	See (1)		90		dB
V_{ICR}	Common-mode input voltage range (ACP)		7		V_{CC}	V
$I_{(SINK)}$	Sink current (COMP)	COMP = 1 V, (ACP – ACN) = 10 mV	0.5	1.5	2.5	mA
I_{IB}	Input bias current (ACP, ACN)	ACP = ACN = 28 V, VCC = 28 V, ACSET = 2.5 V	40	50	65	A
	Input bias current accuracy ratio ($I_{(ACP)}$, $I_{(ACN)}$)	ACP = ACN = 28 V, VCC = 28 V, ACSET = 2.5 V, 0 ≤ T_J ≤ 125°C	–3	0	3	
$V_{(SET)}$	AC current programming voltage (ACSET)		0		2.5	V
A_V	AC current set gain	0.65 V ≤ ACSET ≤ 2.5 V, 12 V ≤ ACP ≤ 20 V (1)	24.5	25.3	26.5	V/V
	Total ac current-sense mid-scale accuracy	ACSET = 1.25 V, T_J = 25°C (2)	–5%		5%	
		ACSET = 1.25 V (2)	–6%		6%	
	Total ac current-sense full-scale accuracy	ACSET = 2.5 V, T_J = 25°C (2)	–3.5%		3.5%	
		ACSET = 2.5 V (2)	–4%		4%	
BATTERY VOLTAGE ERROR AMPLIFIER						
g_m	Transconductance gain		75	135	175	mA/V
CMRR	Common-mode rejection ratio	See (1)		90		dB
V_{ICR}	BATSET common-mode input voltage range		1		2.5	V
V_{IT}	Internal reference override input threshold voltage		0.20	0.25	0.35	V
$I_{(SINK)}$	Sink current COMP	COMP = 1 V, (BATP–BATSET) = 10 mV, BATSET = 1.25 V	0.5	1.5	2.5	mA
$V_{(FB)}$	Error-amplifier precision reference voltage	T_J = 25°C	1.190	1.196	1.202	V
		T_J = 0°C to 85°C	1.183	1.196	1.203	
		T_J = –40°C to 125°C	1.178	1.196	1.204	

(1) Calculation of the ac current: $I_{AC} = \frac{ACSET}{R_{SENSE}} \times \frac{1}{A_V}$

(2) Total ac-current set accuracy is based on the measured value of (ACP-ACN) = Δc, using the measured gain, A_V.

$\Delta c = \frac{ACSET}{A_V}$, Total accuracy in % $= \frac{(\Delta m - \Delta c)}{\Delta c} \times 100, I_{(ACP)} - I_{(ACN)} = 0$

ELECTRICAL CHARACTERISTICS (Continued)

–40°C ≤ T_J ≤ 125°C, 7 V_{DC} ≤ V_{CC} ≤ 28 V_{DC}, all voltages relative to V_{SS} (unless otherwise specified)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BATTERY CURRENT OUTPUT AMPLIFIER						
$G_{(TR)}$	Transfer gain	(SRP–SRN) = 5 mV(1)		20		V/V
$V_{I(BAT)}$	Battery current readback output voltage (IBAT)	(SRP–SRN) = 5 mV, SRP = 12 V, V_{CC} = 18 V, T_J = 25°C		100		mV
	Line rejection voltage	T_J = 25°C		10		mV/V
CM	Common-mode input range (SRP)		5		28	V
$V_{O(IBAT)}$	Battery current output voltage range (IBAT)		0		2.5	V
$I_{S(O)}$	Output source current (IBAT)	(SRP–SRN) = 100 mV	5	7.1	9.4	mA
	Total battery current readback full-scale accuracy	(SRP–SRN) = 50 mV, T_J = 25°C(1)	–3%		2.4%	
		(SRP–SRN) = 50 mV, 0°C ≤ T_J ≤ 85°C	–20%		20%	
		(SRP–SRN) = 100 mV, T_J = 25°C(1)	–1.5%		1.2%	
		(SRP–SRN) = 100 mV, 0°C < T_J < 85°C	–6%		8.5%	
5-V VOLTAGE REFERENCE						
V_{ref}	Output voltage (VREF)	T_J = 25°C	4.985	5	5.013	V
		T_J = 0°C to 85°C	4.946	5	5.013	
		T_J = 40°C to 85°C	4.946	5	5.03	V
		T_J = –40°C to 125°C	4.926	5	5.03	V
	Line regulation	I_{LOAD} = 5 mA		0.1	0.37	mV/V
	Load regulation	1 mA ≤ I_{LOAD} ≤ 5 mA		1.1	4	mV/mA
	Short circuit current		8	20	30	mA
	5V REF output capacitor	Capacitance	2.2		10	µF
	Output capacitor equivalent resistor	ESR	5		1000	mΩ
HALF SUPPLY REGULATOR						
$V_{(HSP)}$	Voltage regulation	$I_{(SINK)}$ = 20 mA, V_{CC} = 18 V	V_{CC} – 11	V_{CC} – 10.2	V_{CC} – 8.5	V
		$I_{(SINK)}$ = 1 mA, V_{CC} = 7 V			1.5	

(1) Battery readback transfer gain $G_{TR} = \frac{V_{IBAT}}{(SRP - SRN)}$

ELECTRICAL CHARACTERISTICS (Continued)

–40°C ≤ T_J ≤ 125°C, 7 V_{DC} ≤ V_{CC} ≤ 28 V_{DC} , all voltages relative to V_{SS} (unless otherwise specified)

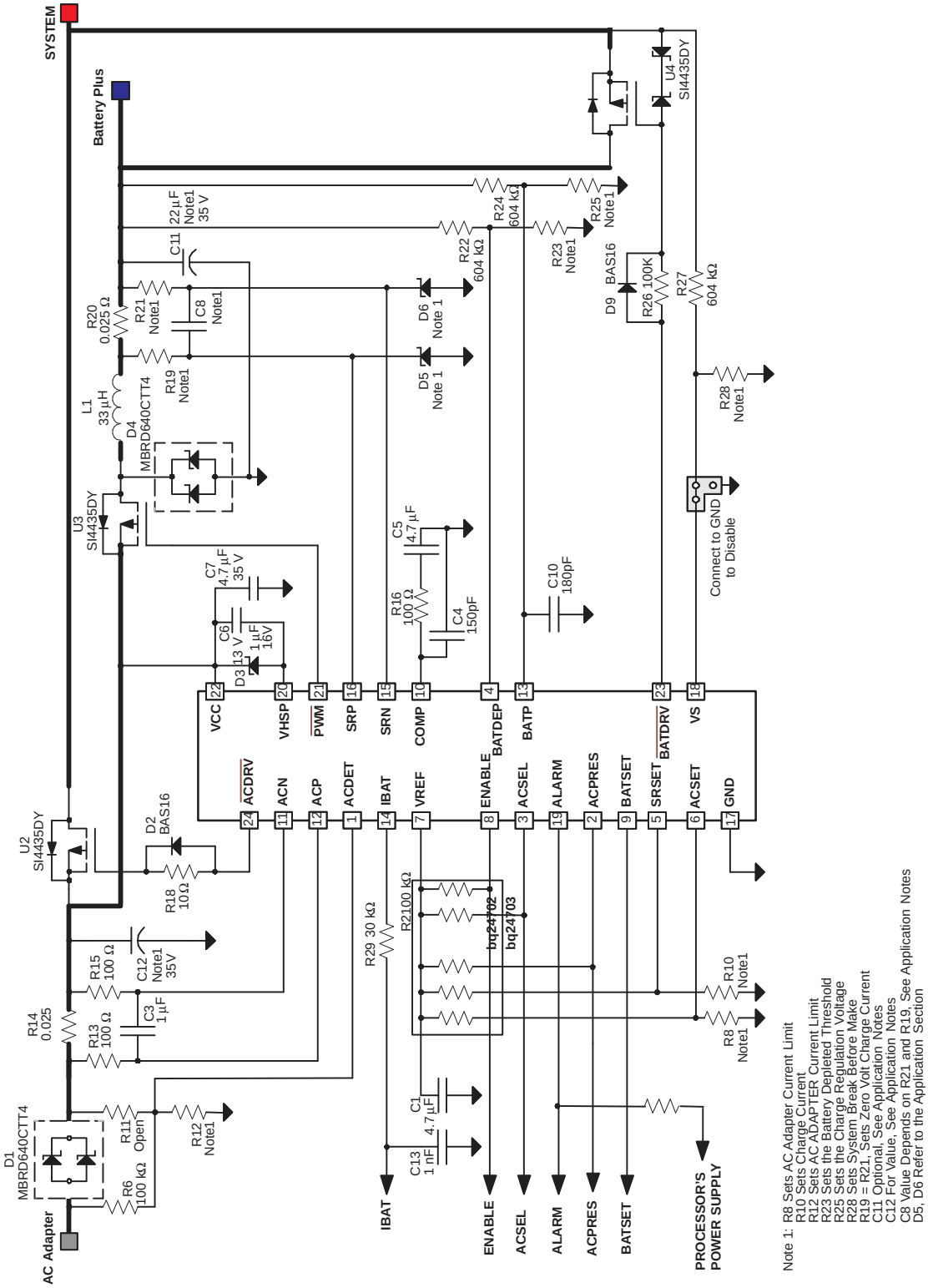
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
MOSFET GATE DRIVE						
	AC driver $R_{DS(on)}$ high	V_{CC} = 18 V, $I_{(\overline{ACDRV})}$ = 1 mA		85	150	Ω
	AC driver $R_{DS(on)}$ low	V_{CC} = 18 V, $I_{(\overline{ACDRV})}$ = 1 mA		55	110	Ω
	Battery driver $R_{DS(on)}$ high	V_{CC} = 18 V, $I_{(\overline{BATDRV})}$ = 1 mA		315	600	Ω
	Battery driver $R_{DS(on)}$ low	V_{CC} = 18 V, $I_{(\overline{BATDRV})}$ = 1 mA		70	115	Ω
t_{da}	Time delay from ac driver off to battery driver on	ACSEL 2.4 V ^ 0.2 V		1.2	2	µs
t_{db}	Time delay from battery driver off to ac driver on	ACSEL 0.2 V $ 2.4 V		2.4	3.3	µs
V_{OH}	PWM driver high-level output voltage	I_O = –10 mA, VCC = 18 V	V_{CC} –0.18	V_{CC} –0.09		V
		I_O = –50 mA, VCC = 18 V	V_{CC} –1.2	V_{CC} –0.8		
	PWM driver $R_{DS(on)}$ high			7	14	Ω
V_{OL}	PWM driver low-level output voltage	I_O = 10 mA, VCC = 18 V		V_{HSP}+0.1	V_{HSP}+0.4	V
		I_O = 50 mA, VCC = 18 V		V_{HSP}+0.6	V_{HSP}+1.2	
	PWM driver $R_{DS(on)}$ low			5	8.5	Ω
SELECTOR						
$V_{(ACPRES)}$	AC presence detect voltage		1.194	1.246	1.286	V
		–40°C to 85°C	1.208	1.246	1.285	
$V_{IT(ACPRES)}$	AC presence hysteresis			1%		
$t_{d(ACPRES)}$	Deglitch delay for adapter insertion			100		µs
$V_{(BATDEP)}$	Battery depletion ALARM trip voltage	See (1)	1.194	1.246	1.286	V
		–40°C to 85°C	1.208	1.246	1.285	
$V_{(NOBAT)}$	No battery detect, switch to ACDRV	bq24702 only(1)	0.869	1	1.144	V
		–40°C to 85°C	0.880	1	1.118	
$t_{(BATSEL)}$	Battery select time (ACSEL low to BATDRV low)	VS < BATP, 50% threshold, ACSEL 2.4 V ↓ 0.2 V	1	2.5	3.5	µs
$t_{(ACSEL)}$	AC select time (ACSEL high to ACDRV low)	ACSEL 0.2 V ↑ 2.4 V	1	2.5	5	µs
$V_{(VS)}$	VS voltage to enable BATDRV	BATP = 1 V	0.98	1	1.02	V
$V_{IT(VS)}$	VS voltage hysteresis	VS > BATP	20	35	85	mV
ZERO VOLT OPERATION(2)						
$r_{DS(on)}$	Static drain source on-state resistance	V_{CC} = 7 V, T_J = 125°C, I_O = 100 mA		5.3	8.7	Ω
	Zero volt operation threshold	BATDEP increasing	0.743	0.794	0.840	V
		BATDEP decreasing	0.570	0.62	0.656	

(1) Total battery current readback accuracy is based on the measured value of V_{IBAT}, V_{IBATm}, and the calculated value of V_{IBAT}, V_{IBATc}, using the measured value of the transfer gain, GTR.

$$V_{IBATc} = (SRP - SRN) \times GTR \quad \text{Total Accuracy in \%} = \frac{V_{IBATm} - V_{IBATc}}{V_{IBATm}} \times 100$$

(2) See Table 1 to determine the logic operation of the bq24702 and the bq24703.

APPLICATION DIAGRAM



Note 1: R8 Sets AC Adapter Current Limit
R10 Sets Charge Current
R12 Sets AC ADAPTER Current Limit
R23 Sets the Battery Depleted Threshold
R25 Sets the Charge Regulation Voltage
R28 Sets System Break Before Make
R19 = R21, Sets Zero Volt Charge Current
C11 Optional, See Application Notes
C12 For Value, See Application Notes
C8 Value Depends on R21 and R19, See Application Notes
D5, D6 Refer to the Application Section

BLOCK DIAGRAM

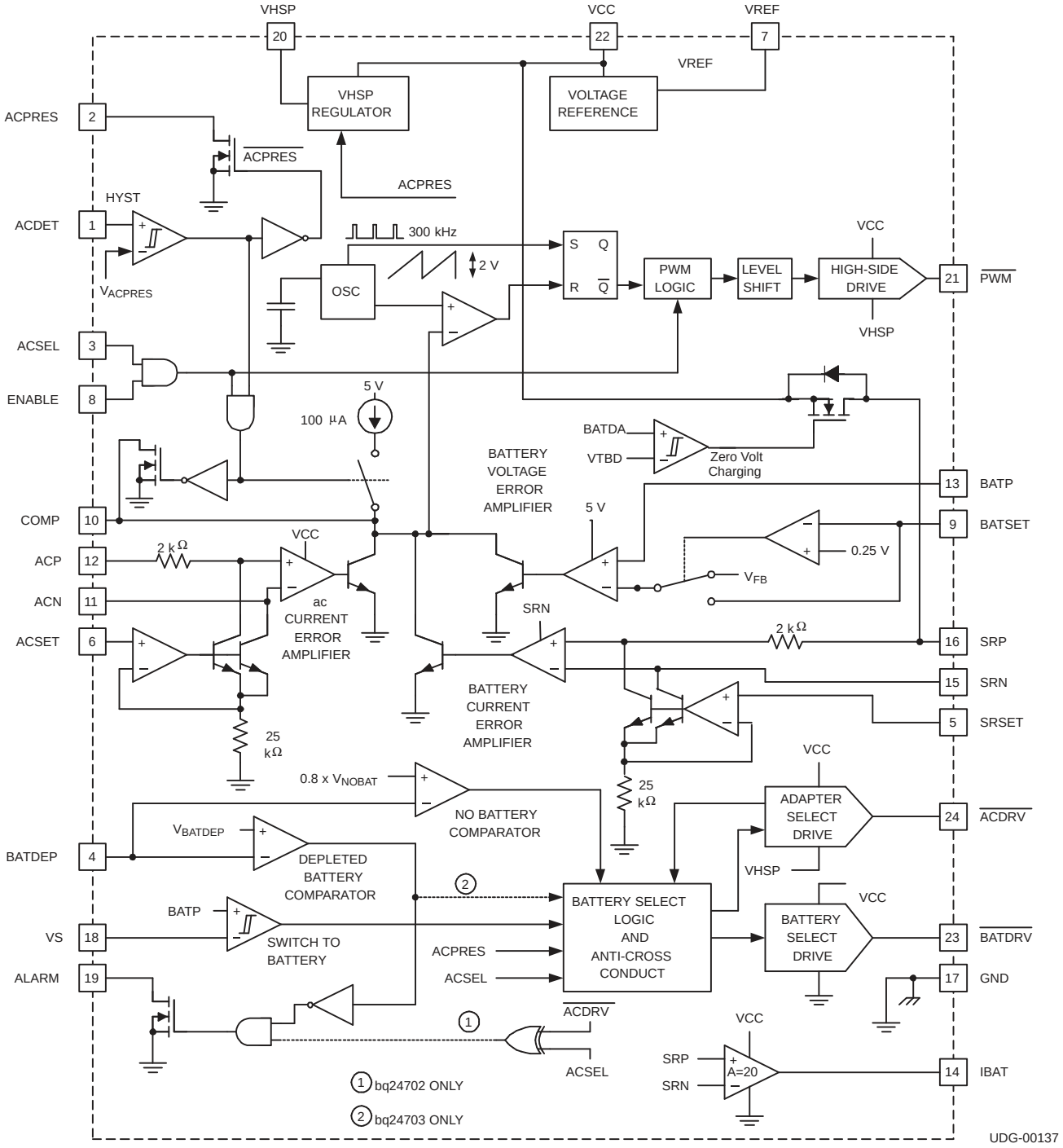


Table 1. TERMINAL FUNCTIONS

TERMINAL			I/O	DESCRIPTION
NAME	bq24702 (PW)	bq24703 (QFN)		
ACDET	1	26	I	AC or adapter power detection
$\overline{\text{ACDRV}}$	24	25	O	AC or adapter power source selection output
ACN	11	8	I	Negative differential input
ACP	12	9	I	Positive differential input
ACPRES	2	27	O	AC power indicator
ACSEL	3	28	I	AC adapter power select
ACSET	6	3	I	Adapter current programming voltage
ALARM	19	19	O	Alarm output
BATDEP	4	1	I	Depleted battery level
$\overline{\text{BATDRV}}$	23	24	O	Battery power source select output
BATP	13	12	I	Battery charge regulation voltage measurement input to the battery-voltage g_m amplifier
BATSET	9	6	I	External override to an internal precision reference
COMP	10	7	O	Inverting input to the PWM comparator
ENABLE	8	5	I	Charge enable
GND	17	17	O	Supply return and ground reference
IBAT	14	13	O	Battery current differential amplifier output
$\overline{\text{PWM}}$	21	21	O	Gate drive output
SRN	15	15	I	Negative differential battery current sense amplifier input
SRP	16	16	I/O	Positive differential battery current sense amplifier input
SRSET	5	2	I	Battery charge current programming voltage
VCC	22	22	I	Operational supply voltage
VHSP	20	20	O	Voltage source to drive gates of the external MOSFETs
VREF	7	4	O	Precision 5-V reference
VS	18	18	I	System (load) voltage input pin

PIN ASSIGNMENTS

ACDET: AC or adapter power detection. This input pin is used to determine the presence of the ac adapter. When the voltage level on the ACDET pin is less than V_{ACPRES}, the bq24702/bq24703 is in sleep mode, the PWM control is disabled, the $\overline{\text{BATDRV}}$ is driven low, and the $\overline{\text{ACDRV}}$ is driven high. This feature can be used to automatically select battery as the system power source.

$\overline{\text{ACDRV}}$: AC or adapter power source select output. This pin drives an external P-channel MOSFET used to switch to the ac wall-adapter as the system power source. When the ACSEL pin is high while the voltage on the ACDET pin is greater than V_{ACPRES}, the output $\overline{\text{ACDRV}}$ pin is driven low (V_{HSP}). This pin is driven high (V_{CC}) when the ACDET is less than V_{ACPRES}.

ACN, ACP: Negative and positive differential inputs, respectively for ac-to-dc adapter current sense resistor.

ACPRES: This open-drain output pin is used to indicate the presence of ac power. A logic high indicates there is a valid ac input. A low indicates the loss of ac power. ACPRES is high when the voltage level on the ACDET pin is greater than V_{ACPRES}.

ACSEL: AC adapter power select. This input selects either the ac adapter or the battery as the power source. A logic high selects ac power, while a logic low selects the battery.

ACSET: Adapter current programming voltage. This input sets the system current level at which dynamic power management occurs. Adapter currents above this programmed level activate the dynamic power management and proportionally reduce the available power to the battery.

ALARM: Depleted battery alarm output. This open-drain pin indicates that a depleted battery condition exists. A pullup on ALARM goes high when the voltage on the BATDEP pin is below V_{ACPRES}. On the bq24702, the ALARM output also activates when the selector inputs do not match the selector state.

BATDEP: Depleted battery level. A voltage divider network from the battery to BATDEP pin is used to set the battery voltage level at which depletion is indicated by the ALARM pin. See ALARM pin for more details. A battery depletion is detected when BATDEP is less than V_{ACPRES}. A no-battery condition is detected when the battery voltage is < 80% of the depleted threshold. In a no-battery condition, the bq24702 automatically selects ac as the input source. If ENABLE = 1, the PWM remains enabled.

$\overline{\text{BATDRV}}$: Battery power source select output. This pin drives an external P-channel MOSFET used to switch the battery as the system's power source. When the voltage level on the ACDET pin is less than V_{ACPRES}, the output of the $\overline{\text{BATDRV}}$ pin is driven low, GND. This pin is driven high (V_{CC}) when ACSEL is high and ACDET > V_{ACPRES}.

BATP: Battery charge regulation voltage measurement input to the battery-voltage g_m amplifier. The voltage on this pin is typically derived from a voltage divider network connected across the battery. In a voltage loop, BATP is regulated to the V_{FB} precision reference of the battery voltage g_m amplifier.

BATSET: An external override to an internal precision reference. When BATSET is > 0.25 V, the voltage level on the BATSET pin sets the voltage charge level. When BATSET ≤ 0.25 V, an internal V_{FB} reference is connected to the inverting input of the battery error amplifier. To ensure proper battery voltage regulation with BATSET, BATSET must be > 1.0 V. Simply ground BATSET to use the internal reference.

COMP: The inverting input to the PWM comparator and output of the g_m amplifiers. A type II compensation network between COMP and GND is recommended.

ENABLE: Charge enable. A high on this input pin allows PWM control operation to enable charging while a low on this pin disables and forces the PWM output to a high state. Battery charging is initiated by asserting a logic 1 on the ENABLE pin.

GND: Supply return and ground reference

IBAT: Battery current differential amplifier output. The output of this pin produces a voltage proportional to the battery charge current. This voltage is suitable for driving an ADC input.

$\overline{\text{PWM}}$: Gate drive output pin drives the P-channel MOSFET for PWM control. The PWM control is active when ACPRES, ACSEL, and ENABLE are high. $\overline{\text{PWM}}$ is driven low to V_{HSP} and high to V_{CC}.

SRN, SRP: Differential amplifier inputs for battery current sense. These pins feed back the battery charge current for PWM control. SRN is tied to the battery terminal. SRP is the source pin for zero volt operation.

SRSET: Battery charge current programmed voltage. The level on this pin sets the battery charge current limit.

VCC: Operational supply voltage.

VHSP: The VHSP pin is connected to a 1-µF capacitor (close to the pin) to provide a stable voltage source to drive the gates of the external MOSFETs. VHSP = VCC – 10 V for VCC > 10.5 V and VHSP = VCC – 0.5 V for VCC <10.5 V. A 13-V Zener diode should be placed between VCC and VHSP to prevent MOSFET overstress during start-up.

VREF: Bypassed precision voltage 5-V output. It can be used to set fixed levels on the inverting inputs of any one of the three error amplifiers if desired. The tight tolerance is suitable for charging lithium-ion batteries.

VS: System (Load) voltage input pin. The voltage on this pin indicates the system voltage in order to insure a break before make transition when changing from ac power to battery power. The battery is protected from an over-voltage condition by disabling the P-channel MOSFET connected to the $\overline{\text{BATDRV}}$ pin if the voltage at VS is greater than BATP. This function can be eliminated by grounding the VS pin.

APPLICATION INFORMATION

PROGRAMMING THE THRESHOLDS

The input-referenced thresholds for battery depleted, ac detection and charge voltage are defined by dimensioning the external dividers connected to pins BATDEP, ACDET and BATP. This calculation is simple, and consists of assuming that when the input voltage equals the desired threshold value the voltage at the related pin is equal to the pin internal reference voltage:

Vinput = Vpin × (1 + Kres)

where:

Vinput = Target threshold, referenced to input signal

Vpin = Internal reference(1.196 V for BATP; 1.246 V for BATDEP, ACDET)

Kres = External resistive divider gain (for instance: R24/R25 for BATP)

When using external dividers with high absolute value the input bias currents for those pins must be included in the threshold calculation. On the bq24702/3 the input bias currents increase the actual value for the threshold voltage, when compared to the values calculated using the internal references and divider gain only:

Vinput = Vpin × (1+Kres) + Vbias

The increase on the threshold voltage is given by:

Vbias = Rdiv × Ipin

where:

Vbias = Voltage increase due to pin bias current

Rdiv = External resistor value for resistor connected from pin to input voltage

Ipin = Maximum pin leakage current

The effect of IB can be reduced if the resistor values are decreased.

DYNAMIC POWER MANAGEMENT

The dynamic power management (DPM) feature allows a cost effective choice of an ac wall-adapter that accommodates 90% of the system's operating-current requirements. It minimizes battery charge time by allocating available power to charge the battery (i.e. $I_{BAT} = I_{ADPT} – I_{SYS}$). If the system plus battery charge current exceeds the adapter current limit, as shown in Figure 1, the DPM feature reduces the battery charge current to maintain an overall input current consumption within user defined power capability of the wall-adapter. As the system's current requirements decrease, additional current can be directed to the battery, thereby increasing battery charge current and minimizing battery charge time.

The DPM feature is inherently designed into the PWM controller by inclusion of the three control loops, battery-charge regulation voltage, battery-charge current, and adapter-charge current, refer to Figure 2. If any of the three user programmed limits are reached, the corresponding control loop commands the PWM controller to reduce duty cycle, thereby reducing the battery charge current.

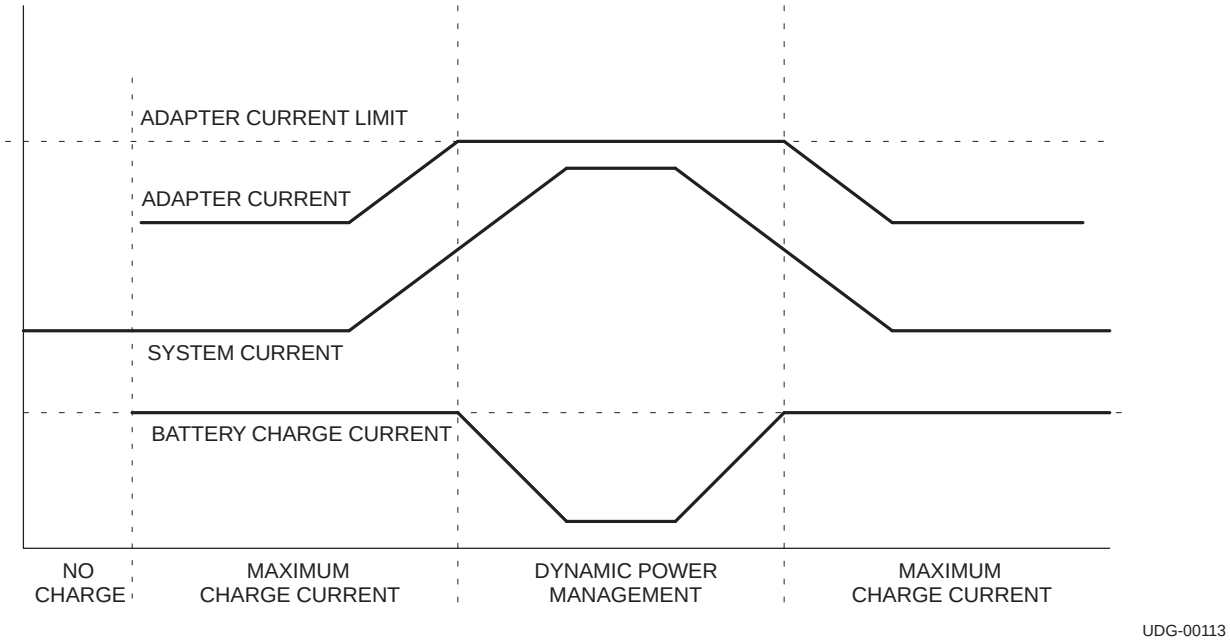


Figure 1. Dynamic Power Management

ACDET OPERATION

The ACDET function senses the loss of adequate adapter power. If the voltage on ACDET drops below the internal V_{ACPRES} reference voltage, a loss of ADAPTER power is declared and the bq24702/bq24703 switches to battery power as the main system power. In addition, the bq24702/bq24703 shuts down its 5-V VREF and enters a low power sleep mode.

BATTERY CHARGER OPERATION

The bq24702/bq24703 fixed-frequency, PWM controller is designed to provide closed-loop control of battery charge-current (I_{CH}) based on three parameters, battery-float voltage (V_{BAT}), battery-charge current, and adapter charge current (I_{ADPT}). The bq24702/bq24703 is designed primarily for control of a buck converter using a high side P-channel MOSFET device (SW, refer to Figure 2).

The three control parameters are voltage programmable through resistor dividers from the bq24702/bq24703 precision 5-V reference, an external or internal precision reference, or directly via a DAC interface from a keyboard controller.

Adapter and battery-charge current information is sensed and fed back to two transconductance (g_m) amplifiers via low-value-sense resistors in series with the adapter and battery respectively. Battery voltage information is sensed through an external resistor divider and fed back from the battery to a third g_m amplifier.

PRECHARGE OPERATION

The precharge operation must be performed using the PWM regulator. The host can set the precharge current externally by monitoring the ALARM pin to detect a battery depleted condition and programming SRSET voltage to obtain the desired precharge current level.

ZERO VOLT OPERATING

The zero volt operation is intended to provide a low current path to close open packs and protect the system in the event of a pack cell short-circuit condition or if a short is applied to the pack terminal. It is not designed to precharge depleted packs, as it is disabled at voltages that are not within normal pack operating range for precharge.

If the voltage at BATDEP pin is below the zero volt operation threshold , charge is enabled (EN=HI), and ac is selected (ACSEL=HI) the bq24702/3 enters the zero volt operation mode. When the zero volt operation mode is on, the internal PWM is disabled, and an internal power MOSFET connects SRP to V_{CC}. The battery charge current is limited by the filter resistor connected to SRP pin (R19). R19 must be dimensioned to withstand the worst case power dissipation when in zero volt operation mode.

The zero volt operation mode is disabled when BATDEP is above the zero volt operation threshold, and the main PWM loop is turned on if charge is enabled, regulating the current to the value set by SRSET voltage. To avoid errors on the charge current both resistors on the SRP, SRN filter must have the same value. Note, however, that R21 (connected to SRN) does not dissipate any power when in zero volt operation and can be of minimum size.

PWM OPERATION

The three open collector g_m amplifiers are tied to the COMP pin (refer to Figure 2), which is internally biased up by a 100-µA constant current source. The voltage on the COMP pin is the control voltage (V_C) for the PWM comparator. The PWM comparator compares V_C to the sawtooth ramp of the internally fixed 300-kHz oscillator to provide duty cycle information for the PWM drive. The PWM drive is level-shifted to provide adequate gate voltage levels for the external P-channel MOSFET. Refer to *PWM selector switch gate drive* section for gate drive voltage levels.

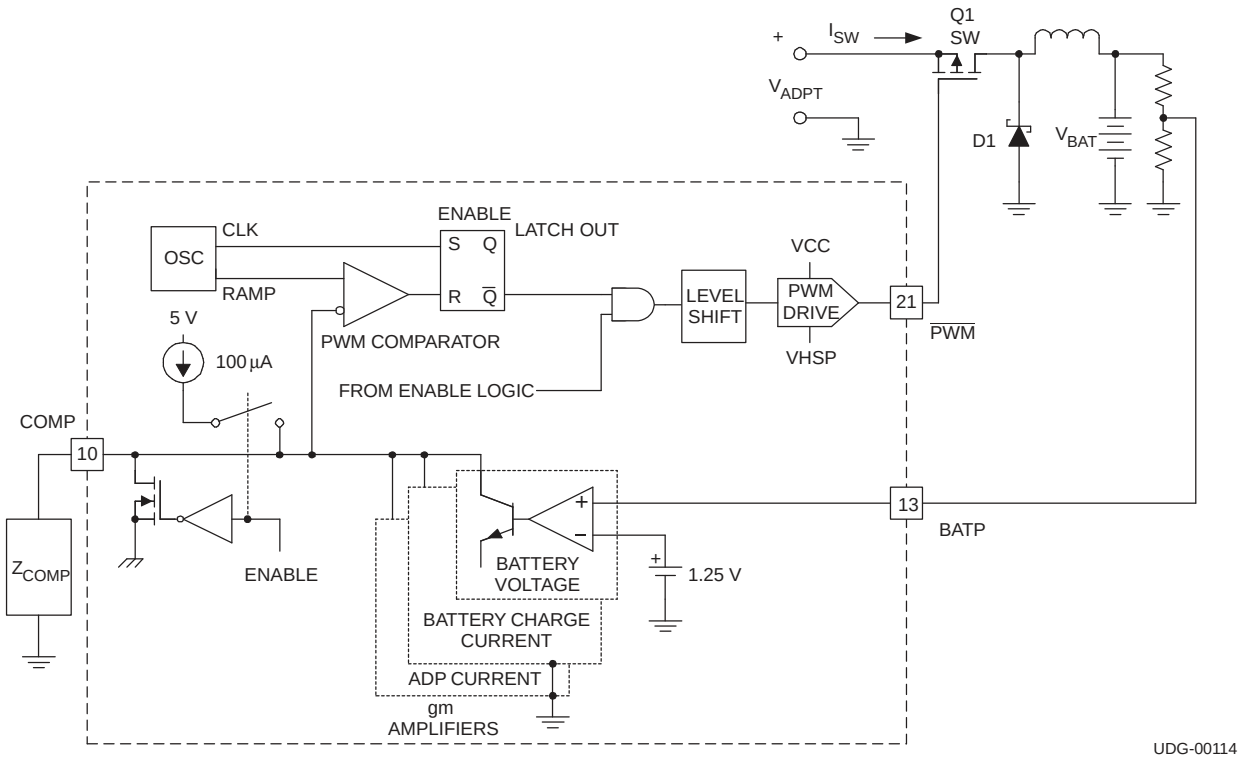


Figure 2. PWM Controller Block Diagram

SOFTSTART

Softstart is provided to ensure an orderly start-up when the PWM is enabled. When the PWM controller is disabled (ENABLE = Low), the 100-µA current source pullup is disabled and the COMP pin is actively pulled down to GND. Disabling the 100-µA pullup reduces current drain when the PWM is disabled. When the bq24702/bq24703 $\overline{\text{PWM}}$ is enabled (ENABLE = High), the COMP pin is released and the 100-µA pullup is enabled (refer to Figure 2). The voltage on the COMP pin increases as the pullup charges the external compensation network connected to the COMP pin. As the voltage on the COMP pin increases the PWM duty cycle increases linearly as shown in Figure 3.

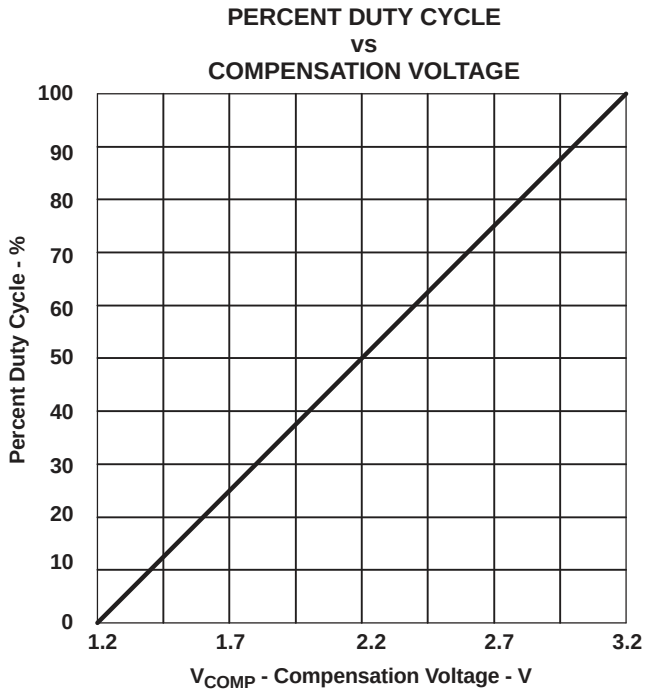


Figure 3.

As any one of the three controlling loops approaches the programmed limit, the g_m amplifier begins to shunt current away from the COMP pin. The rate of voltage rise on the COMP pin slows due to the decrease in total current out of the pin, decreasing the rate of duty cycle increase. When the loop has reached the programmed limit the g_m amplifier shunts the entire bias current (100 µA) and the duty cycle remains fixed. If any of the control parameters tries to exceed the programmed limit, the g_m amplifier shunts additional current from the COMP pin, further reducing the PWM duty cycle until the offending parameter is brought into check.

SETTING THE BATTERY CHARGE REGULATION VOLTAGE

The battery charge regulation voltage is programmed through the BATSET pin, if the internal precision reference is not used. The BATSET input is a high-impedance input that is driven by either a keyboard controller DAC or via a resistor divider from a precision reference (see Figure 4).

The battery voltage is fed back to the g_m amplifier through a resistor divider network. The battery charge regulation voltage can be defined as:

$$V_{BATTERY} = \frac{(R1 + R2) \times V_{BATSET}}{R2} \; V \; + \; I_{BATP} \times R1 \tag{1}$$

where I_{BATP} = input bias current for pin BATP

The overall accuracy of the battery charge regulation voltage is a function of the bypassed 5-V reference voltage tolerance as well as the tolerances on R1 and R2. The precision voltage reference has a 0.5% tolerance making it suitable for the tight battery voltage requirements of Li-ion batteries. Tolerance resistors of 0.1% are recommended for R1 and R2 as well as any resistors used to set BATSET.

The bq24702/bq24703 provides the capability of using an internal precision voltage reference through the use of a multiplexing scheme, refer to Figure 4, on the BATSET pin. When BATSET voltage is less than 0.25 V, an internal reference is switched in and the BATSET pin is switched out from the g_m amplifier input. When the BATSET voltage is greater than 0.25 V, the BATSET pin voltage is switched in to the input of the g_m amplifier and the voltage reference is switched out.

NOTE:

The minimum recommended BATSET is 1.0 V, if BATSET is used to set the voltage loop.

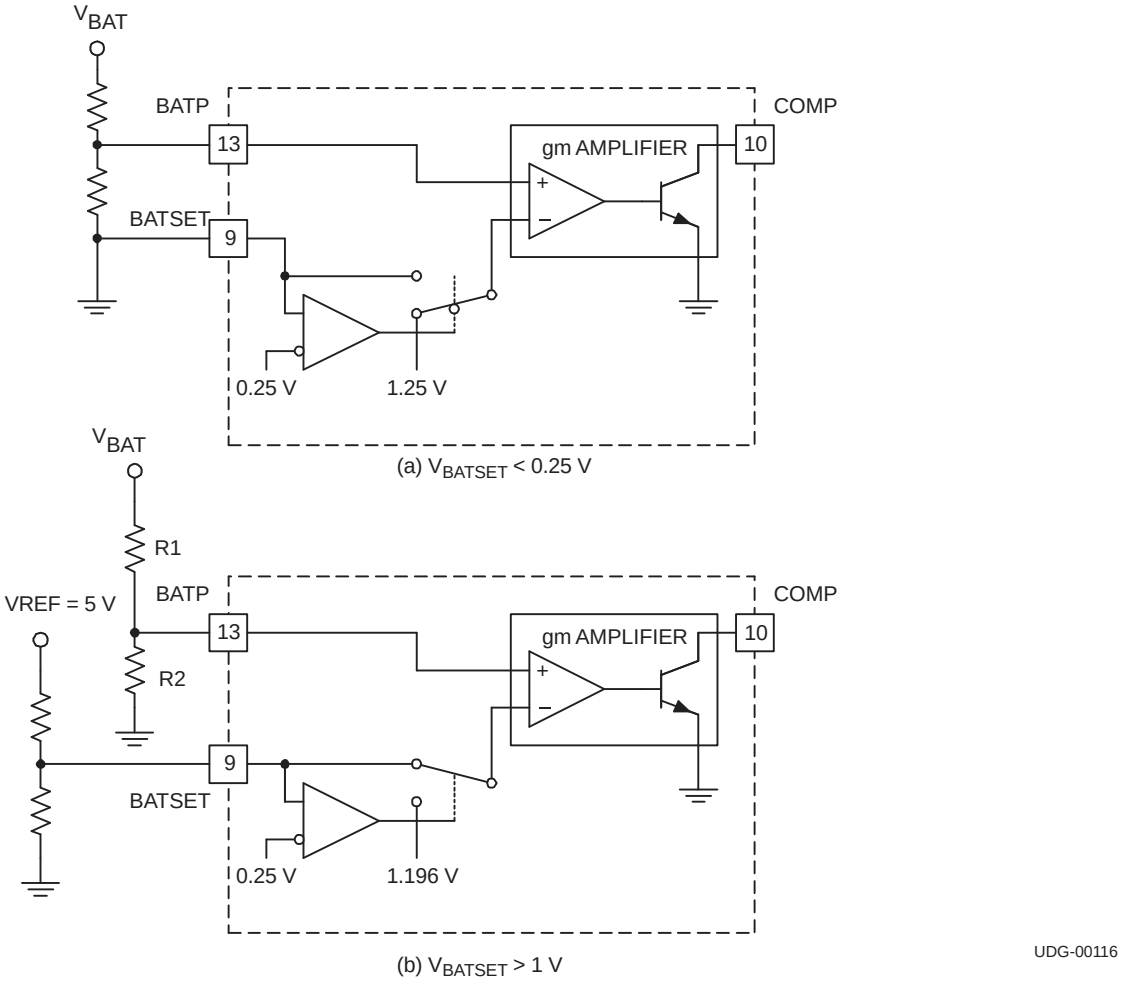


Figure 4. Battery Error Amplifier Input Multiplexing Scheme

PROGRAMMING THE BATTERY CHARGE CURRENT

The battery charge current is programmed via a voltage on the SRSET pin. This voltage can be derived from a resistor divider from the 5-V VREF or by means of an DAC. The voltage is converted to a current source that is used to develop a voltage drop across an internal offset resistor at one input of the SR $g_m$amplifier. The charge current is then a function of this voltage drop and the sense resistor (R_S), refer to Figure 5.

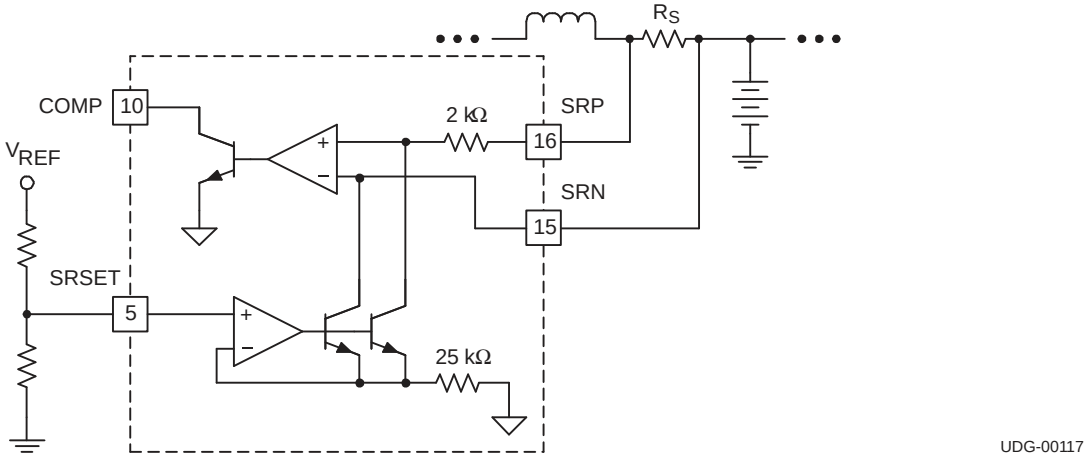


Figure 5. Battery Charge Current Input Threshold Function

The battery charge current can be defined as:

$$I_{BAT} = \frac{V_{SRSET}}{25 \times R_S} \quad (2)$$

where V_{SRSET} is the programming voltage on the SRSET pin. V_{SRSET} maximum is 2.5 V.

PROGRAMMING THE ADAPTER CURRENT

Like the battery charge current described previously, the adapter current is programmed via a voltage on the ACSET pin. That voltage can either be from an external resistor divider from the 5-V VREF or from an external DAC. The adapter current is defined as:

$$I_{ADPT} = \frac{V_{ACSET}}{25 \times R_{S2}} \quad (3)$$

COMPONENT SELECTION

MOSFET Selection

MOSFET selection depends on several factors, namely, gate-source voltage, input voltage, and input current. The MOSFET must be a P-channel device capable of handling at least 15-V gate-to-source with a drain-source breakdown of V_{BV}~ V_{IN}+1 V. The average input current can be approximated by:

$$I_{IN}(avg) = D \times Ichg \quad A$$

D = Duty cycle

Ichg = Charge current (4)

The RMS current through the MOSFET is defined as:

$$I_{IN}(RMS) = Ichg \times \sqrt{D} \quad A_{RMS} \tag{5}$$

The rise/fall times for pin $\overline{PWM}$ for the selected MOSFET should be greater than 40 nsec.

Schottky Rectifier (Freewheeling)

The freewheeling Schottky rectifier must also be selected to withstand the input voltage, V_{IN}. The average current can be approximated from:

$$I_{D1}(avg) = Ichg \times (1 - D) \quad A \tag{6}$$

Choosing an Inductance

Low inductance values result in a steep current ramp or slope. Steeper current slopes result in the converter operating in the discontinuous mode at a higher power level. Steeper current slopes also result in higher output ripple current, which may require a higher number or more expensive capacitors to filter the higher ripple current.

In addition, the higher ripple current results in an error in the sensed battery current particularly at lower charging currents. It is recommended that the ripple current not exceed 20% to 30% of full scale dc current.

$$L = \frac{D \times \left(V_{IN} - V_{BAT}\right)}{F_S \times Ichg \times Ripple}$$

Ripple = % Ripple allowed (Ex.: 0,2 for 20% ripple) (7)

Too large an inductor value results in the current waveform of Q1 and D1 in Figure 2 approximating a squarewave with an almost flat current slope on the step. In this case, the inductor is usually much larger than necessary, which may result in an efficiency loss (higher DCR) and an area penalty.

Selecting an Output Capacitor

For this application the output capacitor is used primarily to shunt the output ripple current away from the battery. The output capacitor should be sized to handle the full output ripple current as defined as:

$$I_C\,(RMS) = \frac{\left(V_{IN} - V_{BAT}\right) \times D}{F_S \times L} \quad A_{RMS} \tag{8}$$

Selecting an Input Capacitor

The input capacitor is used to shunt the converter ripple current on the input lines. The capacitor(s) must have a ripple current (RMS) rating of:

$$I_{RMS} = \sqrt{[Ichg \times (1–D)]^2 \times D + [Ichg \times D]^2 \times (1–D)} \quad A_{RMS} \tag{9}$$

In addition to shunting the converter input ripple when the PWM is operating, the input capacitor also acts as part of an LC filter, where the inductance component is defined by the ac adapter cable inductance and board trace inductance from adapter connector to filter capacitor. Overshoot conditions can be observed at V_{CC} line during fast load transients when the adapter powers the load or when the adapter is hot-plugged .

Increasing the input capacitor value decreases the overshoot at V_{CC}. Avoid overshoot voltages at V_{CC} in excess of the absolute maximum ratings for that pin.

Compensating the Loop

For the bq24702/bq24703 used as a buck converter, the best method of compensation is to use a Type II compensation network from the output of the transconductance amplifiers (COMP pin) to ground (GND) as shown in Figure 2. A Type II compensation adds a pole-zero pair and an additional pole at dc.

The Type II compensation network places a zero at

$$F_Z = \frac{1}{2} \times \left(\frac{1}{\pi \times R_{COMP} \times C_Z} \right) \text{ Hz} \tag{10}$$

and a pole at

$$F_P = \frac{1}{2} \times \left(\frac{1}{\pi \times R_{COMP} \times C_P} \right) \text{ Hz} \tag{11}$$

For this battery charger application the following component values: C_Z = 4.7 µF, C_P = 150 pF, and R_{COMP} = 100 Ω, provides a closed loop response with more than sufficient phase margin, as long as the LC pole [1/2 × PI × sqrt (l×c)] is set below 10 kHz. The SRP/SRN filter (R19, R21, C8) and ACP/ACN filter (R13/R15/C3) are required to filter noise associated with the PWM switching. To avoid adding secondary poles to the PWM closed loop system those filters should be set with cutoff frequencies higher than 1 kHz.

SELECTOR OPERATION

The bq24702/bq24703 allows the host controller to manually select the battery as the system's main power source, without having to remove adapter power. This allows battery conditioning through smart battery learn cycles. In addition, the bq24702/bq24703 supports autonomous supply selection during fault conditions on either supply. The selector function uses low $R_{DS(on)}$ P-channel MOSFETs for reduced voltage drops and longer battery run times.

NOTE:

Selection of battery power whether manual or automatic results in the suspension of battery charging.

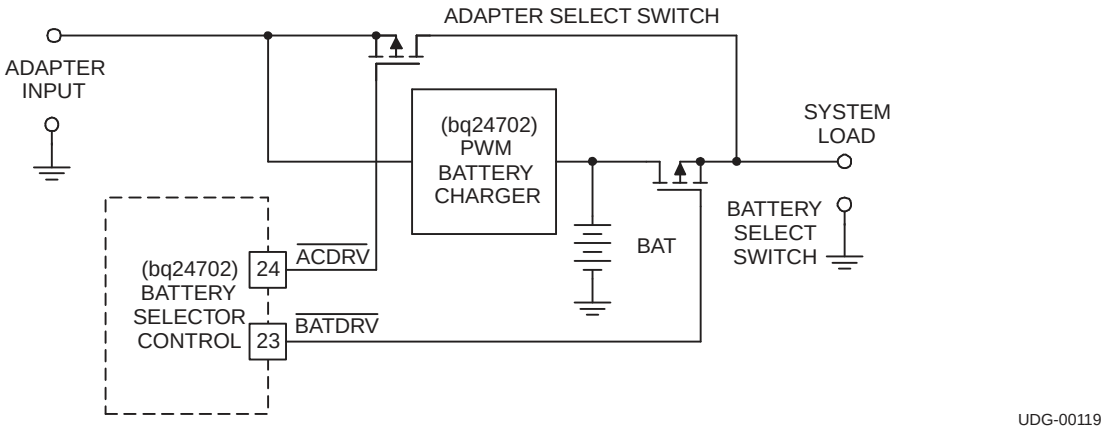


Figure 6. Selector Control Switches

AUTONOMOUS SELECTION OPERATION

Adapter voltage information is sensed at the ACDET pin via a resistor divider from the adapter input. The voltage on the ACDET pin is compared to an internally fixed threshold. An ACDET voltage less than the set threshold is considered as a loss of adapter power regardless of the actual voltage at the adapter input. Information concerning the status of adapter power is fed back to the host controller through ACPRES. The presence of adapter power is indicated by ACPRES being set high. A loss of adapter power is indicated by ACPRES going low regardless of which power source is powering the system. During a loss of adapter power, the bq24702/bq24703 obtains operating power from the battery through the body diode of the P-channel battery select MOSFET. Under a loss of adapter power, ACPRES (normally high) goes low, if adapter power is selected to power the system, the bq24702/bq24703 automatically switches over to battery power by commanding $\overline{\text{ACDRV}}$ high and $\overline{\text{BATDRV}}$ low. During the switch transition period, battery power is supplied to the load via the body diode of the battery select P-channel MOSFET. When adapter power is restored, the bq24702/bq24703 configures the selector switches according to the state of signals; ACSEL, and ACPRES. If the ACSEL pin is left high when ac power is restored, the bq24702/bq24703 automatically switches back to ac power. To remain on battery power after ac power is restored, the ACSEL pin must be brought low.

Conversely, if the battery is removed while the system is running on battery power and adapter power is present, the bq24702/bq24703 automatically switches over to adapter power by commanding $\overline{\text{BATDRV}}$ high and $\overline{\text{ACDRV}}$ low.

NOTE:

For the bq24702 any fault condition that results in the selector MOSFET switches not matching their programmed states is indicated by the ALARM pin momentarily going high. Refer to Battery Depletion Detection Section for more information on the ALARM discrete.

When switching between the ac adapter and battery the internal logic monitors the voltage at pins $\overline{\text{ACDRV}}$ and $\overline{\text{BATDRV}}$ to implement a break-before-make function, with typical dead time on the order of 150 nsec.

The turnon times for the external ac/battery switches can be increased to minimize inrush peak currents; that can be accomplished by adding external resistors in series with the MOSFET gates (R18 and R26). Note, however, that adding those resistors effectively disables the internal break-before-make function for ac/battery-switches, as the MOSFET gate voltages can not be monitored directly. If external resistors are added to increase the rise/fall times for battery/ac switches the break-before-make has to be implemented with discrete external components, to avoid shoot-through currents between ac adapter and battery pack. This functionality can be implemented by adding diodes (D2/D9) that bypass the external resistors when turning off the external FETs.

SMART LEARN CYCLES WHEN ADAPTER POWER IS PRESENT

Smart learn cycles can be conducted when adapter power is present by asserting and maintaining the ACSEL pin low. The adapter power can be reselected at the end of the learn cycle by a setting ACSEL to a logic high, provided that adapter power is present. Battery charging is suspended while selected as the system power source.

NOTE:

On the bq24703 the ac adapter is switched to the load when the battery voltage reaches the battery depleted threshold; it can be used when the learn cycle does not require the battery voltage to go below the battery depleted threshold. If the learn cycle algorithm requires the battery voltage to go lower than the battery depleted voltage, the bq24702 should be used, as it does not switch the ac adapter to load upon battery depleted detection.

SYSTEM BREAK BEFORE MAKE FUNCTION

When selecting the battery as the system primary power source, the adapter power select MOSFET turns off, in a *break-before-make* fashion, before the battery select MOSFET turns on. To ensure that this happens under all load conditions, the system voltage (load voltage) can be monitored through a resistor divider on the VS pin. This function provides protection against switching over to battery power if the adapter selector switch were shorted and adapter power present. Setting the VS resistive divider gain with the same gain selected for the BATP resistive divider assures the battery switch is turned on only when the system voltage is equal or less than the battery voltage. This function can be eliminated by grounding the VS pin.

The ACDET function senses the adapter voltage via a resistive divider (refer to application circuit).The divider can be connected either to the anode of the input blocking diode (directly to the adapter supply) or to the cathode of the input blocking diode (bq24702/3 VCC pin). When the divider is connected to the adapter supply, the adapter power removal is immediately identified and the sleep mode is entered, disabling the break-before-make function for system voltage (see section for system power switching) and coupling system voltage to the battery line. In normal operation with a battery present, the battery low impedance prevents any over-voltage conditions. However, if a pack is not present or the pack is open, the battery line voltage has a transient equal to the adapter voltage. The bq24703 SRP/SRN pins are designed to withstand this over-voltage condition, but avoid connection to the battery line of any external devices that are not rated to withstand the adapter voltage.

Connecting the ACDET resistive divider input to the VCC node keeps the system break-before-make function enabled until the voltage at pin VS is lower than the voltage at pin BATP. However, note that when using this topology the VCC pin voltage can be held by capacitive loads at either the VCC or system (ac switch is on) nodes when the ac adapter is removed. As the ACDET divider is connected to the VCC line there is a time delay from ac adapter removal to ac adapter removal detection by the IC. This time is dependent on load conditions and capacitive load values at VCC and system lines.

BATTERY DEPLETION DETECTION

The bq24702/bq24703 provides the host controller with a battery depletion discrete, the ALARM pin, to alert the host when a depleted battery condition occurs. The battery depletion level is set by the voltage applied to the BATDEP pin through a voltage divider network. The ALARM output asserts high and remains high as long as the battery deplete condition exists, regardless of the power source selected.

For the bq24702, the host controller must take appropriate action during a battery deplete condition to select the proper power source. The bq24702 remains on the selected power source. The bq24703, however, automatically reverts over to adapter power, provided the adapter is present, during a deep discharge state. The battery is considered as being in a deep discharge state when the battery voltage is less than (0.8 $\times$ depleted level).

Feature sets for the bq24702 and bq24703 are detailed in the Available Options table.

SELECTOR/ALARM TIMING EXAMPLE

The selector and ALARM timing example in Figure 7 illustrates the battery conditioning support.

NOTE:

For manual selection of wall power as the main power source, both the ACPRES and ACSEL signals must be a logic high.

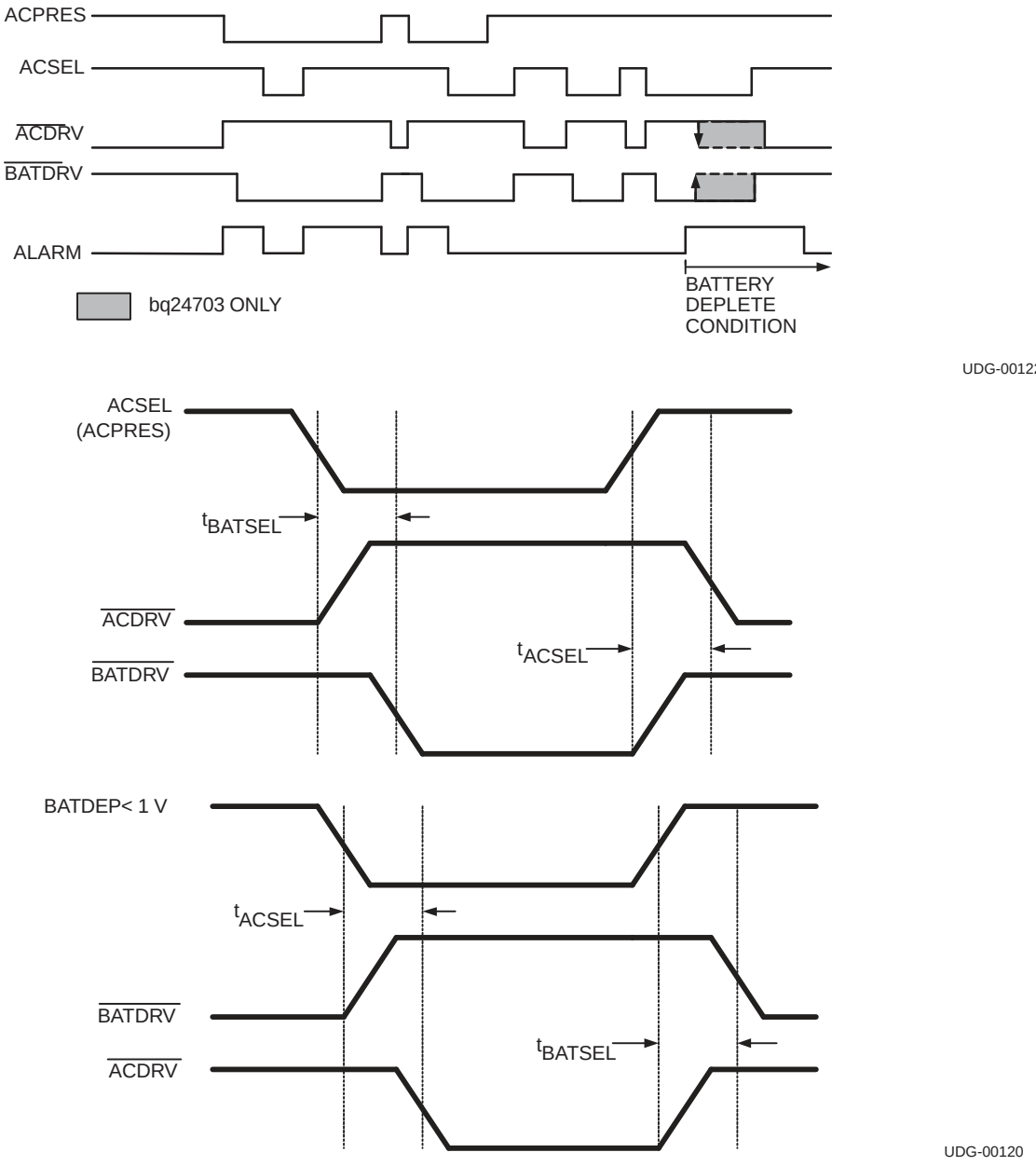


Figure 7. Battery Selector and ALARM Timing Diagram

PWM SELECTOR SWITCH GATE DRIVE

Because the external P-channel MOSFETs (as well as the internal MOSFETs) have a maximum gate-source voltage limitation of the input voltage, VCC, cannot be used directly to drive the MOSFET gate under all input conditions. To provide safe MOSFET-gate-drive at input voltages of less than an intermediate gate drive voltage rail was established (VSHP). Where V_{HSP} = VCC – 10 V. This ensures adequate enhancement voltage across all operating conditions.

An external zener diode (D3) connected between VCC and VHSP is required for transient protection; its breakdown voltage should be above the maximum value for internal VHSP/VCC clamp voltage for all operating conditions.

TRANSIENT CONDITIONS AT SYSTEM, OVER-VOLTAGE AT SYSTEM TERMINAL

Overshoot conditions can be observed at the system terminal due to fast load transients and inductive characteristics of the system terminal to load connection. An overshoot at the system terminal can be directly coupled to the VCC and VBAT nodes, depending on the switch mode of operation. If the capacitors at VBAT and VCC can not reduce this overshoot to values below the absolute maximum ratings, it is recommended that an additional capacitor is added to the system terminal to avoid damage to IC or external components due to voltage overstress under those transient conditions.

AC ADAPTER COLLAPSING DUE TO TRANSIENT CONDITIONS

The ac adapter voltage collapses when the ac switch is on and a current load transient at the system exceeds the adapter current limit protection. Under those conditions the ac switch is turned off when the ac adapter voltage falls below the ac adapter detection threshold. If the system terminal to load impedance has an inductive characteristic, a negative voltage spike can be generated at the system terminal and coupled into the battery line via the battery switch backgate diode.

In normal operation, with a battery present, this is not an issue, as the low battery impedance holds the voltage at battery line. However, if a battery is not present or the pack protector switches are open the negative spike at the system terminal is directly coupled to the SRP/SRN pins via the R19/R21 resistors.

Avoid damage to the SRP/SRN pins if this transient condition happens in the application. If a negative voltage spike happens at system terminal and R19/R21 limit the current sourced from the pin to less than –50 mA (Ipin = Vsystem/R19), the pins SRP/SRN are not damaged and the external protection schottky diodes are not required. However, if the current under those transient conditions exceeds –50 mA, external schottky diodes must be added to clamp the voltage at pins SRP/SRN so they do not exceed the absolute maximum ratings specified (-0.3 V).

IBAT AMPLIFIER

A filter with a cutoff frequency smaller than 10 kHz should be added to the IBAT output to remove switching noise.

POWER DISSIPATION CALCULATION

During PWM operation, the power dissipated internally to the IC increases as the internal driver is switching the PWM FET on/off. The power dissipation figures are dependent on the external FET used, and can be calculated using the following equation:

$$Pd(max) = [IDDOP + Qg \times Fs(max)] \times VADAP$$

where:

Qg = Total gate charge for selected PWM MOSFET

IDDOP = Maximum quiescent current for IC

VADAP = Maximum adapter voltage

Fs(max) = Maximum PWM switching frequency

The maximum junction temperature for the IC must be limited to 125°C, under worst case conditions.

TYPICAL CHARACTERISTICS

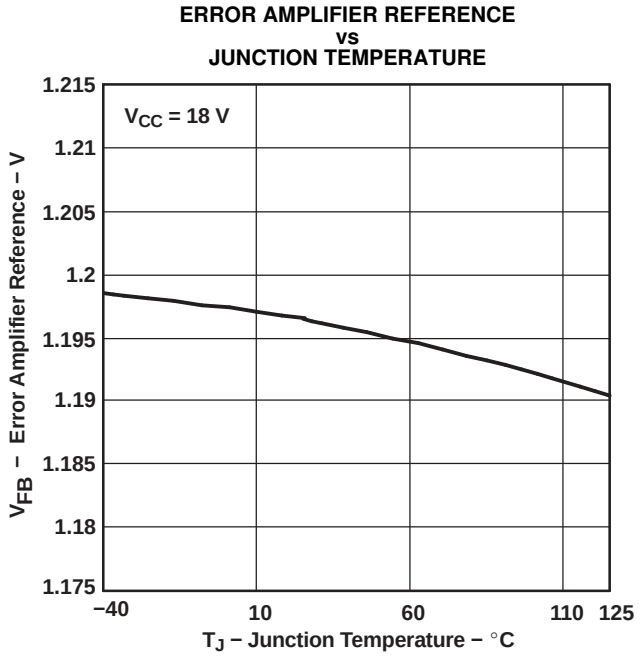


Figure 8.

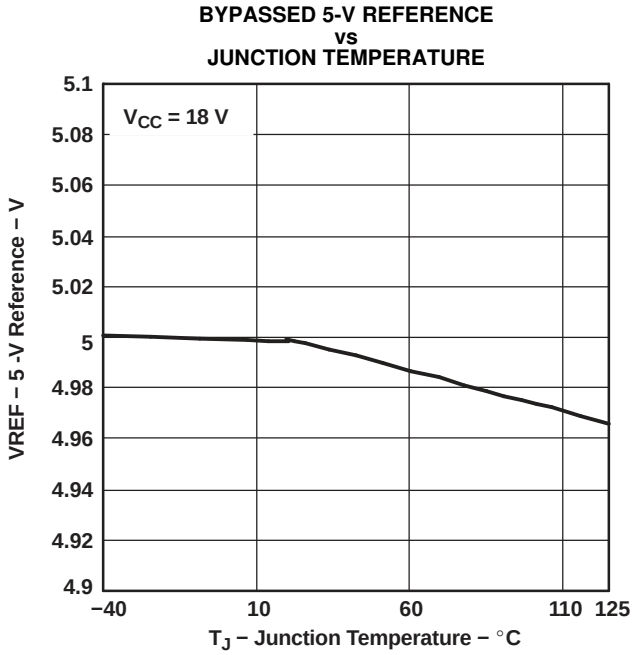


Figure 9.

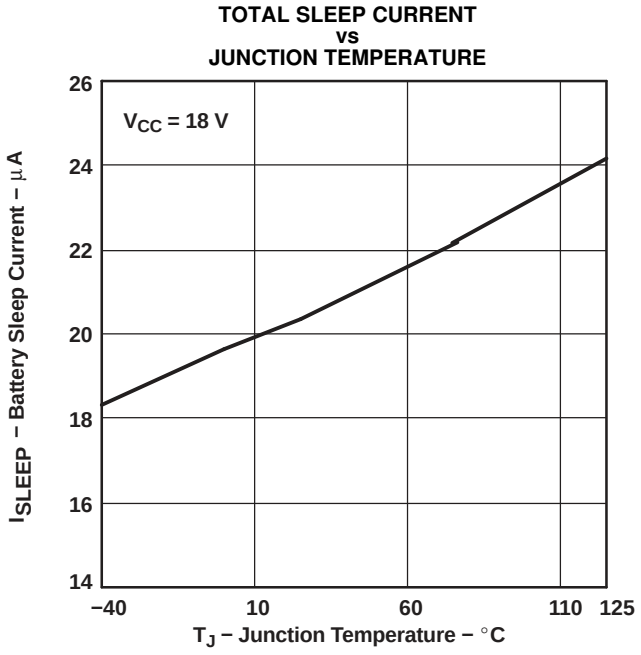


Figure 10.

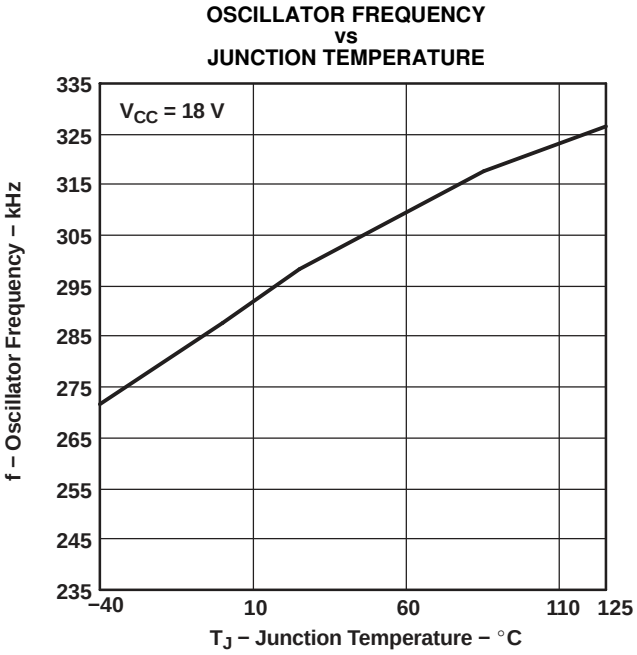


Figure 11.

TYPICAL CHARACTERISTICS (continued)

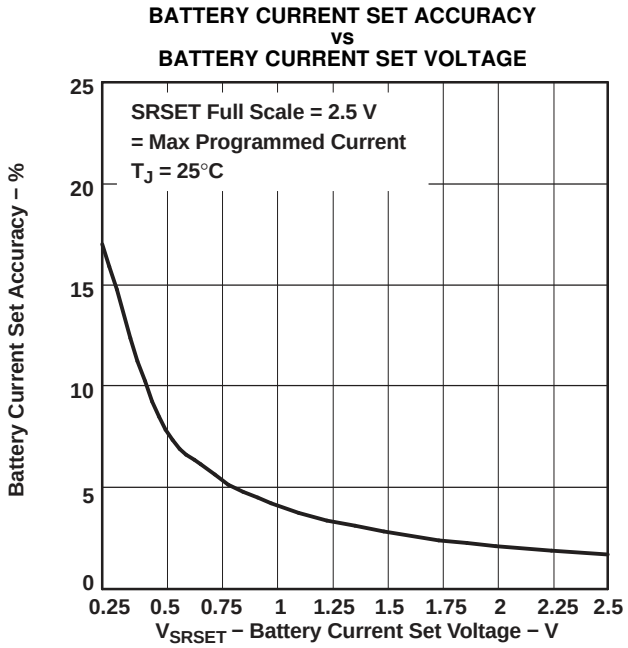


Figure 12.

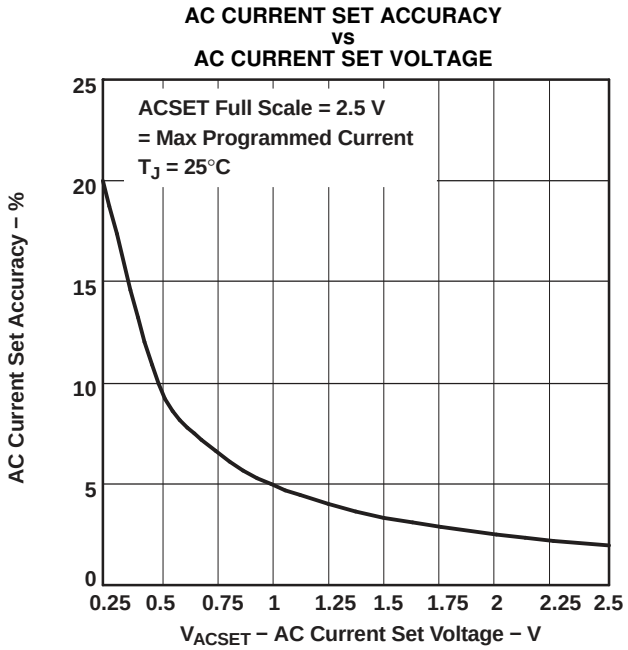


Figure 13.

BOARD LAYOUT GUIDELINES

Recommended Board Layout

Follow these guidelines when implementing the board layout:

1. Do not place lines and components dedicated to battery/adapter voltage sensing (ACDET,BATDEP, VS), voltage feedback loop (BATP, BATSET if external reference is used) and shunt voltage sensing (SRP/SRN/ACP/ACN) close to lines that have signals with high dv/dt (PWM, BATDRV, ACDRV, VHSP) to avoid noise coupling.
2. Add filter capacitors for SRP/SRN (C8) and ACP/ACN (C3) close to IC pins
3. Add Reference filter capacitor C1 close to IC pins
4. Use an isolated, clean ground for IC ground pin and resistive dividers used in voltage sensing; use an isolated power ground for PWM filter cap and diode (C11/D4). Connect the grounds to the battery PACK- and adapter GND.
5. Place C7 close to VCC pin.
6. Place input capacitor C12 close to PWM switch (U3) source and R14.
7. Position ac switch (U2) to minimize trace length from ac switch source to input capacitor C12.
8. Minimize inductance of trace connecting PWM pin and PWM external switch U3 gate
9. Maximize power dissipation planes connected to PWM switch
10. Maximize power dissipation planes connected to SRP resistor if steady state in zero volt mode is possible
11. Maximize power dissipation planes connected to D1

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ24702PW	ACTIVE	TSSOP	PW	24	60	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	24702PW	Samples
BQ24702PWG4	ACTIVE	TSSOP	PW	24	60	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	24702PW	Samples
BQ24702PWR	ACTIVE	TSSOP	PW	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	24702PW	Samples
BQ24703PW	ACTIVE	TSSOP	PW	24	60	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	24703PW	Samples
BQ24703PWR	ACTIVE	TSSOP	PW	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	24703PW	Samples
BQ24703RHDR	ACTIVE	VQFN	RHD	28	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	24703	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

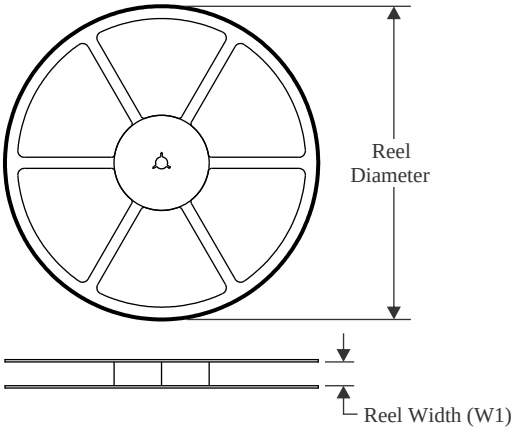
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

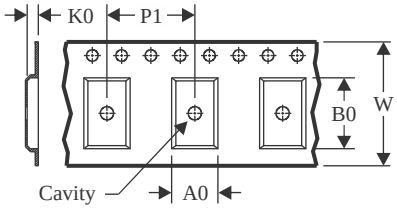
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

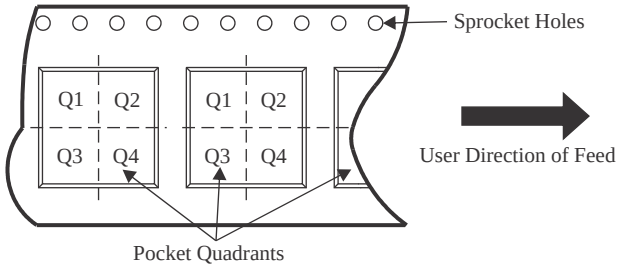


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

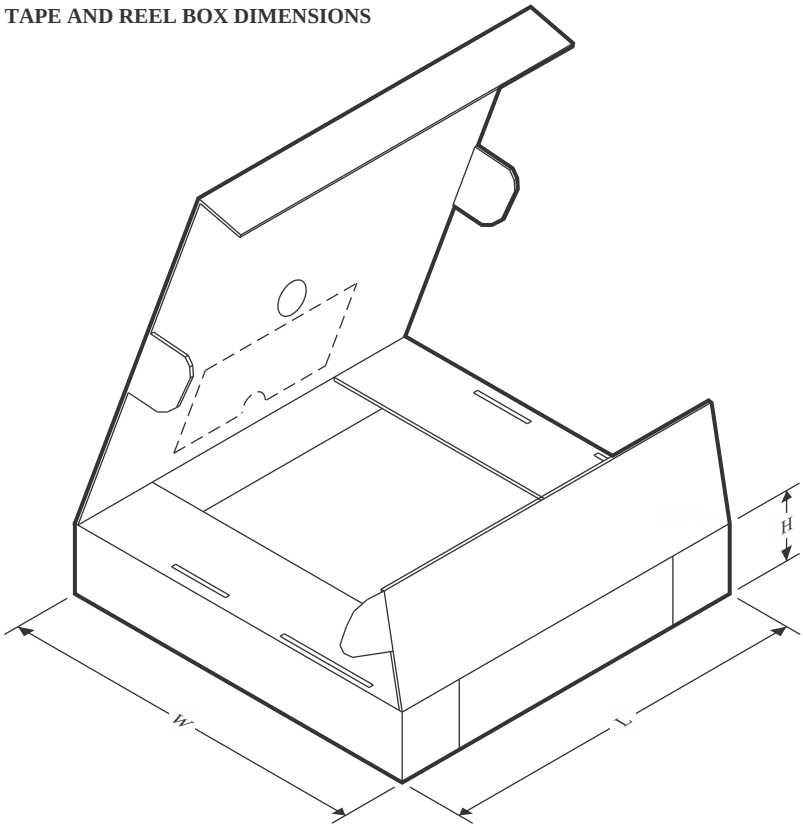
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ24702PWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
BQ24703PWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
BQ24703RHDR	VQFN	RHD	28	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2

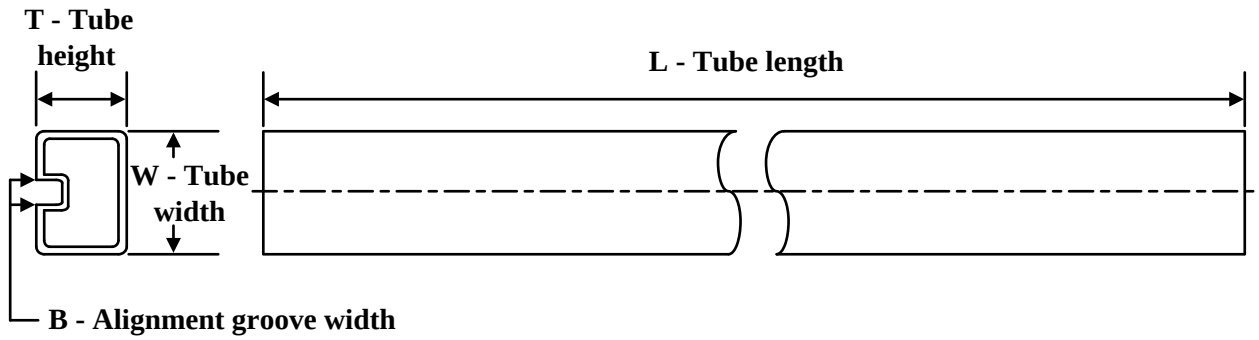
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ24702PWR	TSSOP	PW	24	2000	356.0	356.0	35.0
BQ24703PWR	TSSOP	PW	24	2000	356.0	356.0	35.0
BQ24703RHDR	VQFN	RHD	28	3000	367.0	367.0	35.0

TUBE



*All dimensions are nominal

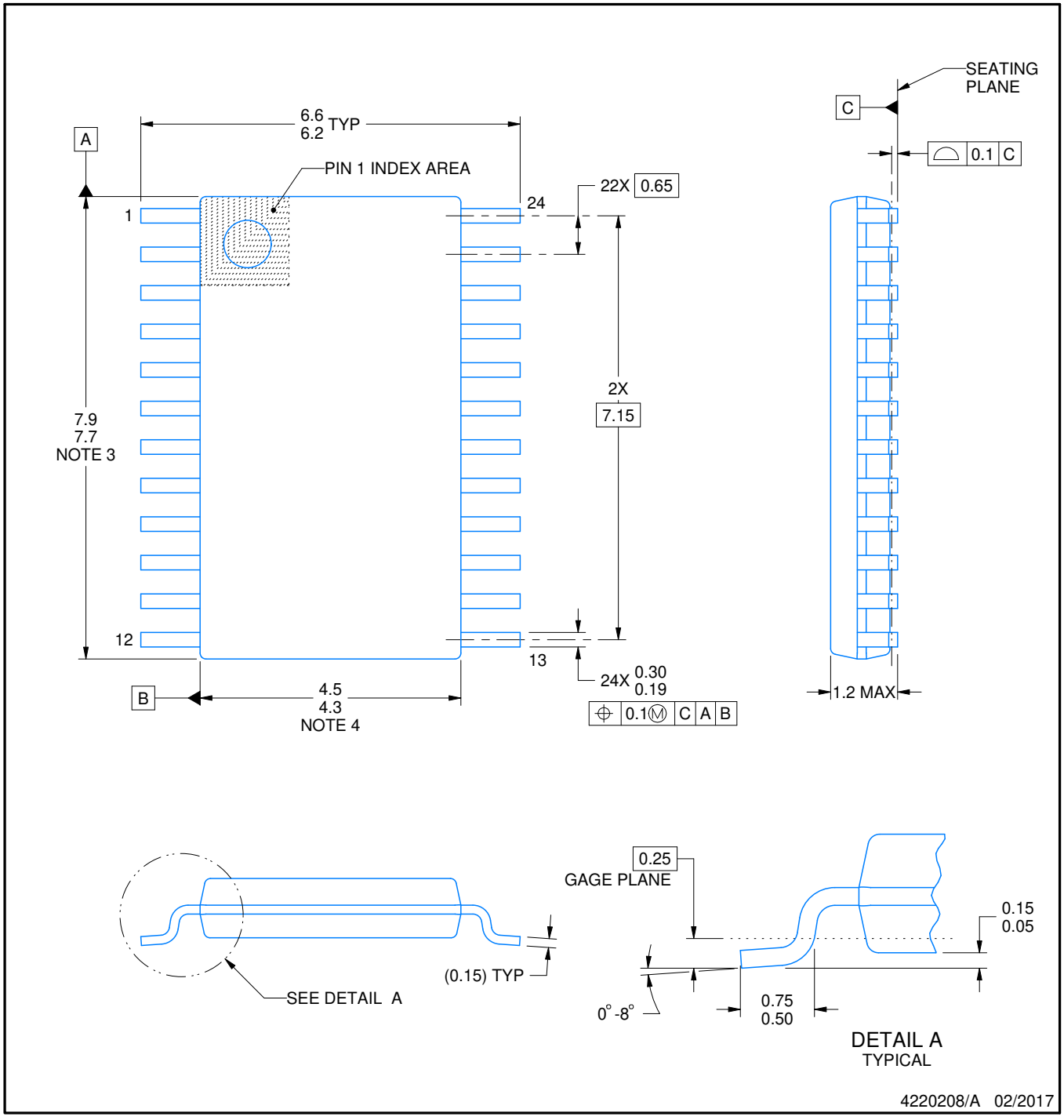
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
BQ24702PW	PW	TSSOP	24	60	530	10.2	3600	3.5
BQ24702PWG4	PW	TSSOP	24	60	530	10.2	3600	3.5
BQ24703PW	PW	TSSOP	24	60	530	10.2	3600	3.5

PACKAGE OUTLINE

PW0024A

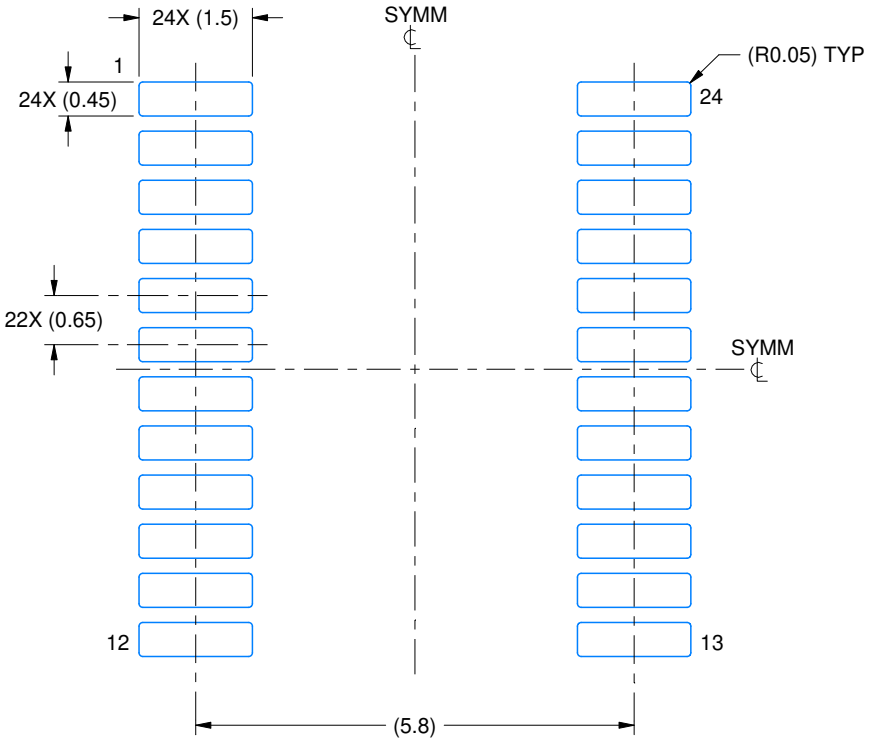
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

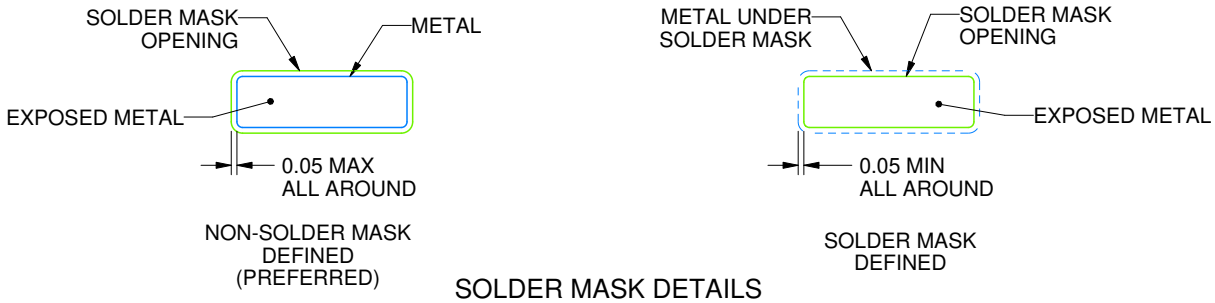


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

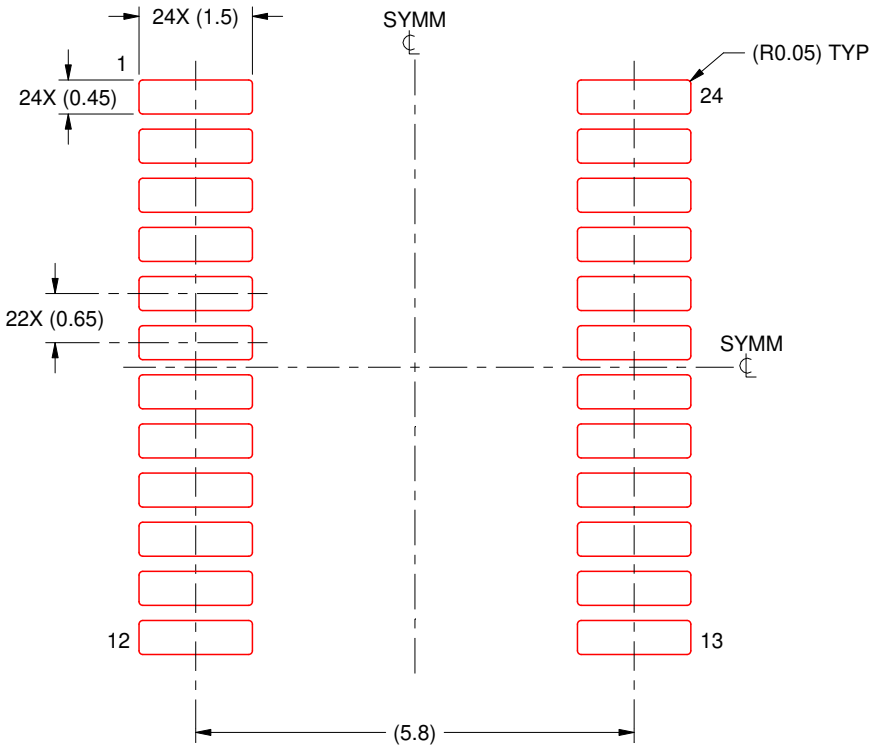


SOLDER MASK DETAILS

4220208/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220208/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

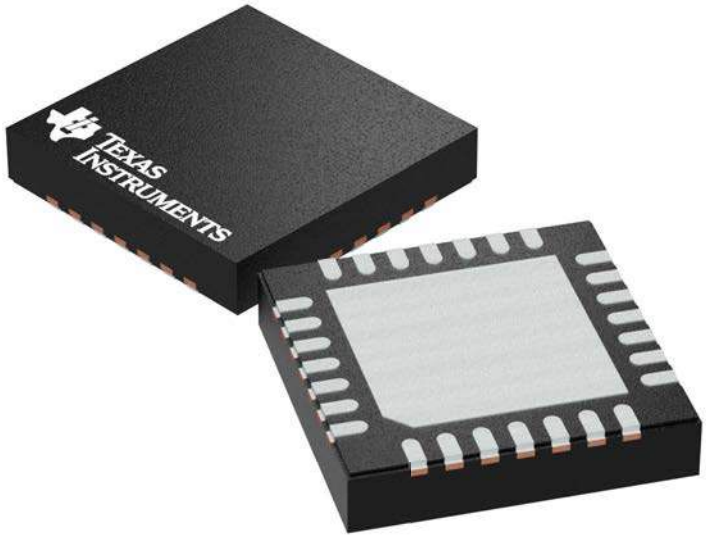
GENERIC PACKAGE VIEW

RHD 28

VQFN - 1 mm max height

5 x 5 mm, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

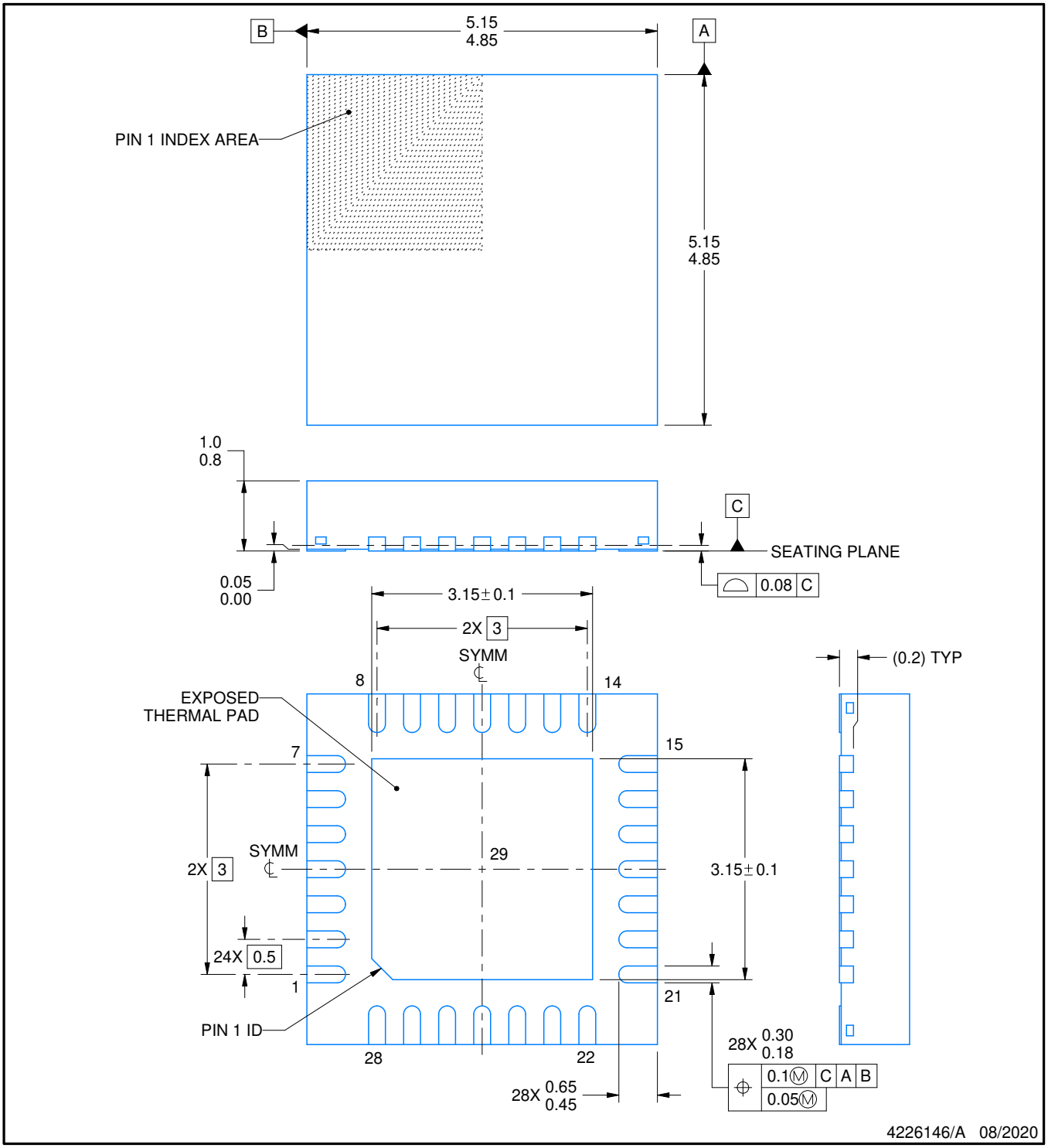
4204400/G

RHD0028B

PACKAGE OUTLINE

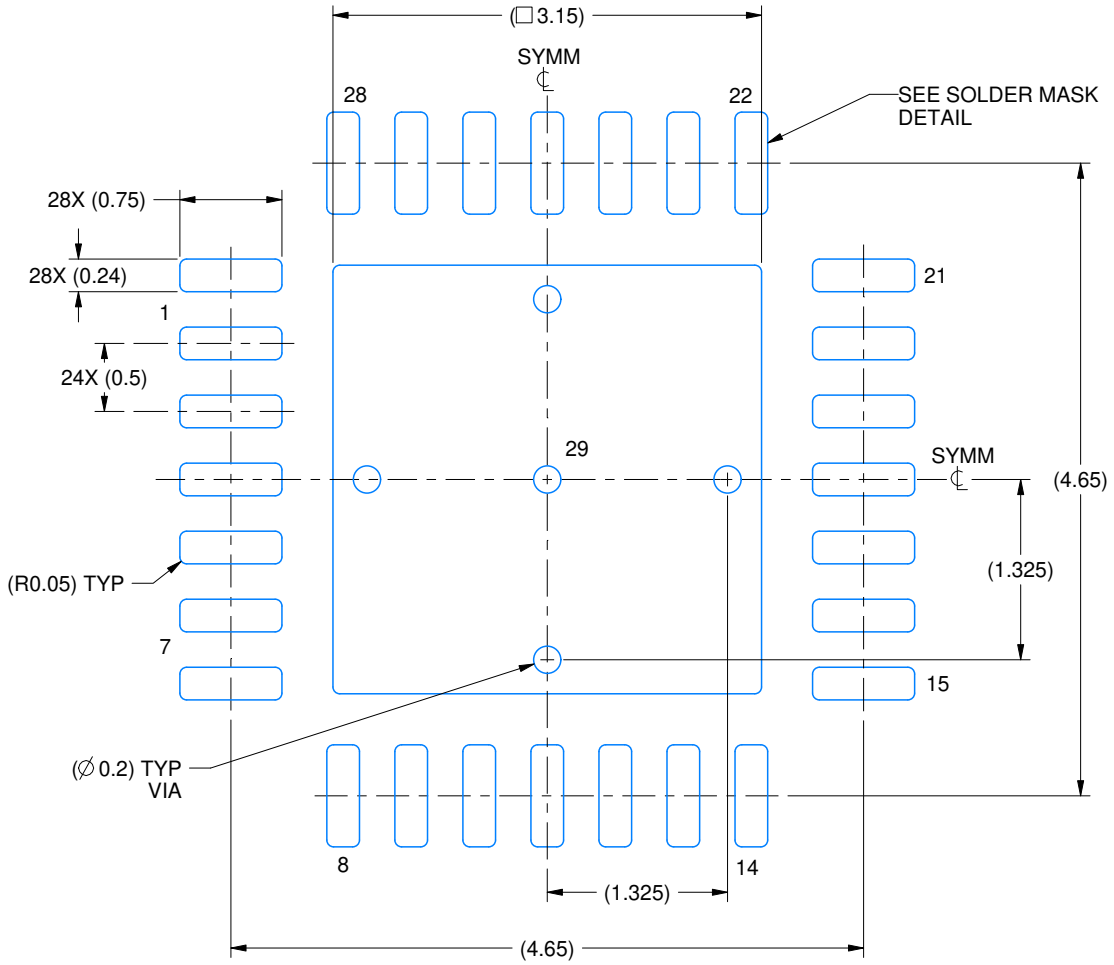
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

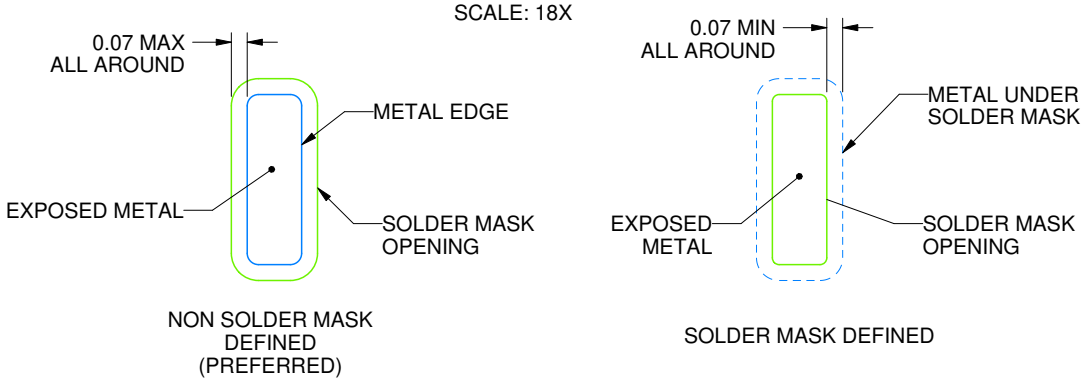


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 18X



SOLDER MASK DETAILS

4226146/A 08/2020

NOTES: (continued)

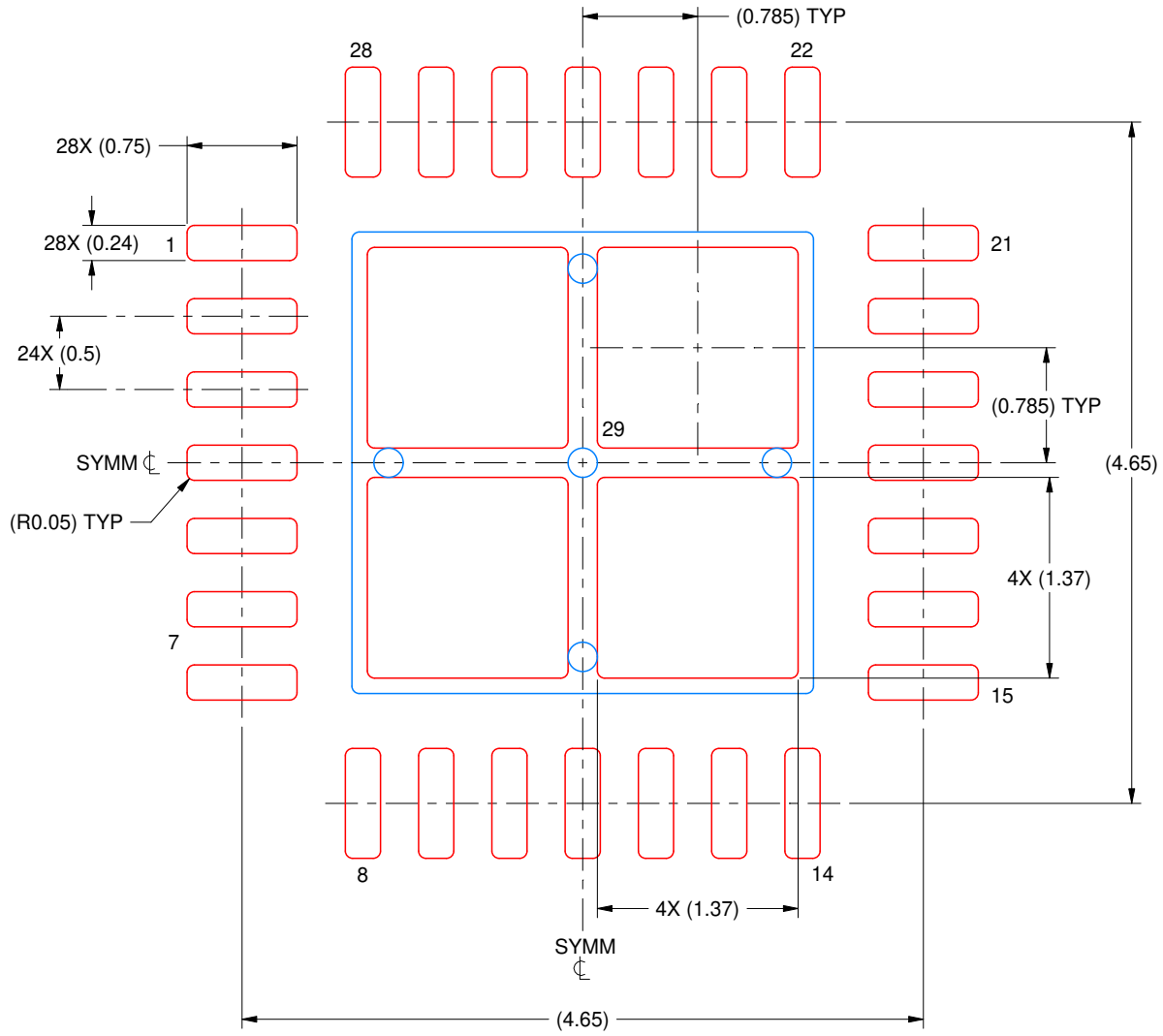
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RHD0028B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 29
76% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4226146/A 08/2020

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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