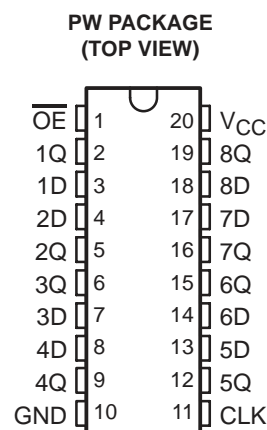


3.3-V ABT OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

SN74LVTH374-EP
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- **Controlled Baseline**
 - One Assembly/Test Site, One Fabrication Site
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product-Change Notification**
- **Qualification Pedigree†**
- **Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})**
- **Typical V_{OLP} (Output Ground Bounce) <0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$**
- **Supports Unregulated Battery Operation Down to 2.7 V**
- **I_{off} and Power-Up 3-State Support Hot Insertion**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Latch-Up Performance Exceeds 500 mA Per JESD 17**
- **ESD Protection Exceeds JESD 22**
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)

† Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.



description/ordering information

This octal flip-flop is designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

The eight flip-flops of the SN74LVTH374 are edge-triggered D-type flip-flops. On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels set up at the data (D) inputs.

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

\overline{OE} does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

When V_{CC} is between 0 and 1.5 V, the devices are in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

This device is fully specified for hot-insertion applications using I_{off} and power-up 3-state. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

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3.3-V ABT OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

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ORDERING INFORMATION

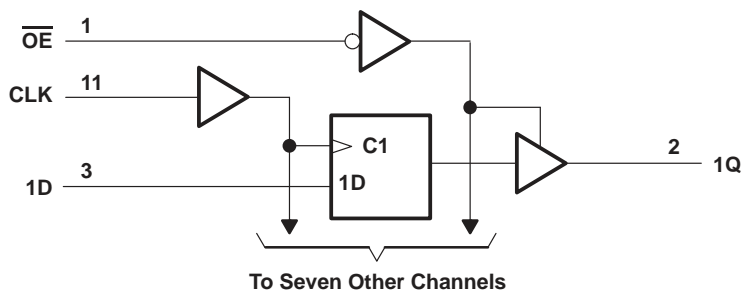
| T _A | PACKAGE† | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|----------------------------|-----------------------|------------------|
| -40°C to 85°C | TSSOP – PW Tape and reel | SN74LVTH374IPWREP | LH374EP |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE (each flip-flop)

| INPUTS | | | OUTPUT |
|-----------------|--------|---|----------------|
| \overline{OE} | CLK | D | Q |
| L | ↑ | H | H |
| L | ↑ | L | L |
| L | H or L | X | Q ₀ |
| H | X | X | Z |

logic diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|---|----------------------------|
| Supply voltage range, V_{CC} | –0.5 V to 4.6 V |
| Input voltage range, V_I (see Note 1) | –0.5 V to 7 V |
| Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1) | –0.5 V to 7 V |
| Voltage range applied to any output in the high state, V_O (see Note 1) | –0.5 V to $V_{CC} + 0.5$ V |
| Current into any output in the low state, I_O | 128 mA |
| Current into any output in the high state, I_O (see Note 2) | 64 mA |
| Input clamp current, I_{IK} ($V_I < 0$) | –50 mA |
| Output clamp current, I_{OK} ($V_O < 0$) | –50 mA |
| Package thermal impedance, θ_{JA} (see Note 3) | 83°C/W |
| Storage temperature range, T_{stg} | –65°C to 150°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
 3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 4)

| | | MIN | MAX | UNIT |
|--------------------------|------------------------------------|-----|-----|------|
| V_{CC} | Supply voltage | 2.7 | 3.6 | V |
| V_{IH} | High-level input voltage | 2 | | V |
| V_{IL} | Low-level input voltage | | 0.8 | V |
| V_I | Input voltage | | 5.5 | V |
| I_{OH} | High-level output current | | –32 | mA |
| I_{OL} | Low-level output current | | 64 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | | 10 | ns/V |
| $\Delta t/\Delta V_{CC}$ | Power-up ramp rate | 200 | | μs/V |
| T_A | Operating free-air temperature | –40 | 85 | °C |

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP† | MAX | UNIT |
|-----------------------|--|--|----------------------------------|------|------|------|
| V _{IK} | | V _{CC} = 2.7 V, I _I = -18 mA | | | -1.2 | V |
| V _{OH} | | V _{CC} = 2.7 V to 3.6 V, I _{OH} = -100 μA | V _{CC} -0.2 | | | V |
| | | V _{CC} = 2.7 V, I _{OH} = -8 mA | 2.4 | | | |
| | | V _{CC} = 3 V, I _{OH} = -32 mA | 2 | | | |
| V _{OL} | | V _{CC} = 2.7 V | I _{OL} = 100 μA | | 0.2 | V |
| | | | I _{OL} = 24 mA | | 0.5 | |
| | | V _{CC} = 3 V | I _{OL} = 16 mA | | 0.4 | |
| | | | I _{OL} = 32 mA | | 0.5 | |
| | | | I _{OL} = 64 mA | | 0.55 | |
| I _I | | V _{CC} = 0 or 3.6 V, V _I = 5.5 V | | | 10 | μA |
| | | Control inputs V _{CC} = 3.6 V, V _I = V _{CC} or GND | | | ±1 | |
| | | Data inputs V _{CC} = 3.6 V | V _I = V _{CC} | | | |
| | | | V _I = 0 | | | -5 |
| I _{off} | | V _{CC} = 0, V _I or V _O = 0 to 4.5 V | | | ±100 | μA |
| I _I (hold) | | Data inputs V _{CC} = 3 V | V _I = 0.8 V | | 75 | μA |
| | | | V _I = 2 V | | -75 | |
| | | V _{CC} = 3.6 V‡, V _I = 0 to 3.6 V | | | | |
| I _{OZH} | | V _{CC} = 3.6 V, V _O = 3 V | | | 5 | μA |
| I _{OZL} | | V _{CC} = 3.6 V, V _O = 0.5 V | | | -5 | μA |
| I _{OZPU} | | V _{CC} = 0 to 1.5 V, V _O = 0.5 V to 3 V, \overline{OE} = don't care | | | ±100 | μA |
| I _{OZPD} | | V _{CC} = 1.5 V to 0, V _O = 0.5 V to 3 V, \overline{OE} = don't care | | | ±100 | μA |
| I _{CC} | | V _{CC} = 3.6 V, I _O = 0, V _I = V _{CC} or GND | Outputs high | | 0.19 | mA |
| | | | Outputs low | | 5 | |
| | | | Outputs disabled | | 0.19 | |
| ΔI _{CC} § | | V _{CC} = 3 V to 3.6 V, One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND | | | 0.2 | mA |
| C _i | | V _I = 3 V or 0 | | | 3 | pF |
| C _o | | V _O = 3 V or 0 | | | 7 | pF |

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

‡ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

§ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

| | | V _{CC} = 3.3 V ± 0.3 V | | V _{CC} = 2.7 V | | UNIT |
|--------------------|---------------------------------|------------------------------------|-----|-------------------------|-----|------|
| | | MIN | MAX | MIN | MAX | |
| f _{clock} | Clock frequency | 150 | | 150 | | MHz |
| t _w | Pulse duration, CLK high or low | 3.3 | | 3.3 | | ns |
| t _{su} | Setup time, data before CLK↑ | 1.5 | | 2 | | ns |
| t _h | Hold time, data after CLK↑ | 0.8 | | 0 | | ns |



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switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

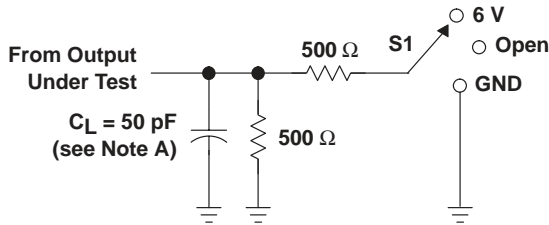
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$ | | | $V_{CC} = 2.7\text{ V}$ | | UNIT |
|-----------|-----------------|----------------|---|------|-----|-------------------------|-----|------|
| | | | MIN | TYP† | MAX | MIN | MAX | |
| f_{max} | | | 150 | | | 150 | | MHz |
| t_{PLH} | CLK | Q | 1.8 | 2.9 | 4.5 | 5 | | ns |
| t_{PHL} | | | 1.8 | 2.9 | 4.2 | 4.3 | | |
| t_{PZH} | \overline{OE} | Q | 1.3 | 2.8 | 4.7 | 5.6 | | ns |
| t_{PZL} | | | 1.6 | 3 | 4.7 | 5.2 | | |
| t_{PHZ} | \overline{OE} | Q | 1.9 | 3 | 4.6 | 4.9 | | ns |
| t_{PLZ} | | | 2 | 3.1 | 4.5 | 4.6 | | |

† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

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3.3-V ABT OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOP
WITH 3-STATE OUTPUTS

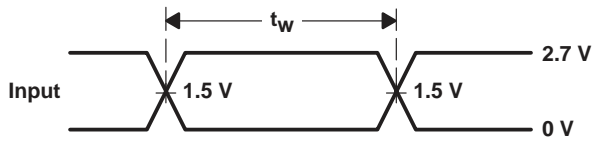
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PARAMETER MEASUREMENT INFORMATION

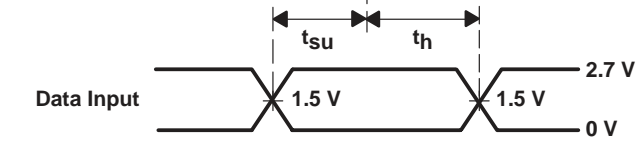
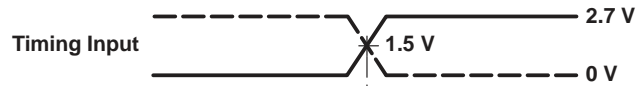


LOAD CIRCUIT

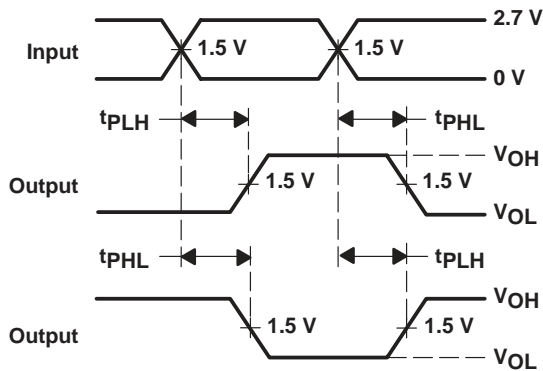
| TEST | S1 |
|-------------------|------|
| t_{PLH}/t_{PHL} | Open |
| t_{PLZ}/t_{PZL} | 6 V |
| t_{PHZ}/t_{PZH} | GND |



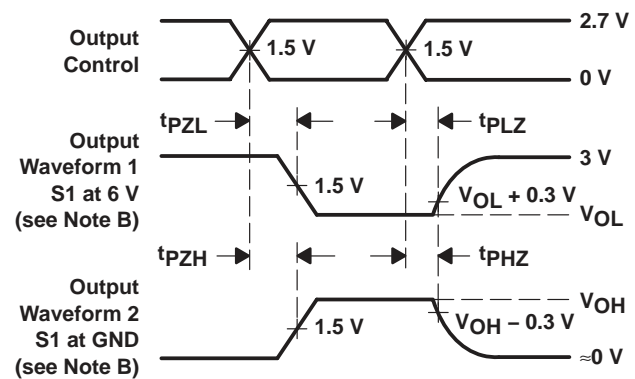
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|-------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| SN74LVTH374IPWREP | ACTIVE | TSSOP | PW | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LH374EP | Samples |
| V62/04676-01XE | ACTIVE | TSSOP | PW | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LH374EP | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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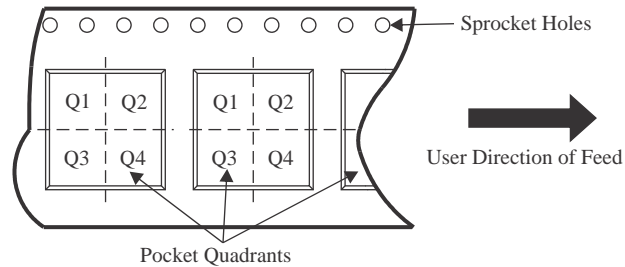
OTHER QUALIFIED VERSIONS OF SN74LVTH374-EP :

- Catalog: [SN74LVTH374](#)
- Military: [SN54LVTH374](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74LVTH374IPWREP | TSSOP | PW | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.1 | 1.6 | 8.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74LVTH374IPWREP | TSSOP | PW | 20 | 2000 | 356.0 | 356.0 | 35.0 |

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