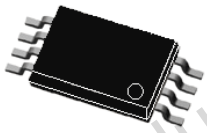
STC5NF20V

N-channel 20V - 0.030Ω - 5A - TSSOP8
2.7V-drive STripFET™ II Power MOSFET

Features

Type	V_{DSS}	$R_{DS(on)}$	I_D
STC5NF20V	20V	< 0.040 Ω (@ 4.5 V) < 0.045 Ω (@ 2.7 V)	5A

- Ultra low threshold gate drive (2.7V)
- Standard outline for easy automated surface mount assembly



TSSOP8

Application

- Switching applications

Description

This Power MOSFET is the latest development of STMicroelectronics unique "single feature size" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

Figure 1. Internal schematic diagram

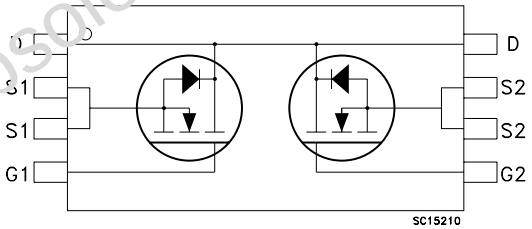


Table 1. Device summary

Order code	Marking	Package	Packaging
STC5NF20V	5N20V	TSSOP8	Tape & reel

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage (V_{GS} = 0)	20	V
V_{DGR}	Drain-gate voltage (R_{GS} = 20KΩ)	20	V
V_{GS}	Gate-source voltage	± 12	V
I_D	Drain current (continuous) at T_C = 25°C	5	A
I_D	Drain current (continuous) at T_C=100°C	3	A
I_{DM}(1)	Drain current (pulsed)	20	A
P_{TOT}	Total dissipation at T_C = 25°C	1.5	W
T_{stg}	Storage temperature	–55 to 150	°C
T_J	Max. Operating junction temperature	–55 to 150	°C

1. Pulse width limited by safe operating area

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thJ\text{-}PBC}$	Thermal resistance junction-PBC Max	100 (1)	°C/W
$R_{thJ\text{-}PBC}$	Thermal resistance junction-PBC Max	83.5 (2)	°C/W

1. When Mounted on FR-4 board with 1 inch^2 pad, 2 oz. of Cu. and t = 10 sec.
2. When Mounted on minimum recommended footprint

2 Electrical characteristics

(T_{CASE}=25°C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 250µA, V_{GS}= 0	20			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max rating, V_{DS} = Max rating @125°C			1 10	µA µA
I_{GSS}	Gate body leakage current (V_{DS} = 0)	V_{GS} = ±12V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS}= V_{GS}, I_D = 250µA	0.6			V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS}= 4.5V, I_D= 2.5A V_{GS} =2.7V, I_D = 2.5A		0.030 0.037	0.040 0.045	Ω Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward transconductance	V_{DS} = 15 V, I_D = 2.5A		9.5		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} =15V, f = 1 MHz, V_{GS} = 0		460 200 50		pF pF pF
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} =10V, I_D = 4.5A V_{GS} =4.5V		8.5 1.8 2.4	11.5	nC nC nC

1. Pulsed: pulse duration=300µs, duty cycle 1.5%

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on delay time Rise time Turn-off delay time Fall time	V_{DD}= 10V, I_D= 2.5A, R_G=4.7Ω, V_{GS}=4.5V *Figure 14 on page 8*		7 33 27 10		ns ns ns ns
$t_{d(off)}$ t_f t_c	Off-voltage rise time Fall time Cross-over time	Vclamp =16V, I_D = 5A R_G = 4.7Ω, V_{GS} = 4.5V *Figure 16 on page 8*		26 11 21		ns ns ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
I_{SD}	Source-drain current				5	A
I_{SDM}(1)	Source-drain current (pulsed)				20	A
V_{SD}(2)	Forward on voltage	I_{SD} = 5A, V_{GS} = 0			1.2	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 5A, di/dt = 100A/µs, V_{DD} = 10V, T_J = 150°C *Figure 16 on page 8*		26 13 1		ns µC A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

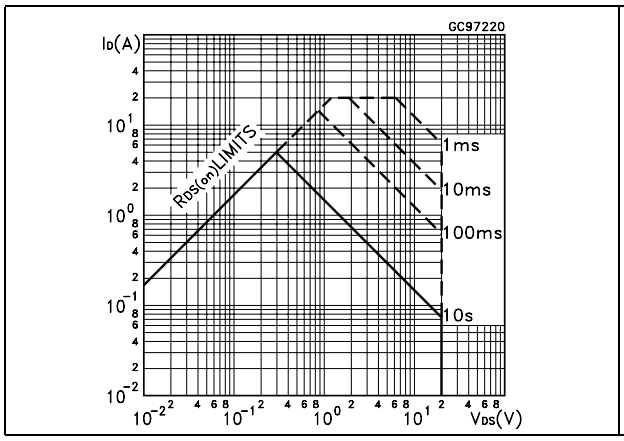


Figure 3. Thermal impedance

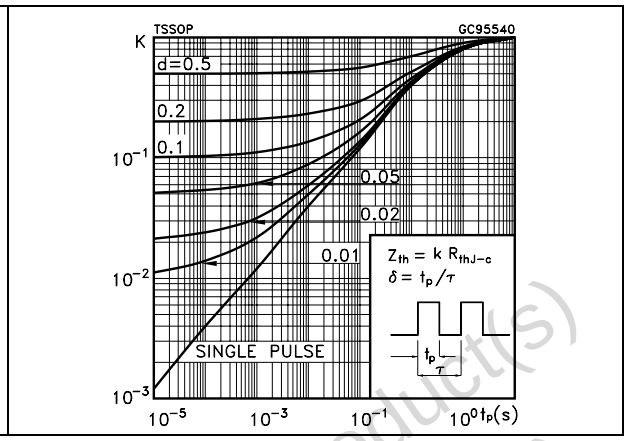


Figure 4. Output characteristics

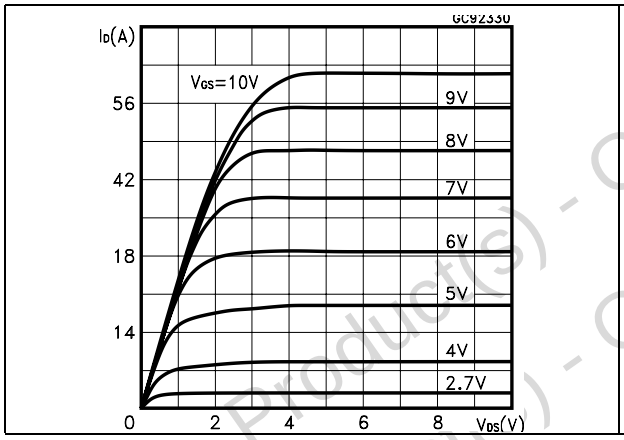


Figure 5. Transfer characteristics

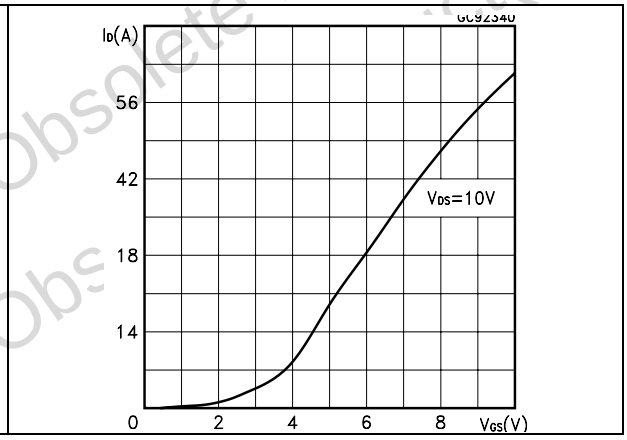


Figure 6. Transconductance

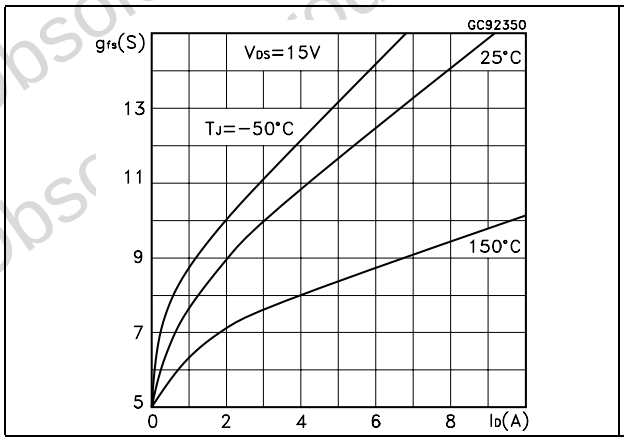


Figure 7. Static drain-source on resistance

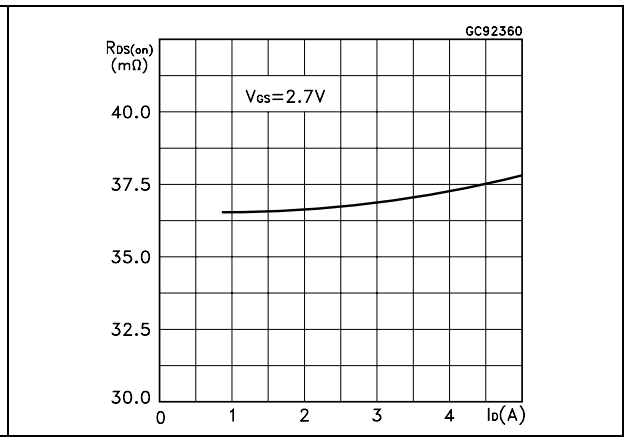


Figure 8. Gate charge vs. gate-source voltage

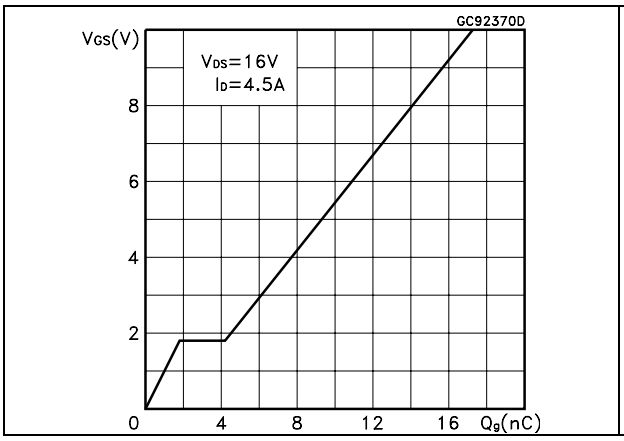


Figure 9. Capacitance variations

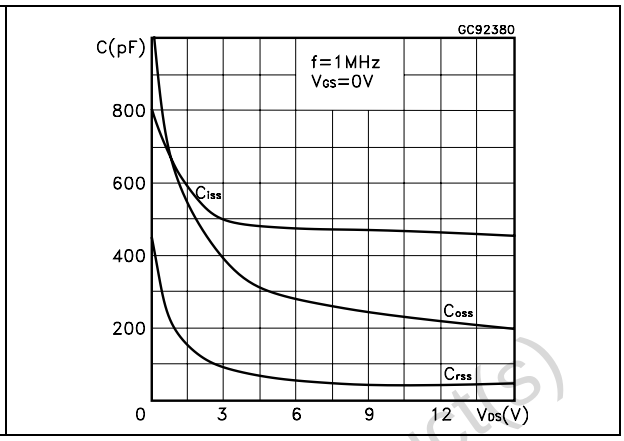


Figure 10. Normalized gate threshold voltage vs. temperature

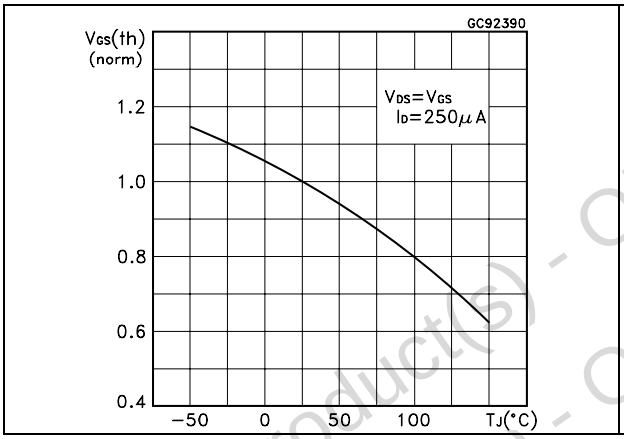


Figure 11. Normalized on resistance vs. temperature

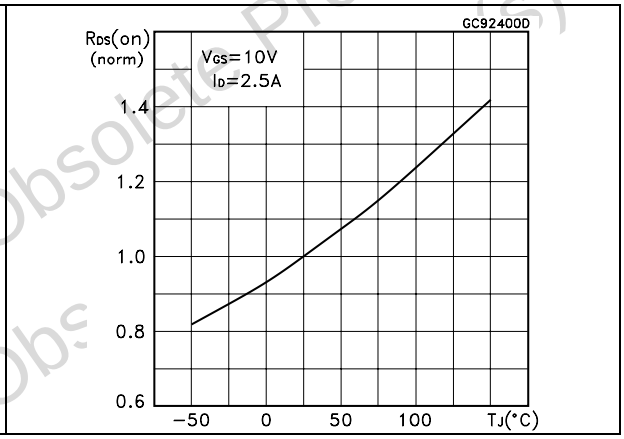


Figure 12. Source-drain diode forward characteristics

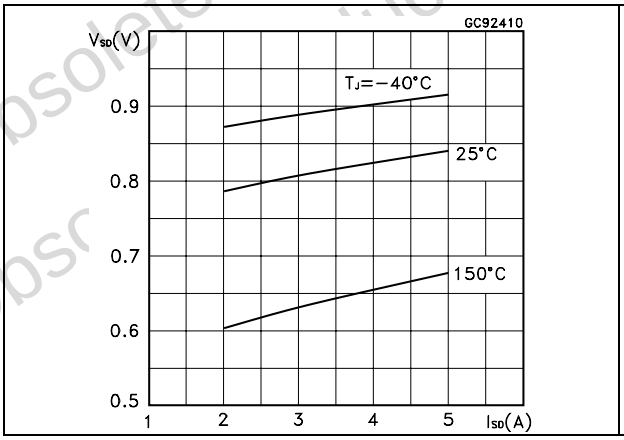
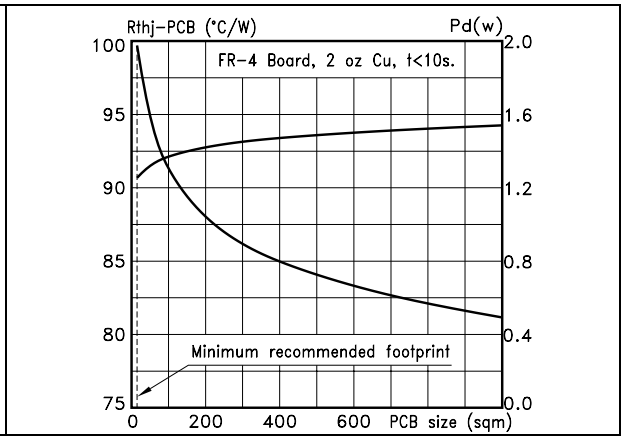


Figure 13. Thermal resistance and max power



3 Test circuit

Figure 14. Switching times test circuit for resistive load

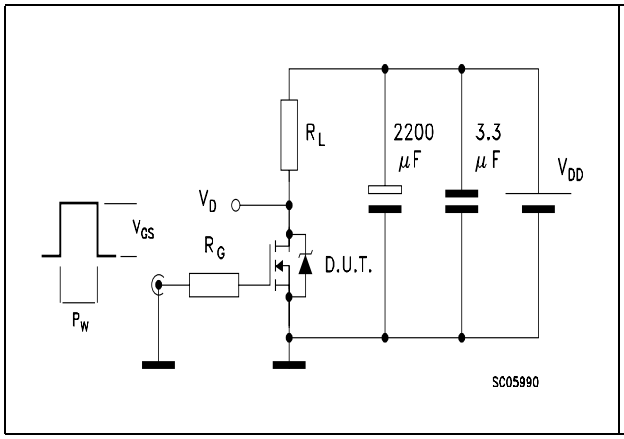


Figure 15. Gate charge test circuit

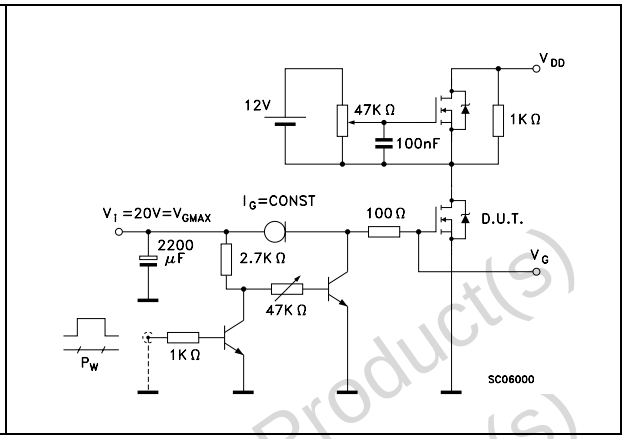


Figure 16. Test circuit for inductive load switching and diode recovery times

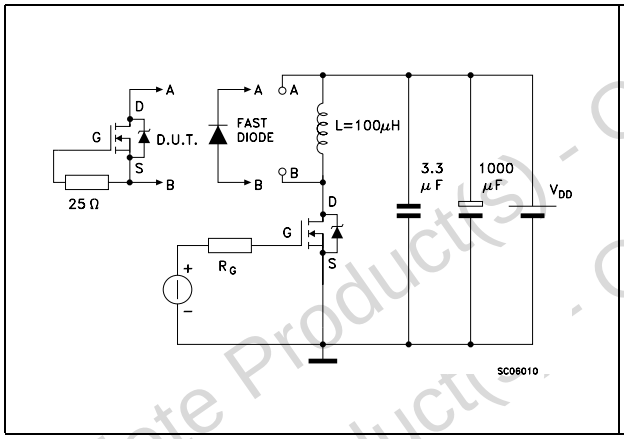


Figure 17. Unclamped Inductive load test circuit

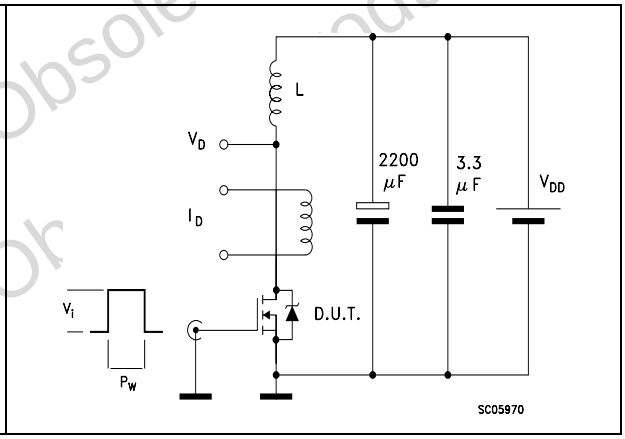
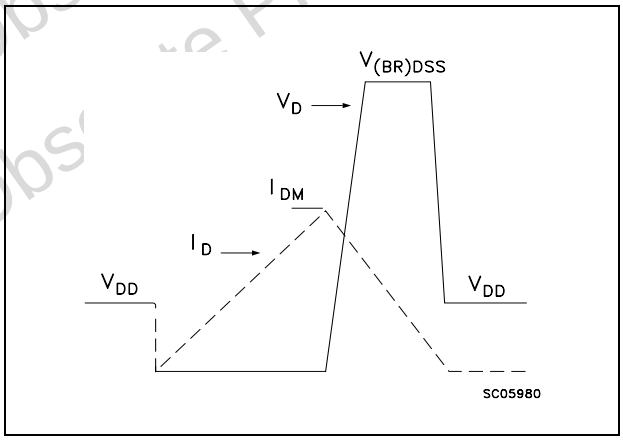


Figure 18. Unclamped inductive waveform

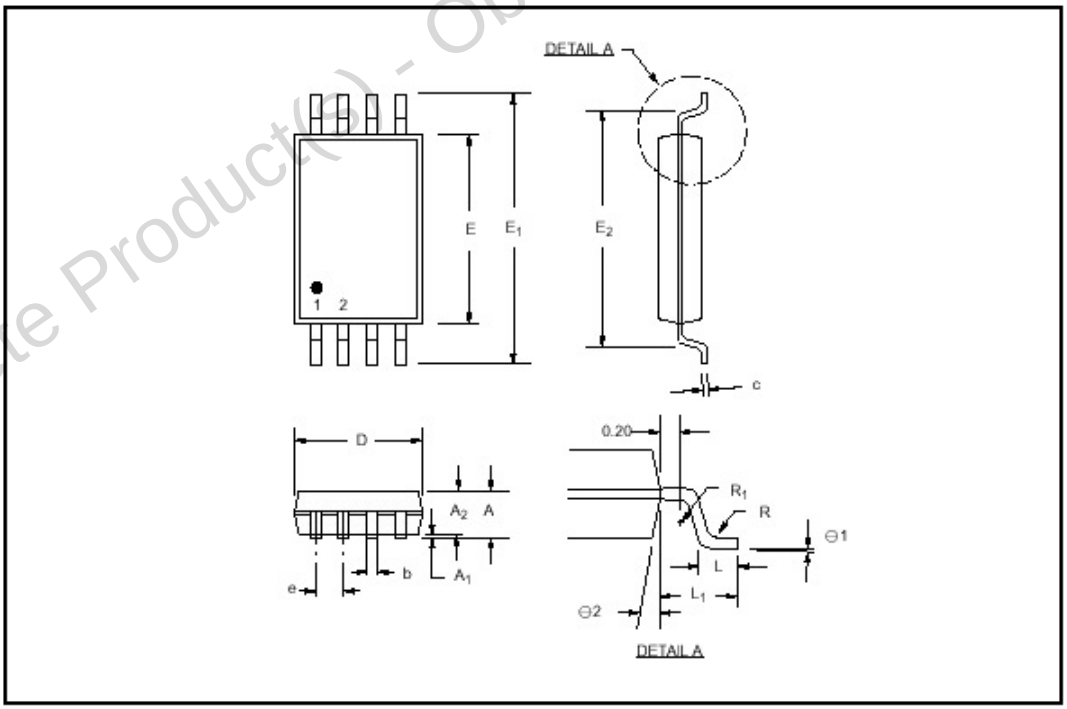


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

TSSOP8 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	1.05		1.20	0.041		0.047
A1	0.05		0.15	0.002		0.006
A2	0.80		1.05	0.032		0.041
b	0.19		0.30	0.008		0.012
c		0.127			0.005	
D	2.90		3.10	0.114		0.122
E	4.30		4.50	0.170		0.177
E1	6.20		6.60	0.240		0.260
E2	5.14		5.24	0.202		0.206
e		0.65			0.025	
L	0.45		0.75	0.018		0.030
L1	0.90		1.10	0.0355		0.0433
R	0.09			0.004		
R1	0.09			0.004		
θ1	0°		8°	0°		8°
θ2	12°					



5 Revision history

Table 8. Document revision history

Date	Revision	Changes
09-Sep-2004	3	Initial electronic version
03-Aug-2006	4	The document has been reformatted, SOA updated
01-Feb-2007	5	Typo mistake on *Table 2*.
25-Oct-2007	6	Update marking on *Table 1*