

# Low IF Receiver Reference Design

National Semiconductor  
RD-170  
Strategic Signal Path Applications  
December 2008



## 1.0 Design Description

The SP16130CH4RB Reference Board demonstrates a low IF receiver subsystem application including an ADC16V130 analog-to-digital converter (ADC) and LMK04031B clock conditioner which provides digitization and clocking as used in wireless infrastructure systems.

This subsystem reference design provides single to differential conversion and lowpass filtering of the input signal with an optimized, double-balun network and high dynamic range digitization to parallel LVDS outputs using the ADC16V130. The 125 MHz low-jitter, LVPECL clock signal for the ADC is generated by a LMK04031B clock conditioner which demonstrates less than 250 fs of total jitter over the input bandwidth of the ADC.

The measured system performance demonstrates a large signal SNR of 75.8 dBFS and SFDR greater than 84 dBFS for a -1 dBFS, 52 MHz input signal and a sampling frequency of 125 MSPS. For small signals, the performance improves to 78.0 dBFS SNR and greater than 94 dBFS SFDR.

Evaluation of this reference board is simplified with the WaveVision 5.1 Data Capture Board and WaveVision 5 software.

## 2.0 Features

**Key Features of the SP16130CH4RB Low IF Receiver Reference Design Board**

- Demonstrates a subsystem architecture used in wireless infrastructure systems and frequency domain analyzers

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- Configured for input frequencies between 5 and 52 MHz
- Board comes fully assembled and tested
- Single (+5V) supply needed
- All ADC features can be exercised
- **Featured Products Include:**
  - ADC16V130 16-bit, 130 Megasample per second (MSPS) ADC with parallel LVDS outputs
  - LMK04031B low-jitter precision clock conditioner consisting of cascaded phase locked loops (PLLs), an internal voltage controlled oscillator (VCO) and a distribution stage
  - Several energy-efficient power management ICs
- Large-signal (-1 dBFS) performance for a 52 MHz input signal:
  - SNR = 75.8 dBFS
  - SFDR > 84 dBFS
- Small-signal (-20 dBFS) performance for a 52 MHz input signal:
  - SNR = 78.0 dBFS
  - SFDR > 94 dBFS
- Total integrated jitter < 250 fs
- PIC Loader board included with reference board for quick and easy configuration of the LMK04031B
- Compatible with the WaveVision 5.1 Data Capture Board and WaveVision 5 software for simplified evaluation

3.0 Schematic

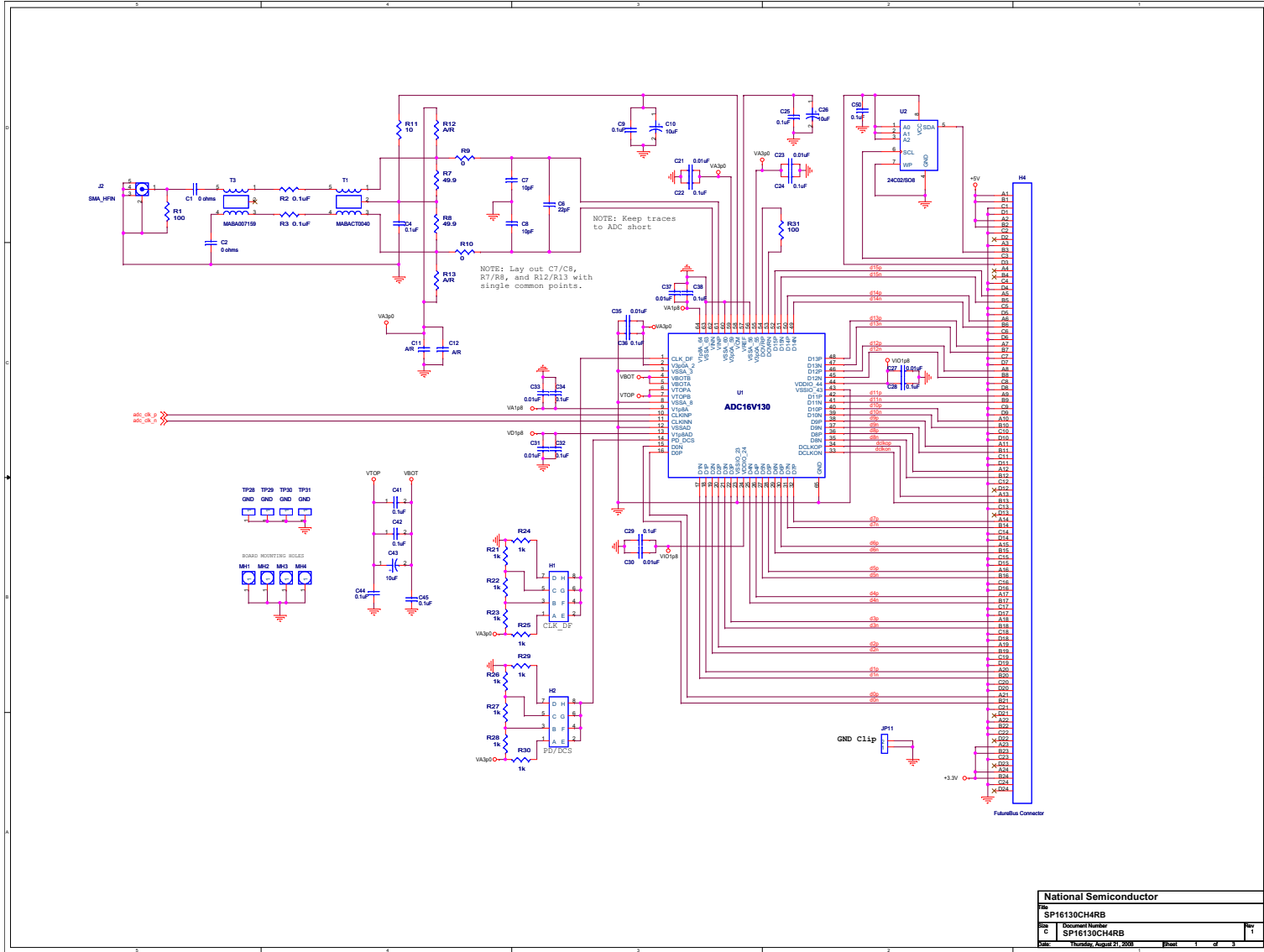


FIGURE 1. SP16130CH4RB Schematic - ADC

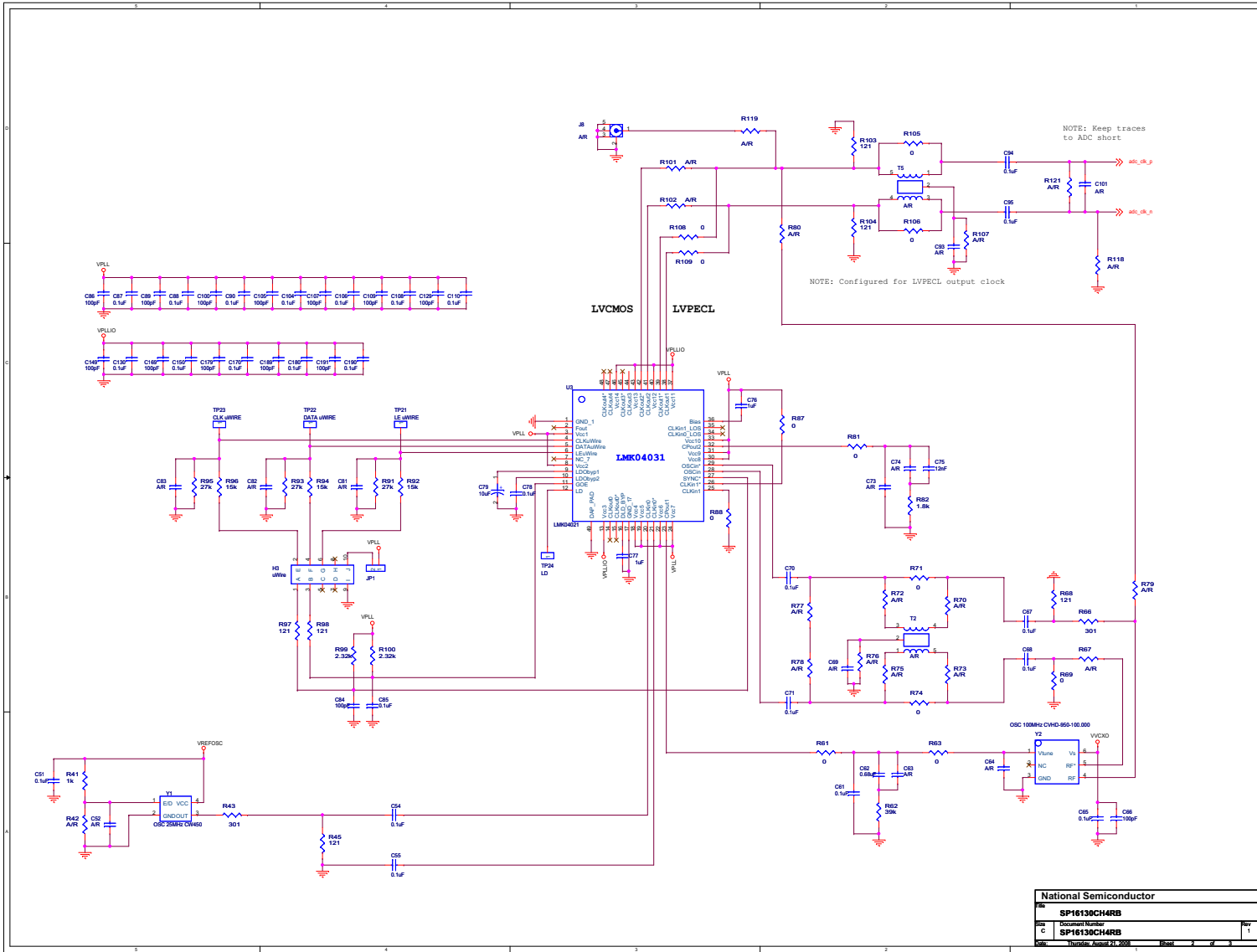
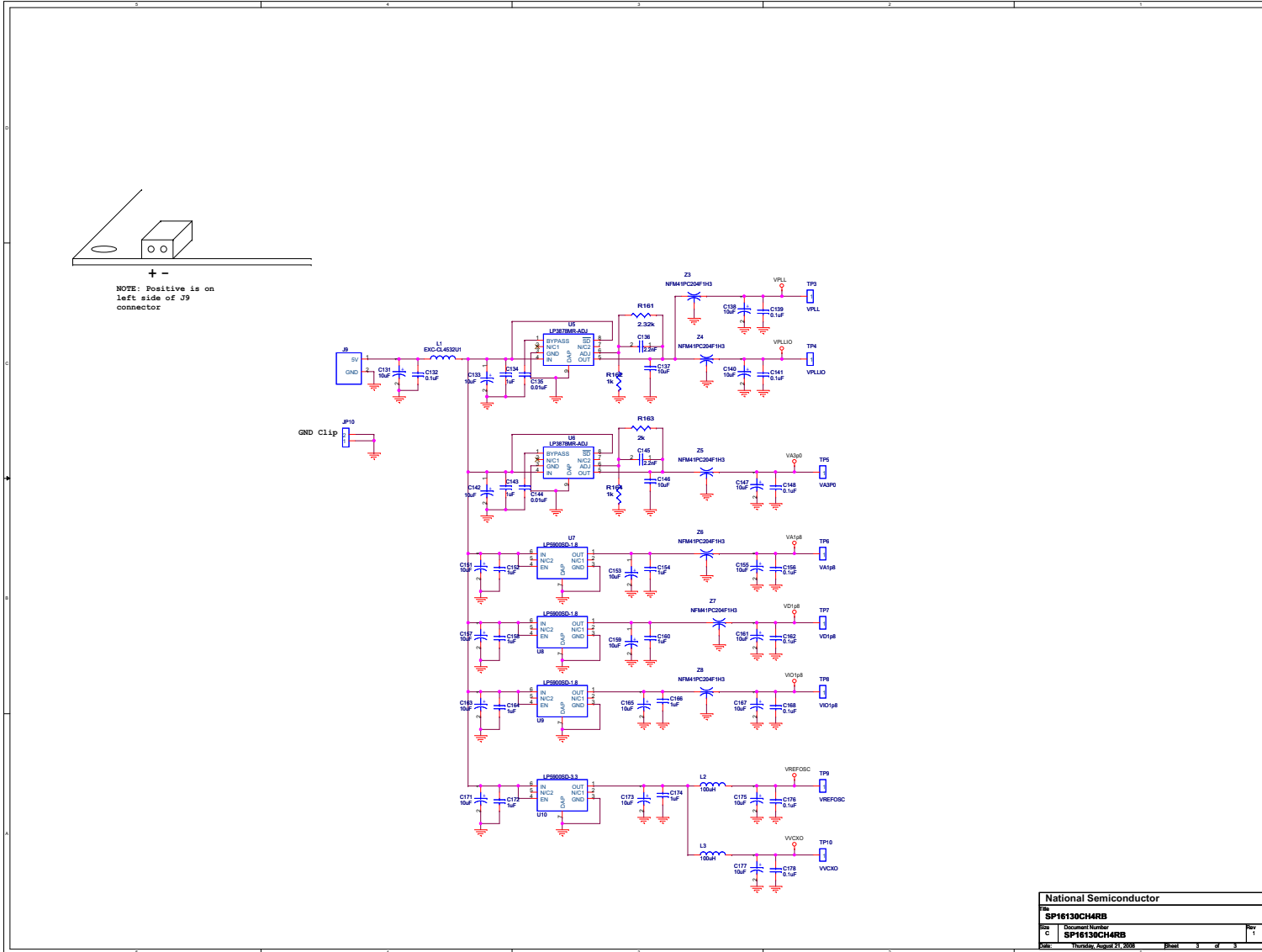


FIGURE 2. SP16130CH4RB Schematic - LMK

schematic2

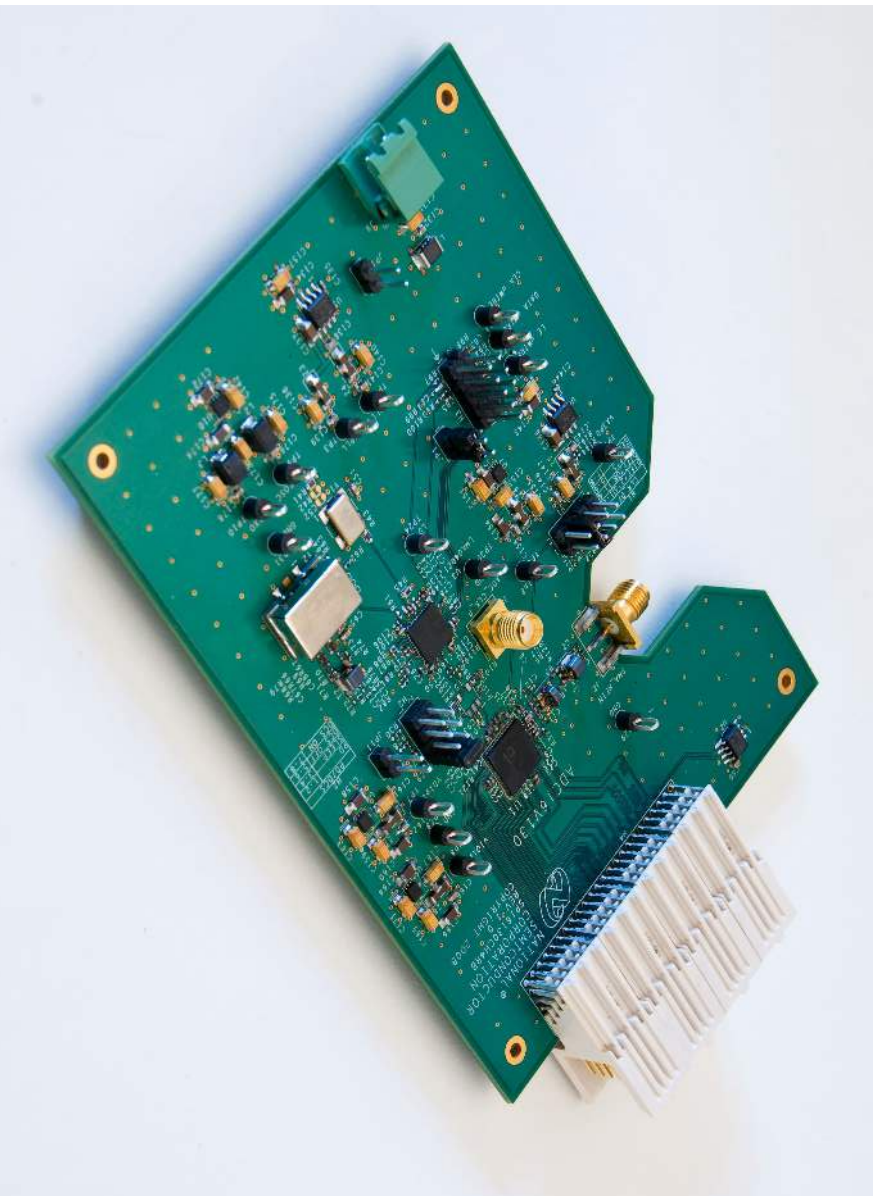


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|------------------------|-------------------------------|
| National Semiconductor |                               |
| Part: SP16130CH4RB     |                               |
| Doc. C                 | Document Number: SP16130CH4RB |
| Rev. C                 | SP16130CH4RB                  |
| Date:                  | Thursday, August 21, 2008     |
| Sheet:                 | 3 of 3                        |

FIGURE 3. SP16130CH4RB Schematic - Power



## 5.0 Board Photos



boardphoto

FIGURE 5. SP16130CH4RB Board Photo

## 6.0 Hardware Description

A comprehensive discussion of this design is within in the **SP16130CH4RB Low IF Receiver Reference Design Board ADC16V130 + LMK04031B User's Guide**. The user

guide can be found in the **Design Resources** section on the RD-170 reference design folder:

<http://www.national.com/rd/RDhtml/RD-170.html>

## 7.0 Layouts

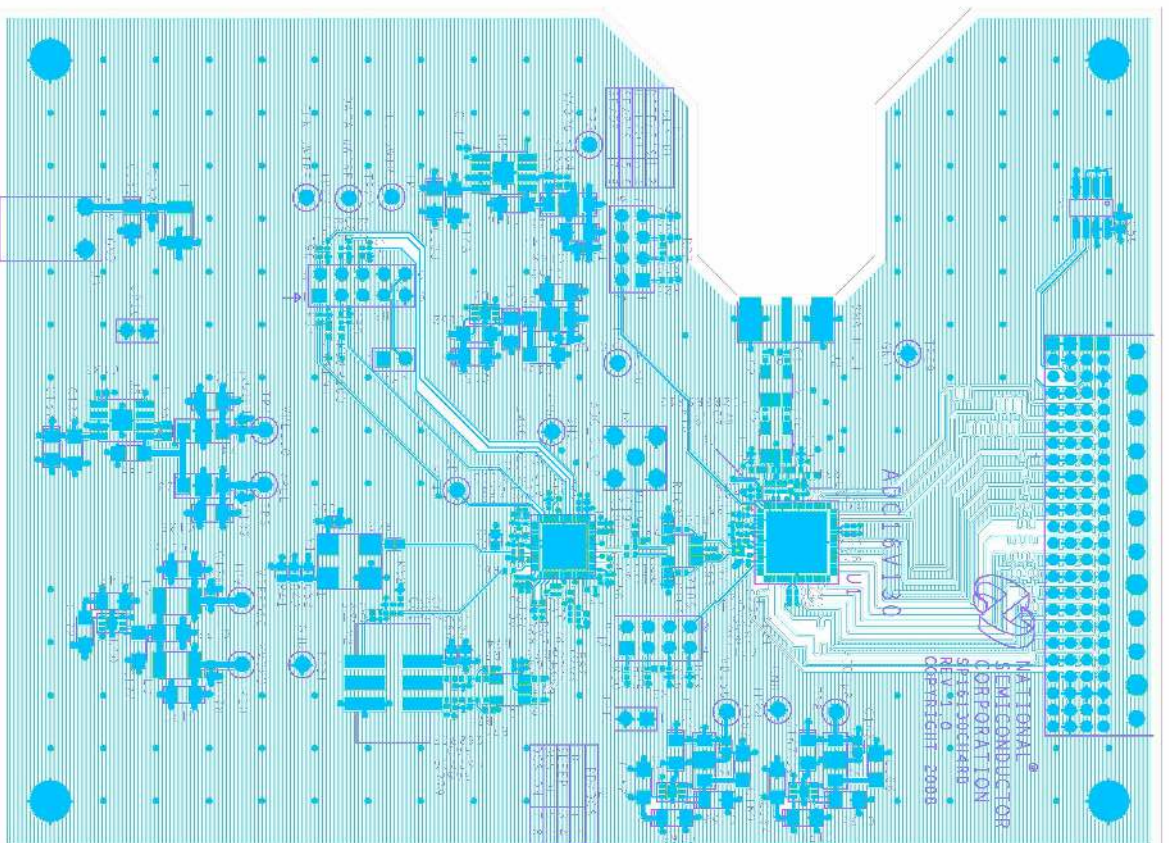


FIGURE 6. SP16130CH4RB Layout - Top Signal Layer

layout

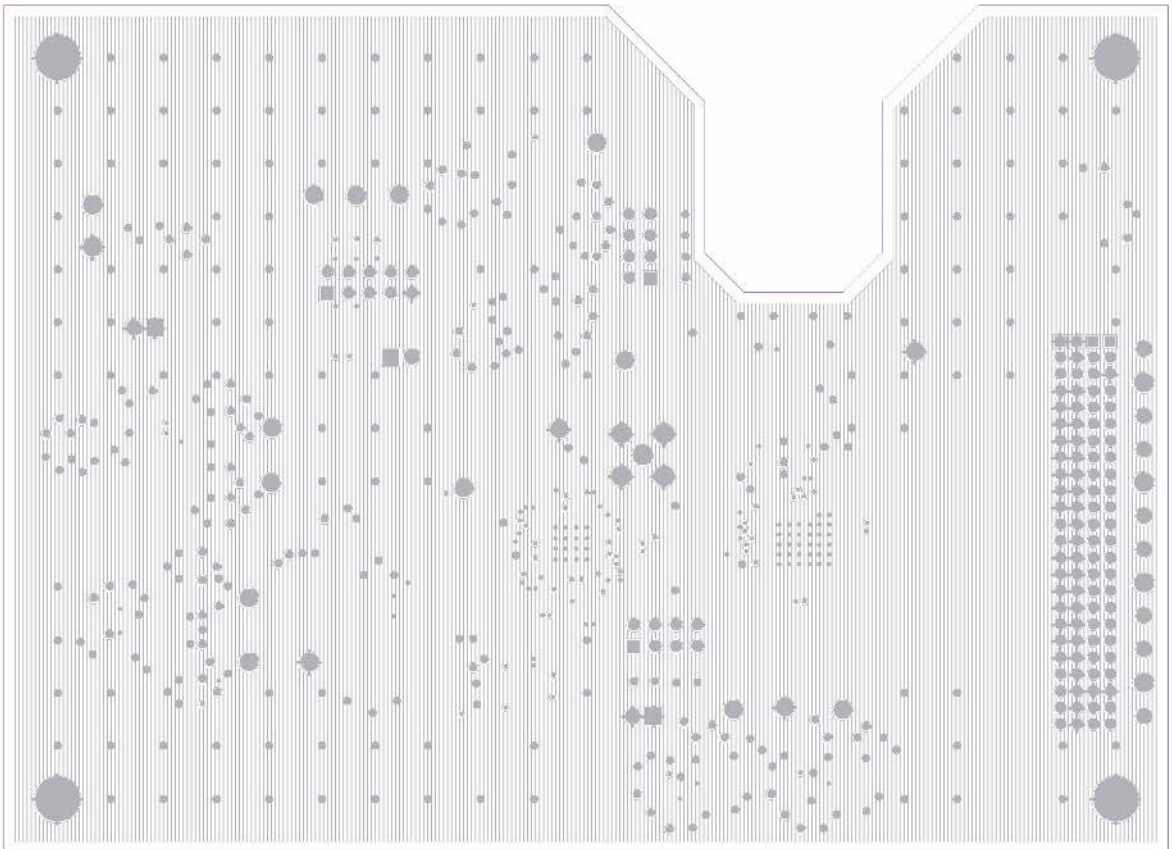
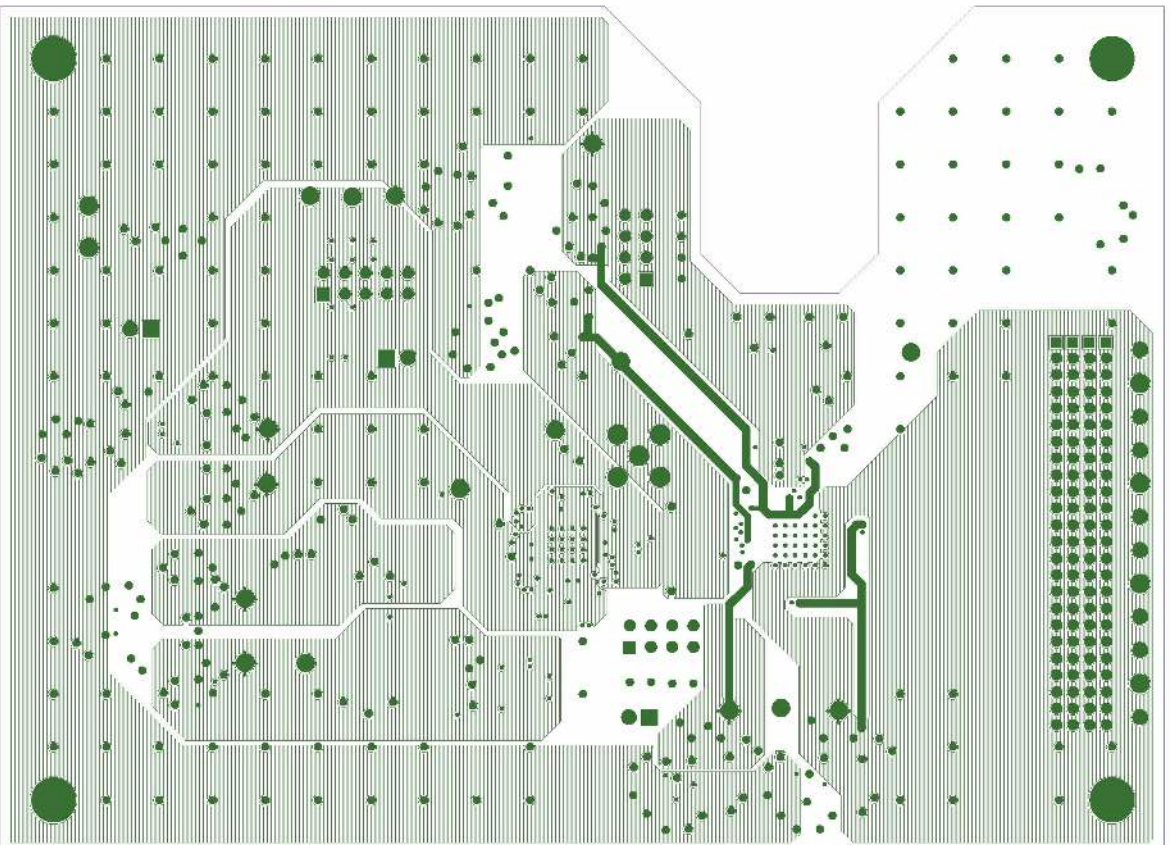


FIGURE 7. SP16130CH4RB Layout - Second GND Layer

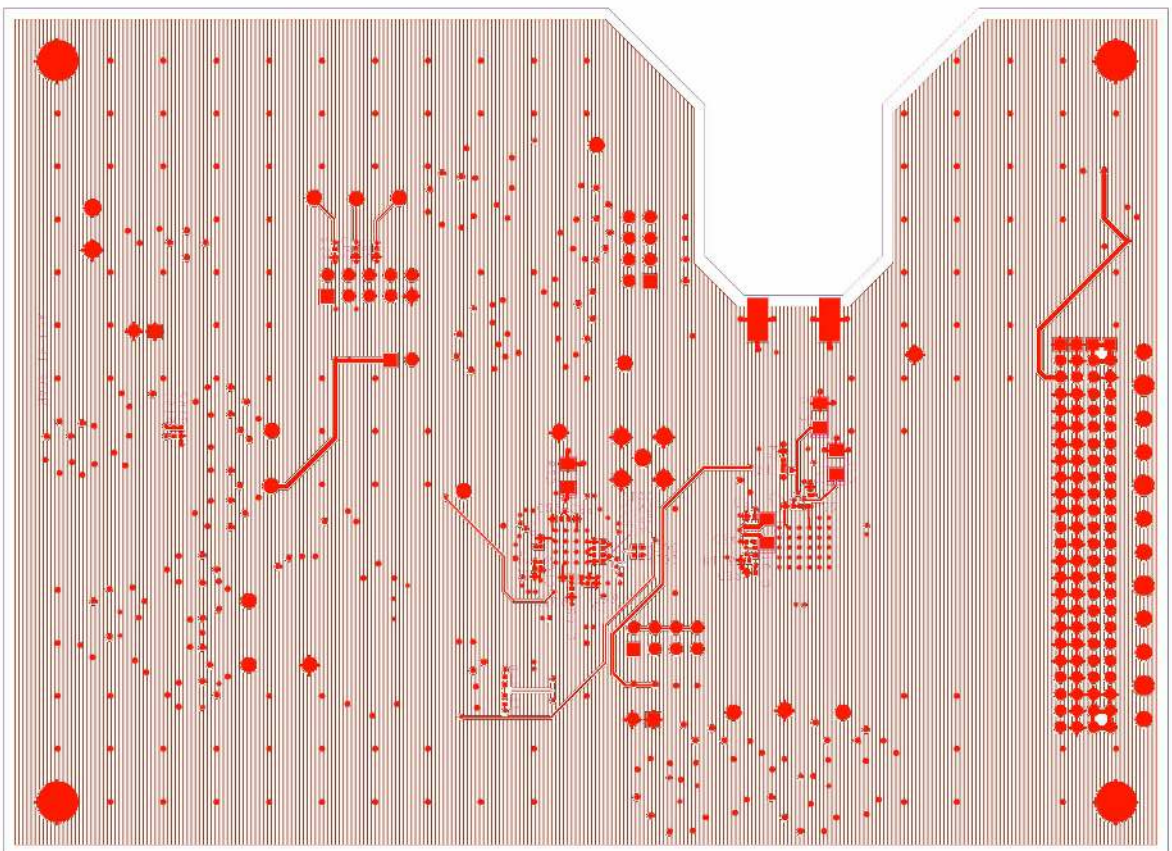
layout





layout2

FIGURE 8. SP16130CH4RB Layout - Third Power Layer



layout3

FIGURE 9. SP16130CH4RB Layout - Bottom Signal Layer

# Notes

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