UM11134

FRDMGD3100HBIEVM half-bridge evaluation board

Rev. 3 — 10 February 2020 User guide

1 FRDMGD3100HBIEVM

Figure 1. FRDMGD3100HBIEVM

2 Important notice

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This evaluation kit is intended for use of ENGINEERING DEVELOPMENT OR EVALUATION PURPOSES ONLY. It is provided as a sample IC pre-soldered to a printed circuit board to make it easier to access inputs, outputs, and supply terminals. This evaluation board may be used with any development system or other source of I/O signals by simply connecting it to the host MCU or computer board via off-the-shelf cables. This evaluation board is not a Reference Design and is not intended to represent a final design recommendation for any particular application. Final device in an application will be heavily dependent on proper printed circuit board layout and heat sinking design as well as attention to supply filtering, transient suppression, and I/O signal quality.

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3 Getting started

The NXP analog product development boards provide an easy-to-use platform for evaluating NXP products. These development boards support a range of analog, mixed-signal, and power solutions. These boards incorporate monolithic integrated circuits and system-in-package devices that use proven high-volume technology. NXP products offer longer battery life, a smaller form factor, reduced component counts, lower cost, and improved performance in powering state-of-the-art systems.

The tool summary page for FRDMGD3100HBIEVM is at http://www.nxp.com/FRDMGD3100HBIEVM. The overview tab on this page provides an overview of the device, a list of device features, a description of the kit contents, links to supported devices and a **Get Started** section.

The **Get Started** section provides information applicable to using the FRDMGD3100HBIEVM.

1. Go to http://www.nxp.com/FRDMGD3100HBIEVM.
2. On the **Overview** tab, locate the **Jump To** navigation feature on the left side of the window.
3. Select the **Get Started** link.
4. Review each entry in the **Get Started** section.
5. Download an entry by clicking on the linked title.

After reviewing the **Overview** tab, visit the other related tabs for additional information:

- **Documentation**: Download current documentation.
- **Software & Tools**: Download current hardware and software tools.
- **Buy/Parametrics**: Purchase the product and view the product parametrics.

After downloading files, review each file, including the user guide, which includes setup instructions. If applicable, the bill of materials (BOM) and supporting schematics are also available for download in the **Get Started** section of the **Overview** tab.

3.1 Kit contents/packing list

The FRDMGD3100HBIEVM kit contents include:

- Half-bridge gate driver board (FRDMGD3100HBIEVB)
- Logic translator board (KITGD3100TREVB) attached to FRDM-KL25Z
- USB cable, type A male/type mini B male, 3 ft
- Quick start guide

3.2 Required equipment

To use this kit, you will also need:

- Infineon IGBT FS820R08A6P2B Hybrid PACK Drive
- DC link capacitor compatible with IGBT
  – SBE Power Ring 700A186 500 µF, 500 V DC
- 50 mil jumpers for configuration
- 30 µH to 50 µH, high current air core inductor for double pulse testing
- HV power supply with protection shield and hearing protection
- 25 V, 1.0 A DC power supply
- Pulse generator

- TEK MSO 4054 500 MHz 2.5 GS/s 4-channel oscilloscope
- Rogowski coil, PEM Model CWT Mini HF60R or CTW Mini HF30 (smaller diameter)
- Two isolated high voltage probes (CAL Test Electric CT2593-1, LeCroy AP030)
- Four low voltage probes
- Two digital voltmeters

3.3 System requirements

The kit requires the following to function properly with the software:

- Windows 7 or higher operating system

4 Getting to know the hardware

4.1 Overview

The FRDMGD3100HBIEVM is a half-bridge evaluation kit populated with two GD3100 single channel IGBT gate drive devices on a half-bridge evaluation board. The kit includes the Freedom KL25Z microcontroller hardware for interfacing a PC installed with SPIGen software for communication to the SPI registers on the GD3100 gate drive devices in either daisy chain or standalone configuration.

The GD3100 translator board is used to translate 3.3 V signals to 5.0 V signals between the MCU and GD3100 gate drivers. The evaluation kit can be connected to a single phase of an Infineon Hybrid PACK Drive IGBT module for half-bridge evaluations and applications development.

4.2 Board features

- Capability to connect to Infineon Hybrid PACK Drive IGBT module for half-bridge evaluations
- SPI communication, capable of daisy chain or normal
- Software configurable power and fail-safe controls
- Easy access power, ground and signal test points
- Easy to install and use SPIGen GUI for interfacing via SPI through PC. Software includes double pulse and short-circuit testing capability
- DC link bus voltage monitor on low-side driver via AMUXIN and AOUT

4.3 Device features

Table 1. Device features

Device	Description	Features
GD3100	The GD3100 is an advanced single channel gate driver for IGBTs.	• Compliant with ASIL C/D ISO 26262 functional safety requirements • SPI interface for safety monitoring, programmability and flexibility • Compatible with current sense and temp sense IGBTs • DESAT detection capability for detecting V_{CE} desaturation condition • Fast short-circuit protection for IGBTs with current sense feedback • Integrated Galvanic signal isolation • Integrated gate drive power stage capable of 15 A peak source and sink • Interrupt pin for fast response to faults • Compatible with negative gate supply • Complimentary PWM/PWMALT controls for dead time insertion • Independent fail-safe enable and fail-safe state controls • Compatible with 200 V to 1700 V IGBTs, power range > 125 kW

4.4 Board description

The FRDMGD3100HBIEVM is a half-bridge evaluation board populated with two GD3100 single channel IGBT gate drive devices. The board supports connection to a FRDM-KL25Z microcontroller for SPI communication and programming, through the use of a logic translator board. The board includes DESAT circuitry for short-circuit detection and implementation of GD3100 IGBT shutdown protection capabilities.

The evaluation board is designed to connect to a single phase of an Infineon Hybrid PACK Drive IGBT for evaluation of the GD3100 performance and capabilities.

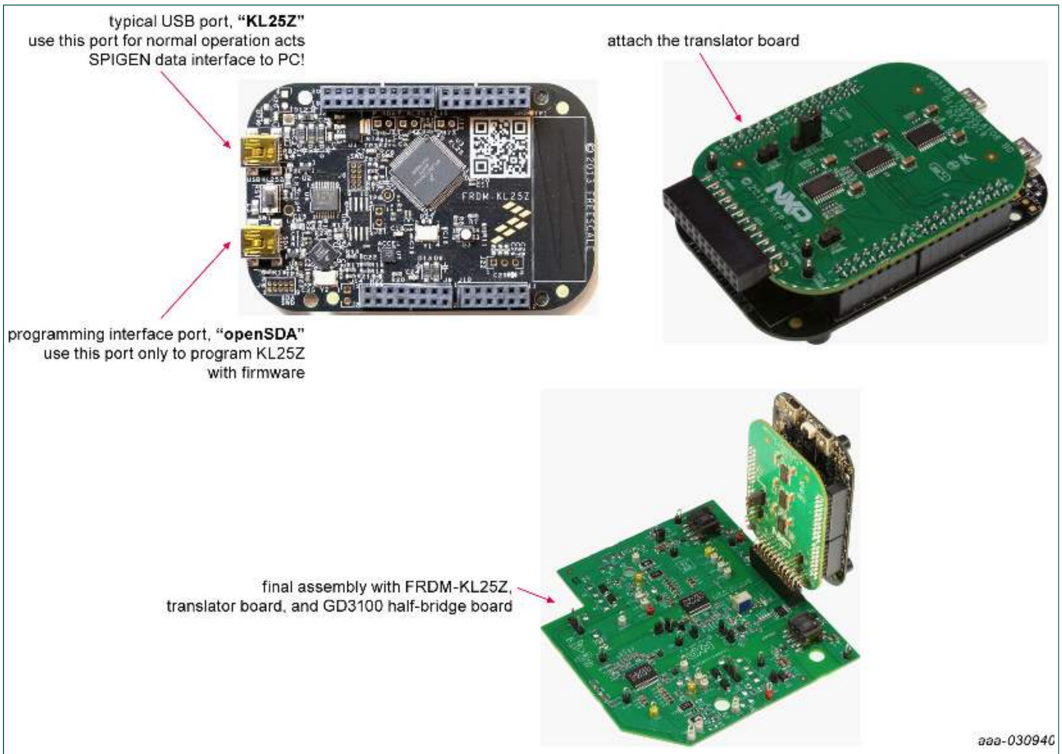

Figure 2. Connecting FRDM-KL25Z, GD3100 half-bridge EVB and translator board

4.4.1 Low-voltage logic and controls connector

Low-voltage domain is 12 V VSUP/VPWR domain that interfaces with the MCU and GD3100 control registers through the 24-pin connector interface.

Low-side driver and high-side driver domains are driver control interfaces to IGBT single phase connections and test points.

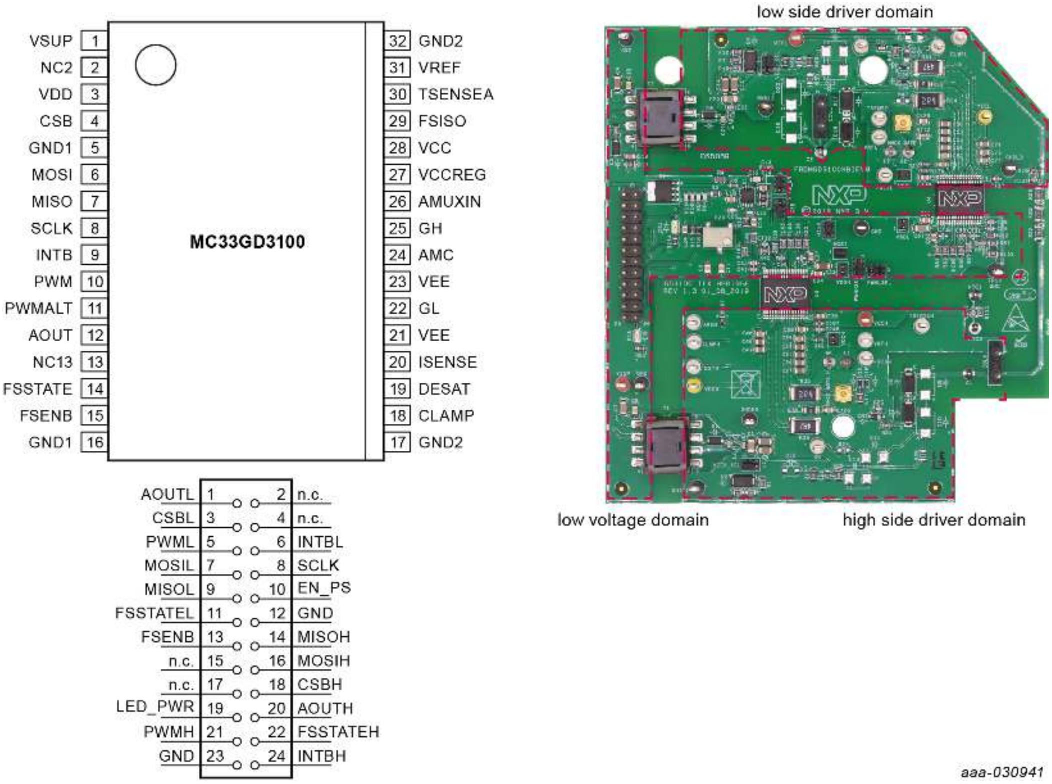

Figure 3. Evaluation board voltage and interface domains

Table 2. Low-voltage (LV) domain 24-pin connector definitions

Pin	Name	Function
1	AOUTL	Duty cycle encoded signal (low-side)
2	n.c.	No connection
3	CSBL	Chip select bar (low-side)
4	n.c.	No connection
5	PWML	PWM input (low-side)
6	INTBL	Interrupt bar (low-side)
7	MOSIL	Master out slave in (low-side)
8	SCLK	Serial clock input
9	MISOL	Master in slave out (low-side)
10	EN_PS	Enable power supplies for VCC/VEE
11	FSSTATEL	Fail-safe state (low-side)
12	GND	Ground
13	FSENB	Fail-safe enable (high-side and low-side)
14	MISOH	Master in slave out
15	n.c.	No connection
16	MOSIH	Master out slave in
17	n.c.	No connection
18	CSBH	Chip select bar (high-side)
19	LED_PWR	3.3 V supply for INTB LEDs (high-side and low-side)

Pin	Name	Function
20	AOUTH	Duty cycle encoded signal (high-side)
21	PWMH	PWM input (high-side)
22	FSSTATEH	Fail-safe state (high-side)
23	GND	Ground
24	INTBH	Interrupt bar (high-side)

4.4.2 Test point definitions

All test points are clearly marked on the evaluation board. Figure 4 shows the location of various test points.

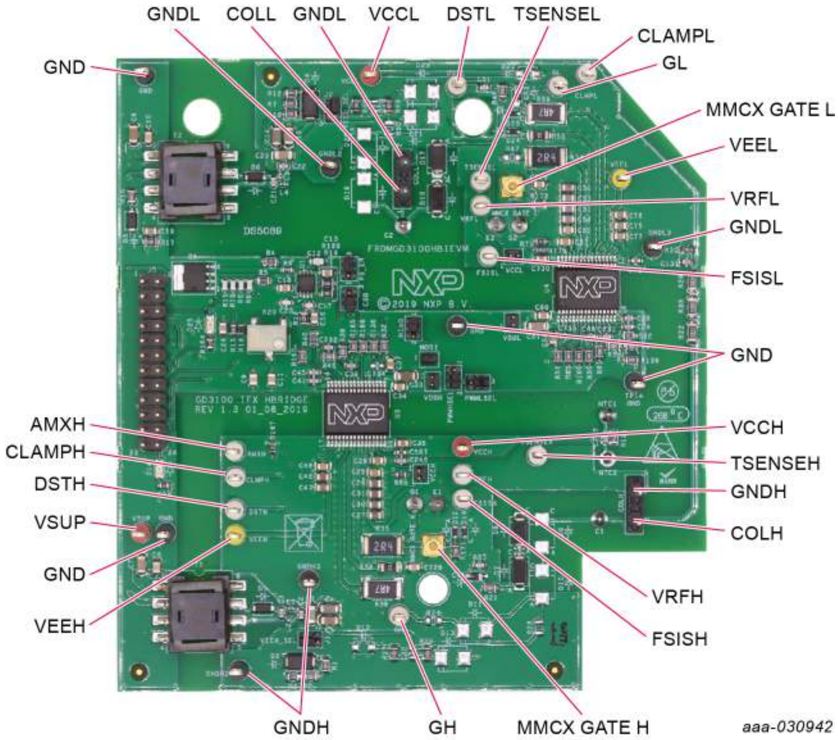

Figure 4. Key test point locations

Table 3. Driver board test point definitions

Test point	Reference designator	Definition
Low voltage (LV) domain		
VSUP	TP2	DC voltage source connection point for VSUP power input of GD3100 devices and flyback power supplies. Typically supplies by vehicle battery +12 V DC, but can also be configured for +5 V DC operation.
GND	TP13, TP14, TP15, TP16	Grounding points for low-voltage domain
Low-side (LS) driver domain		
VCCL	TP17	Provides access to measure positive voltage supply powering HV die and gate driver for low-side IGBT

Test point	Reference designator	Definition
VRFL	TP18	Monitor internal 5.0 V reference for analog circuitry on HV isolated die
TSENSEL	TP19	Input for low-side IGBT temperature measurement. Onboard components optimized for use with NTC.
FSISL	TP20	Initiate fail-safe state control from HV domain for low-side driver
GL	TP21	Test point providing direct measurement of low-side IGBT gate
MMCX GATE L	J23	50 Ω connector (MMCX) providing direct measurement of low-side IGBT gate
DSTL	TP22	VCE desaturation test point connected to low-side driver DESAT pin and circuitry
CLMPL	TP23	VCE sense test point connected to low-side driver clamp pin and circuitry
VEEL	TP24	Negative voltage supply test point for low-side driver gate of IGBT
GNDL	TP25, TP26	Isolated low-side driver ground point. Connected to low-side IGBT emitter
COLL	J27	Two-post header provides direct access to measure VCE for low-side IGBT
High-side (HS) driver domain		
VCCH	TP1	Provides access to measure positive voltage supply powering HV die and gate driver for high-side IGBT
VRFH	TP3	Monitor internal 5.0 V reference for analog circuitry on HV isolated die
TSENSEH	TP4	Input for high-side IGBT temperature measurement. Onboard components optimized for use with NTC
FSISH	TP5	Initiate fail-safe state control from HV domain for high-side driver
AMXH	TP6	Test point for analog MUX input for high-side driver
GH	TP7	Test point providing direct measurement of high-side IGBT gate
MMCX GATE H	J21	50 Ω connector (MMCX) providing direct measurement of high-side IGBT gate
DSTH	TP8	VCE desaturation test point connected to high-side driver DESAT pin and circuitry
CLMPH	TP9	VCE sense test point connected to high-side driver clamp pin and circuitry
VEEH	TP10	Negative voltage supply test point for high-side driver gate of IGBT
GNDH	TP11, TP12	Isolated high-side driver ground point. Connected to high-side IGBT emitter and low-side IGBT collector
COLH	J28	Two-post header provides direct access to measure VCE for high-side IGBT

4.4.3 Power related jumpers configuration

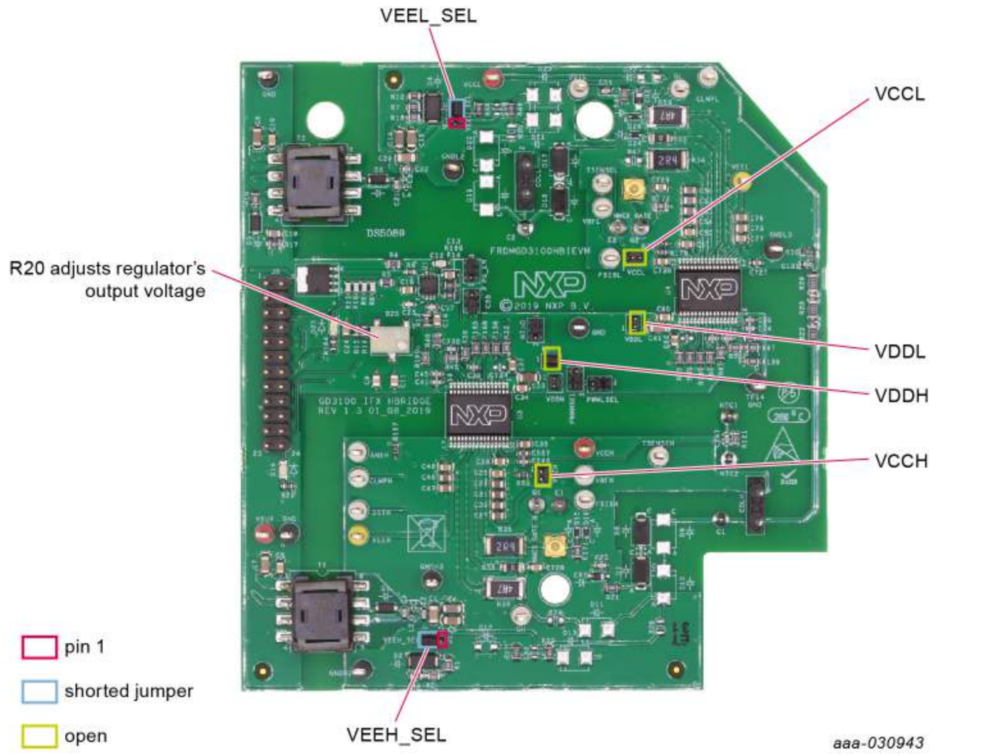

Figure 5. Power supply and jumpers configuration

Table 4. Power related jumper definitions

Jumper	Reference designator	Position	Function
VDDL	J33	Open	VDD-VSUP are separate. Device powered from VSUP, VDD uses internal regulator (default)
		Closed	VDD-VSUP connected. VDD internal regulator bypassed. Device powered by external 5.0 V.
VCCL	J6	Open	VCC regulator (VCCREG) active, gate driver (GH) uses VCCREG (default)
		Closed	VCC regulator (VCCREG) disabled, gate driver (GH) uses VCC
VEEL_SEL	J2	1-2	VEE is negative supply (default)
		2-3	VEE is tied to IGBT emitter (GNDISOL)
		Open	Not allowed. VCC and VEE float relative to IGBT emitter (GNDISOL).
VDDH	J29	Open	VDD-VSUP are separate. Device powered from VSUP, VDD uses internal regulator (default)
		Closed	VDD-VSUP connected. VDD internal regulator bypassed. Device powered by external 5.0 V.
VCCH	J3	Open	VCC regulator (VCCREG) active, gate driver (GH) uses VCCREG (default)
		Closed	VCC regulator (VCCREG) disabled, gate driver (GH) uses VCC

Jumper	Reference designator	Position	Function
VEEH_SEL	J1	1-2	VEE is negative supply (default)
		2-3	VEE is tied to IGBT emitter (GNDISOH)
		Open	Not allowed. VCC and VEE float relative to IGBT emitter (GNDISOH)

The FRDMGD3100HBIEVM provides configurability for different gate driver power architectures. Steps for some common configurations are summarized below. The jumper functionalities are detailed in Table 4.

4.4.3.1 Configuring power delivery to GD3100

To configure GD3100 for 12 V power - open VDD, provide 12 V to VSUP connection (default):

- Open VDDH (J29) jumper
- Open VDDL (J6) jumper
- Connect 12 V to VSUP (TP2)

To configure GD3100 for 5.0 V power - short VDD to VSUP, provide 5.0 V to VSUP connection:

- Short VDDH (J29) jumper
- Short VDDL (J6) jumper
- Connect 5.0 V to VSUP (TP2)

4.4.3.2 Configuring VEE for gate drive (GL)

To configure for negative VEE, provided by onboard zener network (default):

- Connect VEEH_SEL (J1) jumper to 1-2
- Connect VEEL_SEL (J2) jumper to 1-2
- VEE for high-side provided by Zener (D2) and bias resistors (R2, R3)
- VEE for low-side provided by Zener (D4) and bias resistors (R12, R7)

To configure for VEE = 0 V, VEE tied to IGBT emitter:

- Connect VEEH_SEL (J1) jumper to 2-3
- Connect VEEL_SEL (J2) jumper to 2-3
- Tune VCC-VEE output voltage (high and low sides) with feedback resistor (R20)

4.4.3.3 Configuring VCC for gate drive (GH)

To utilize internal VCC regulator (VCCREG = ~15 V) for gate drive (default):

- Open VCCH (J3) jumper
- Open VCCL (J6) jumper
- Ensure VCCREG is fixed around 15 V above isolated GNDH, GNDL

To disable VCC regulator, drive gate directly from VCC:

- Short VCCH (J3) jumper
- Short VCCL (J6) jumper
- Tune VCC-GNDx output voltage (high and low sides) with feedback resistor (R20)

4.4.4 Signal related jumpers and configuration

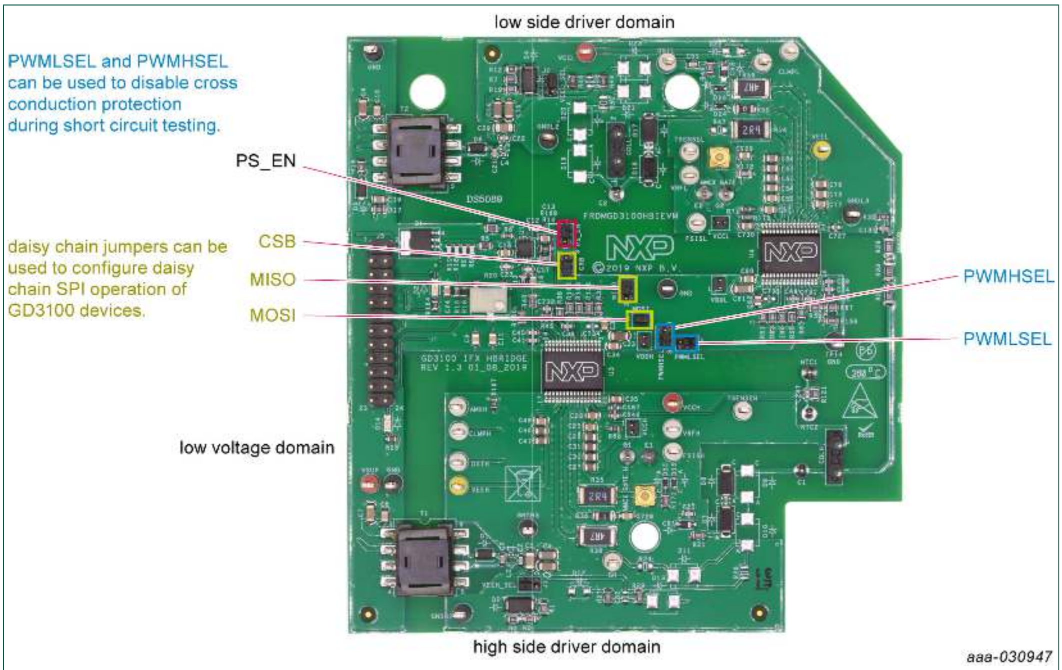

Figure 6. Signal related jumper locations

Table 5. Signal related jumper configurations

Jumper	Reference designator	Position	Function
PS_EN	J25	1-2	MCU/software controls VCC/VEE power supply
		2-3	VCC/VEE power supplies always enabled. MCU control signal is disconnected (default).
		Open	Passive pulldown (R14) disables VCC/VEE power supplies
CSB	J34	1-2	Separate CSBH and CSBL. Use for normal mode (default)
		2-3	CSBH and CSBL tied together. Use for daisy chain.
		Open	Not allowed. Only CSBL will be active, not recommended for normal use.
MISO	J35	1-2	MISOL is passed directly to MCU. Use for normal SPI mode. (default)
		2-3	MISOL is passed to MOSIH. Use for daisy-chain SPI mode.
		Open	Not allowed. MISOL is not routed anywhere for valid communication.
MOSI	J30	Closed	MOSIH is routed directly to MCU. Use for normal SPI mode (default)
		Open	MOSIH receives MISOL signal. Use for daisy-chain SPI mode.

Jumper	Reference designator	Position	Function
PWMLSEL	J31	1-2	PWMALTL receives complementary PWMH signal. Enables dead time protection (default).
		2-3	PWMALTL is grounded. Bypasses dead time control (i.e. double-pulse, short-circuit test).
		Open	Not allowed. PWMALTL is in an unknown state.
PWMHSEL	J32	1-2	PWMALTH receives complementary PWML signal. Enables dead time protection (default).
		2-3	PWMALTH is grounded. Bypasses dead time control (i.e. double-pulse, short-circuit test).
		Open	Not allowed. PWMALTH is in an unknown state.

The FRDMGD3100HBIEVM provides configurability for accessing the GD3100 under a few different controls schemes. Some common configurations are summarized below, along with steps to adapt the driver board are described. The jumper functionalities are detailed in Table 5.

4.4.4.1 SPI configuration options

To configure for normal SPI; low and high side GD3100s are addressable separately (default):

- Set CSB (J34) jumper to 1-2
- Set MISO (J35) jumper to 1-2
- Short MOSI (J30) jumper
- From SPIGen, “SPI0” addresses low-side GD3100 (U4) with CSBL; use “SPI1” to address high-side GD3100 (U3) with CSBH.

To configure both GD3100 in daisy-chain configuration:

- Set CSB (J34) jumper to 2-3
- Set MISO (J35) jumper to 2-3
- Open MOSI (J30) jumper
- From SPIGen, use “SPI0” to address both devices in daisy-chain configuration; “SPI1” will be inactive.

4.4.4.2 Configuring dead time application in hardware

To enable dead time and cross-conduction protection, PWMALT receives complimentary signals (default):

- Set PWMHSEL (J32) to 1-2
- Set PWMLSEL (J31) to 1-2

To bypass dead time insertion (set PWMALT = 0) for specialized testing:

- Set PWMHSEL (J32) to 2-3
- Set PWMLSEL (J31) to 2-3

4.4.4.3 Setting method of power supply control (VCCx, VEEx)

VCC and VEE flyback controllers are always ON (default):

- Connect PS_EN (J25) jumper to 2-3

Allow control to turn VCC/VEE flyback supplies ON/OFF:

- Connect PS_EN (J25) jumper to 1-2
- Utilize EN_PS signal (J5.10) to enable or disable the power supplies

4.4.5 Bottom view

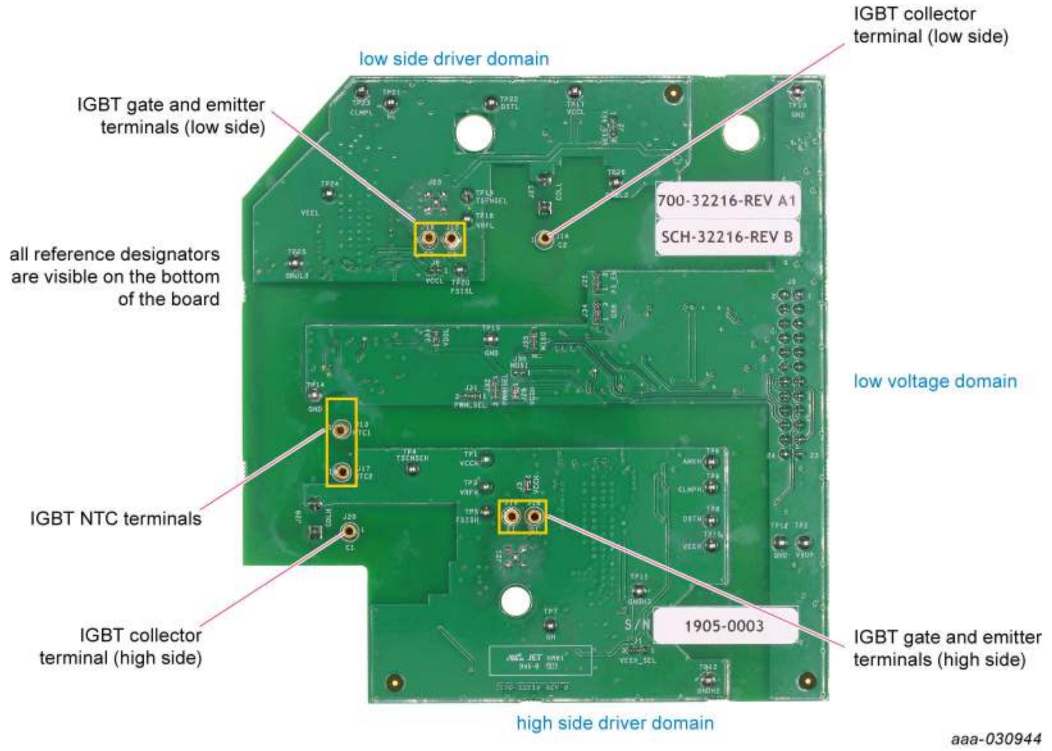

Figure 7. GD3100 evaluation board bottom view

4.4.6 Gate drive resistors

- RGH - gate high resistor in series with the GH pin at the output of the GD3100 high-side driver and IGBT gate that controls the turn-on current for IGBT gate.
- RGL - gate low resistor in series with the GL pin at the output of the GD3100 low-side driver and IGBT gate that controls the turn-off current for IGBT gate.
- RAMC - series resistor between IGBT gate and AMC input pin of the GD3100 high-side/low-side driver for gate sensing and Active Miller clamping.

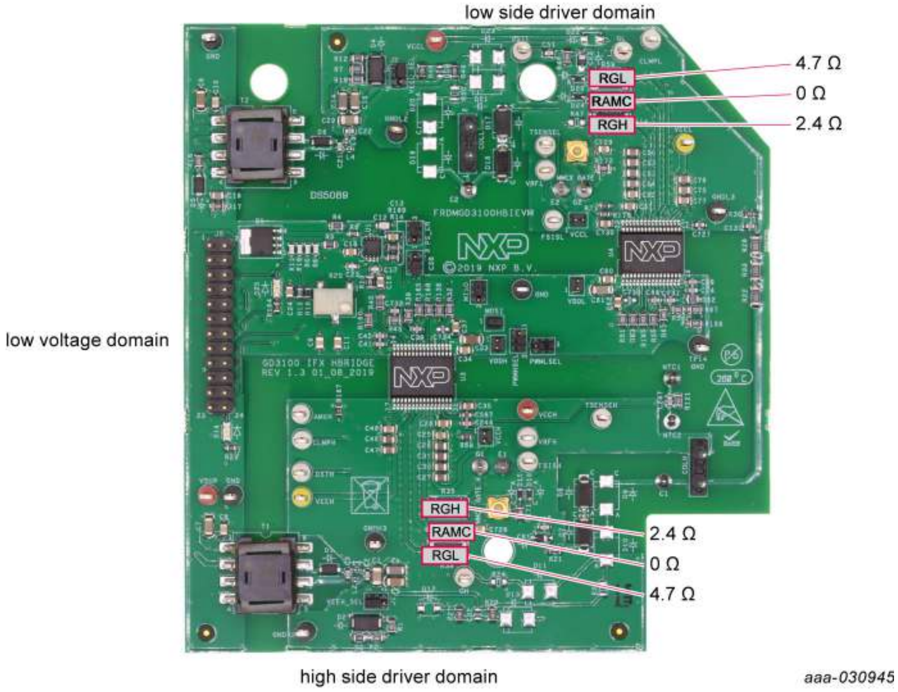

Figure 8. Gate drive resistors

4.4.7 LED interrupt indicators

Interrupt LEDs are provided to visually alert the user of a reported fault. The LEDs are supplied with 3.3 V from the KL25Z, and are driven directly by the INTB pin of the respective GD3100 device. A 220 Ω resistor is used for current limiting.

- D14 (INTBH) LED is ON while fault is being reported (INTB low). LED is OFF while no fault is reported (INTB high).
- D25 (INTBL) LED is ON while fault is being reported. LED is OFF while no fault is reported (INTB high).

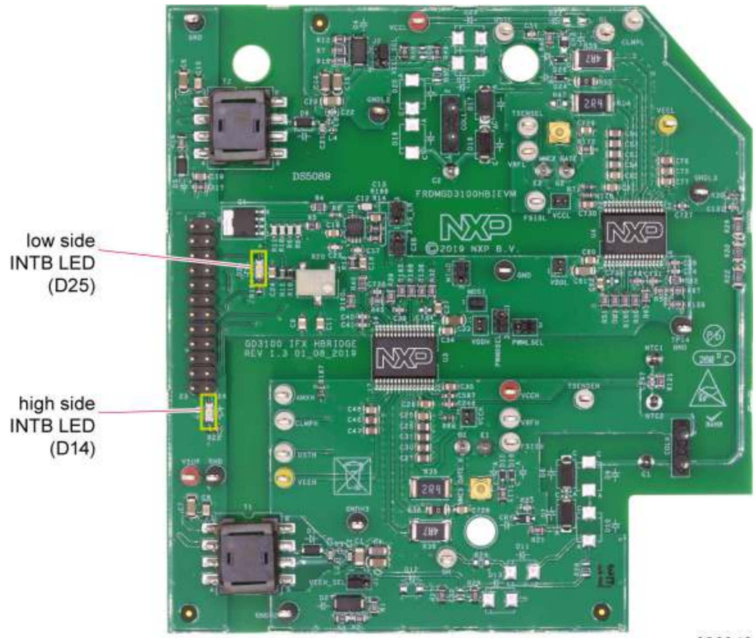

Figure 9. LED interrupt indicators

Table 6. Interrupt LED definitions

LED	Reference designator	Description
Low-side INTB	D25	Connected to the INTB output pin (active low) of low-side GD3100 • LED is ON: indicates reported fault, check system • LED is OFF: indicates no reported fault
High-side INTB	D14	Connected to the INTB output pin (active low) of high-side GD3100 • LED is ON: indicates reported fault, check system • LED is OFF: indicates no reported fault

4.5 Kinetis KL25Z freedom board

The Freedom KL25Z is an ultra-low-cost development platform for Kinetis® L Series MCU built on Arm® Cortex®-M0+ processor.

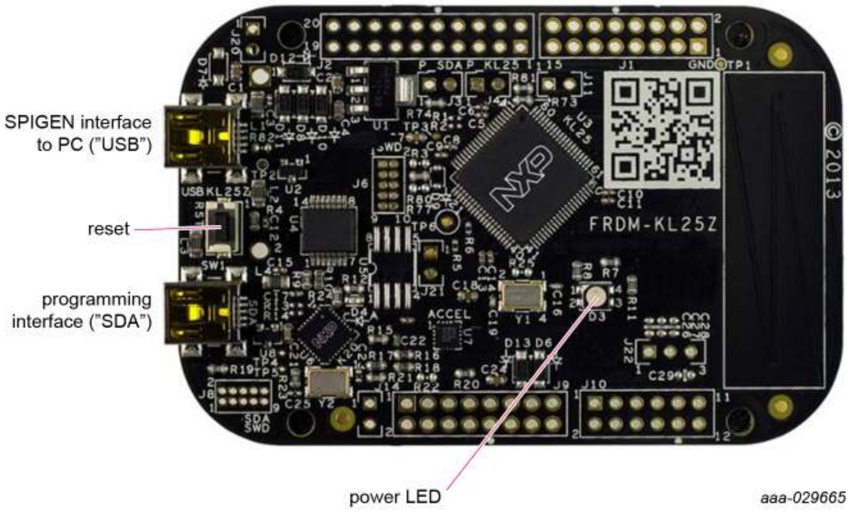

Figure 10. Freedom Development Platform

4.6 Logic translator board

The FRDMGD3100HBIEVM includes a logic translator board, which provides simple isolation and is capable of level-shifting communication signals between the MCU and the GD3100 driver board. The driver board is exposed to high voltage, and may require 3.3 V or 5.0 V logic, necessitating an interface board.

Various signals, like the SPI communication, interrupt, fail-safe controls, and PWM pass through the translator board. The translator board provides a configurable output voltage (3.3 V or 5.0 V) going out to the GD3100 driver board.

The translator board also provides the choice of using PWM signals from the MCU, or wiring in an external control from a function generator. Jumper configurations are explained in Figure 11 and Table 7. Test points are reviewed in Table 8.

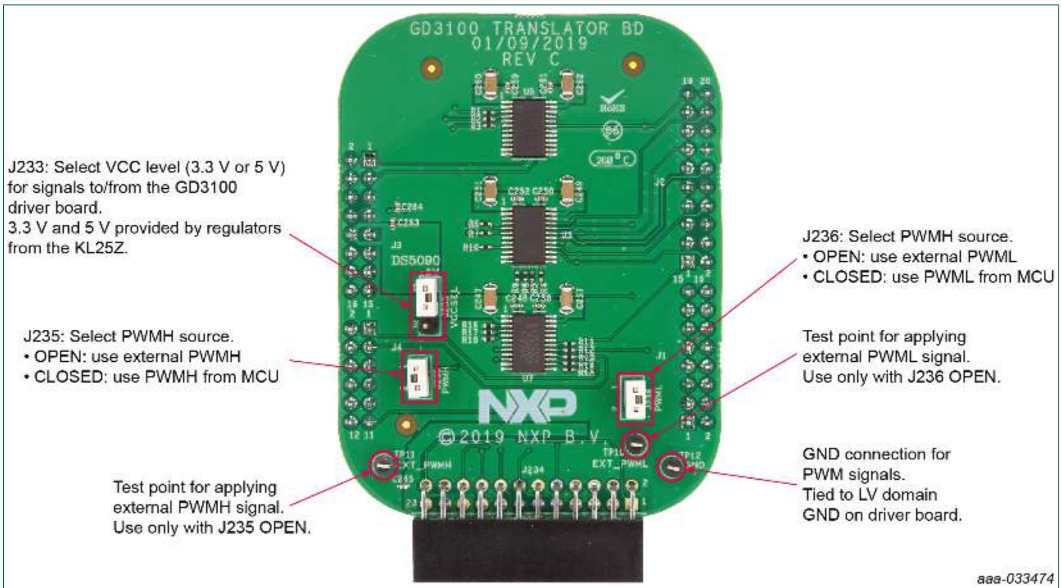

Figure 11. Logic translator board

Table 7. Translator board jumper functionality

Jumper	Reference designator	Position	Function
VCCSEL	J233	1-2	5.0 V regulator from KL25Z powers all translator VCC, 5.0 V signals to/from the driver board (default) • Use with 5.0 V GD3100 (MC33GD3100EK)
		2-3	3.3 V regulator from KL25Z powers all translator VCC, 3.3 V signals to/from the driver board • Use with 3.3 V version of GD3100 (MC33GD3100A3EK)
		Open	Not allowed. There is no power provided to logic translators, and no signals will be passed to the driver board. • Provide external power to J233, pin 2 (max 5.5 V) to enable communications
PWMH	J235	Closed	PWMH signal from MCU is passed to the driver board (default)
		Open	External signal for PWMH must be provided at EXT_PWMH (TP11)
PWML	J236	Closed	PWML signal from MCU is passed to the driver board (default)
		Open	External signal for PWML must be provided at EXT_PWML (TP10)

Table 8. Translator board test point definition

Test point	Reference designator	Definition
EXT_PWML	TP10	PWML signal provided to driver board
EXT_PWMH	TP11	PWMH signal provided to driver board
GND	TP12	GND connection for translator, also connected to GND on LV domain of driver board

The translator board in FRDMGD3100HBIEVM supports different configurations for various application tests. The translator supports PWM from either the KL25Z (see Section 4.6.1 "Configuring the translator for KL25Z-controlled PWM") or from external source (see Section 4.6.2 "Configuring the translator for external PWM control"), one of these implementations will be used in testing. Similarly, based on the GD3100 device populated, the translator will need to support either 5.0 V logic (see Section 4.6.3 "Configuring the translator for 5.0 V logic operation") or 3.3 V logic (see Section 4.6.4 "Configuring the translator for 3.3 V logic operation").

4.6.1 Configuring the translator for KL25Z-controlled PWM

By default, the translator is setup to send PWM signals generated on the KL25Z out to the driver board. These signals pass through the translator and are level-shifted according to the translator’s own configuration. Test points EXT_PWML (TP10) and EXT_PWMH (TP11) are available to monitor commanded PWM state.

To configure the translator board for KL25Z-controlled PWM, perform the following:

1. Short PWMH (J235) jumper.
2. Short PWML (J236) jumper.
3. Use SPIGen to apply double-pulse, short-circuit, or PWM waveforms.

4.6.2 Configuring the translator for external PWM control

The translator may be setup to pass externally provided signals to the driver board, normally applied at EXT_PWML (TP10) and EXT_PWMH (TP11) test points. These signals do not pass through the translator, so their logic level must match those required by the GD3100 populated on the driver board.

To configure the translator board for external PWM control, perform the following:

1. Open PWMH (J235) jumper.
2. Open PWML (J236) jumper.
3. Apply desired PWM function between EXT_PWML (TP10) and GND (TP12).
4. Apply desired PWM function between EXT_PWMH (TP11) and GND (TP12).

4.6.3 Configuring the translator for 5.0 V logic operation

This configuration is for use with the 5.0 V gate driver device (MC33GD3100EK) populated on the driver board. The attached KL25Z has a 5.0 V supply (drawn from USB power bus) that is pinned out to the translator for this purpose.

To configure the translator board to send/receive 5.0 V logic level signals, perform the following:

1. Set VCCSEL (J233) jumper to 1-2.

4.6.4 Configuring the translator for 3.3 V logic operation

This configuration is for use with the 3.3 V gate driver device (MC33GD3100A3EK) populated on the driver board. The attached KL25Z has a 3.3 V regulator onboard that is pinned out to the translator for this purpose.

To configure the translator board to send/receive 3.3 V logic level signals, perform the following:

1. Set VCCSEL (J233) jumper to 2-3.

5 Configuring the hardware

5.1 System setup

FRDMGD3100HBIEVM is connected to any phase of an Infineon Hybrid PACK Drive module with SBE DC Link capacitor as shown in Figure 12. Double pulse and short-circuit testing can be conducted utilizing Windows based PC with SPIGEN software.

Suggested equipments needed for test:

- Rogowski coil high current probe
- High voltage differential voltage probe
- High sample rate digital oscilloscope with probes
- DC link capacitor
- Infineon Hybrid PACK Drive IGBT module
- Windows 7 based PC
- High voltage DC power supply for DC link
- Low voltage DC power supply for VSUP/GD3100PWR
  - +12 V DC gate drive board low voltage domain

- Voltmeter for monitoring high voltage DC Link supply
- Load coil for double pulse and short-circuit type 2 testing

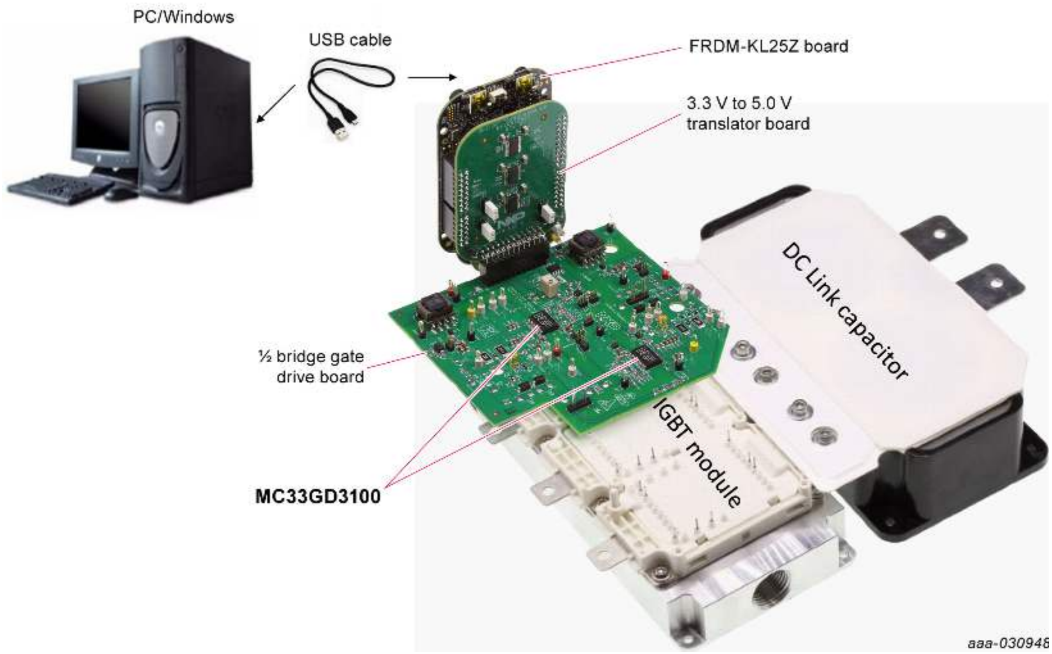

Figure 12. Evaluation board and system setup

5.2 Quick start

5.2.1 Scope and purpose

This section provides comprehensive quick start notes for the FRDMGD3100HBIEVM half-bridge evaluation kit. Within a few minutes the user can install SPIGEN application on a PC, power up the half-bridge evaluation kit, start SPI communication, and pass PWM signals to evaluate working operation.

5.2.2 Intended audience

Experienced engineers evaluating GD3100 gate drive device for IGBT control.

5.2.3 Setting up and connecting the evaluation kit

1. Download and Install latest SPIGEN software – Windows application from NXP.com to your PC (see Section 6.2 "Configuring the FRDM-KL25Z microcode").
2. Assemble the FRDMGD3100HBIEVM with KL25Z micro board and translator board as shown in Figure 2.
3. Check jumper configuration on the evaluation board before powering up, and ensure the configuration meets desired use case.
   a. The default jumper configuration (shipped from factory) is setup normal SPI (non-daisy chain) communication with high-side and low-side driver domains VEE negative supply level active. Also, ensure jumper J233 is populated on Translator board for powering KL25Z micro.

   b. For alternate configurations and setup details, see Section 4.4.3, Section 4.4.4 "Signal related jumpers and configuration", and Section 4.4.7 "LED interrupt indicators".
4. Start SPIGEN application software on PC. Connect USB cable from PC to USBKL25Z port on KL25Z micro board. A successful connection results in a connection successful pop-up (reading "SPI dongle is connected") on the PC with SPIGEN application running.
   a. KL25Z micro shipped with proper firmware is already flashed. See Section 6 "Installation and use of software tools" for additional details.
5. Next supply 12 V DC power to low voltage domain of evaluation board (12 V DC to VSUP connection point and grounding to GND1 connection point on low voltage domain).
6. Check high-side and low-side driver domain regulated voltage level by checking VCCH and VCCL test points for ~17 V DC with respect to grounding to points GNDH and GNDL in each domain respectively.
   a. If voltage level on VCCH and VCCL are low adjust R20 potentiometer for proper level as shown in Figure 5.
7. With proper PC interface connection and voltage levels, SPI communication can be conducted with GD3100 devices over SPIGen as described in Section 6.3 "Using the SPIGEN graphical user interface". See GD3100 data sheet for additional details.
   a. Selecting SPI0 communicates with low-side gate drive device and SPI1 communicates with high-side gate drive device (see Figure 14).
8. Apply PWM signals to each gate drive. Gate drive output can be observed on high-side and low-side driver devices with test points (GH, GL), or 50 Ω port (MMCX GATE H/L).
   a. To receive PWM as provided by the KL25Z, see Section 4.6.1 "Configuring the translator for KL25Z-controlled PWM". Use SPIGen to control, see Section 6.3.4 "Pulse test".
   b. To set up for external PWM control, see Section 4.6.2 "Configuring the translator for external PWM control". Apply a control signal with an external function generator.
9. For double pulse and short-circuit testing with an IGBT and inductive load, use the "Pulse test" view as part of the SPIGen GUI. Set parameterized pulse widths commanded by the KL25Z.
   a. For short-circuit testing, PWMHSEL and PWMLSEL must be configured so as to bypass dead time control (see Section 4.4.4.2 "Configuring dead time application in hardware").

6 Installation and use of software tools

Software for FRDMGD3100HBIEVM is distributed with the SPIGen GUI tool (available on NXP.com). Necessary firmware comes pre-installed on the FRDM-KL25Z with the kit.

Even if the user intends to test under other software or PWM, it is recommended the user install this software below as a backup or in help debugging.

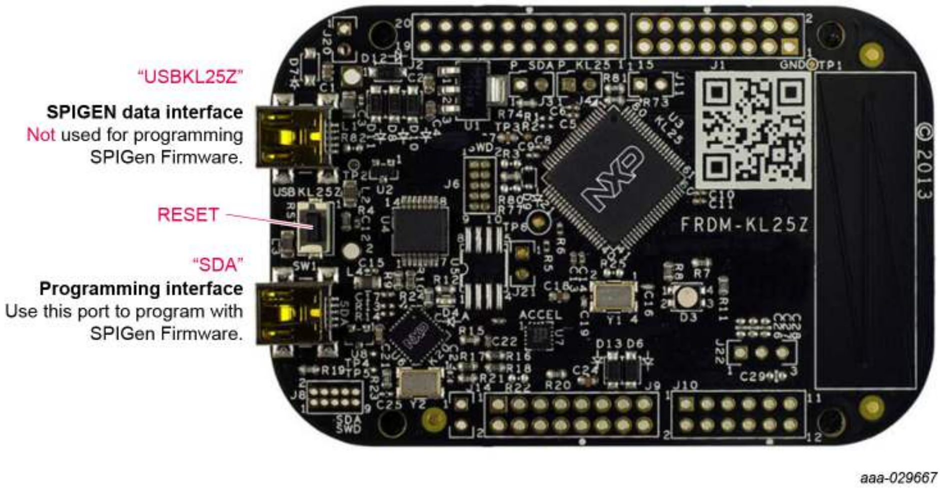

Figure 13. FRDM-KL25Z setup and interface

6.1 Installing SPIGen on your computer

The latest version of SPIGen supports the GD3100 and is designed to run on any Windows 10, Windows 8, or Windows 7-based operating system. To install the software, do the following:

1. Go to www.nxp.com/SPIGen and click **Download**.
2. When the SPIGEN: SPI Generator (SPIGen) software page appears, go to the **Lab and Test Software** section and click **Download** associated with the description of the selected environment. A wizard guides the user through the process.
3. If instructed for the SPIGen wizard to create a shortcut, a SPIGen icon appears on the desktop. By default, the SPIGen executable file is installed at **C:\Program Files (x86)\SPIGen**.
   Installing the device drivers overwrites any previous SPIGen installation and replaces it with a current version containing the GD3100 drivers. However, configuration files (.spi) from the previous version remain intact.

6.2 Configuring the FRDM-KL25Z microcode

By default, the FRDM-KL25Z with this kit is preprogrammed with the current and most up-to-date firmware available for the kit.

A way to quickly check that the microcode is programmed and board is functioning properly, is to plug the KL25Z into the computer, open SPIGen, and verify the software version at the bottom is 5.4.7 software (see Figure 14).

In the event of a loss of functionality following a board reset, reprogramming, or a corrupted data issue, the microcode may be rewritten per the following steps:

1. To clear the memory and place the board in bootloader mode, hold down the reset button while plugging a USB cable into the **OpenSDA** USB port.
2. Verify the board appears as a "BOOTLOADER" device and continue to step 3. If the board appears as KL25Z, you may skip to step 6.
3. Download the **Firmware Apps** .zip archive from the PEMicro OpenSDA web page (http://www.pemicro.com/opensda/). Validate your email address to access the files.

4. Find the most recent MDS-DEBUG-FRDM-KL25Z_Pemicro_v***.SDA and copy/drag-and-drop into the **BOOTLOADER** device.
5. Reboot the board by unplugging and re-plugging the connection to the **OpenSDA** port. Verify now the device appears as a “KL25Z” device to continue.
6. Locate the most recent KL25Z firmware; this is distributed as part of the SPIGen package.
   a. From the SPIGen install directory, this is located in the **SPI Dongle Firmware** folder and is named of the form “UsbSPIDongleKL25Z_GD3100_v***.srec”.
      - When using translator revC, use the firmware version 5.4.7 or later.
      - When using the translator revB, use the firmware version only up to 5.4.6, to maintain backward compatibility and pinout.
   b. This .srec file is a product/family-specific configuration file for FRDM-KL25Z containing the pin definitions, SPI/PWM generation code, and pin mapping assignments necessary to interface with the translator board as part of FRDMGD3100HBIEVM.
7. With the KL25Z still plugged through the **OpenSDA** port, copy/drag-and-drop the .srec file into the KL25Z device memory. Once done, disconnect the USB and plug into the other USB port, labeled **KL25Z**.
   a. The device may not appear as a distinct device to the computer while connected through the KL25Z USB port, this is normal.
8. The FRDM-KL25Z board is now fully set up to work with FRDMGD3100HBIEVM and the SPIGen GUI.
   a. There is no software stored or present on either the driver or translator boards, only on the FRDM-KL25Z MCU board.

All uploaded firmware is stored in non-volatile memory until the reset button is hit on the FRDM-KL25Z. There is no need to repeat this process upon every power up, and there is no loss of data associated with a single unplug event.

6.3 Using the SPIGEN graphical user interface

The SPIGen graphical user interface is available from NXP.com as an evaluation tool demonstrating GD3100-specific functionality, configuration, and fault reporting. SPIGen also includes basic capacity for the FRDMGD3100HBIEVM to control an IGBT, enabling double-pulse or short-circuit testing.

SPI messages can be realized graphically or in hexadecimal format, and the CSB is selectable to address one or both GD3100 present on the board. See Figure 14 for SPIGen graphical user interface for GD3100 internal register read and write access.

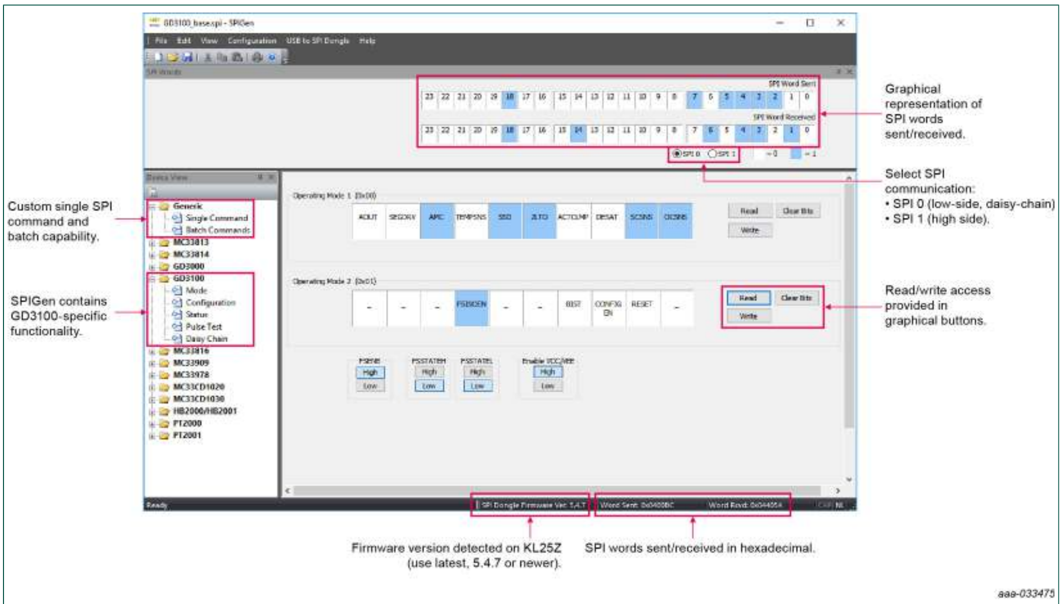

Figure 14. SPIGen general view

Some general guidelines on SPIGen usage:

- When attempting to change operating modes, configuration registers, or status mask bits, ensure the CONFIG_EN bit in the MODE2 register is set to 1. Fault status bits can be cleared without CONFIG_EN being set to 1.
- On Mode, Configuration, and Status views, READ operations send identical back-to-back commands so the response is obtained upon a single click of the “Read” button. This is normal SPI operation, but is implemented this way for the end-user’s convenience.
- On Daisy Chain view, only one READ operation is performed per click. Two READ operations must be performed to obtain response data.
- On all views, WRITE operations are only performed once per click.

6.3.1 Mode registers

See Figure 15 for an overview of control options available on the “Mode” view on SPIGen. See GD3100 data sheet for a complete description of MODE1 and MODE2 registers and pin functionalities. The onboard flyback power supply providing VCC and VEE for the HV domains can be enabled (default) or disabled in the event and external supply or characteristic is desired.

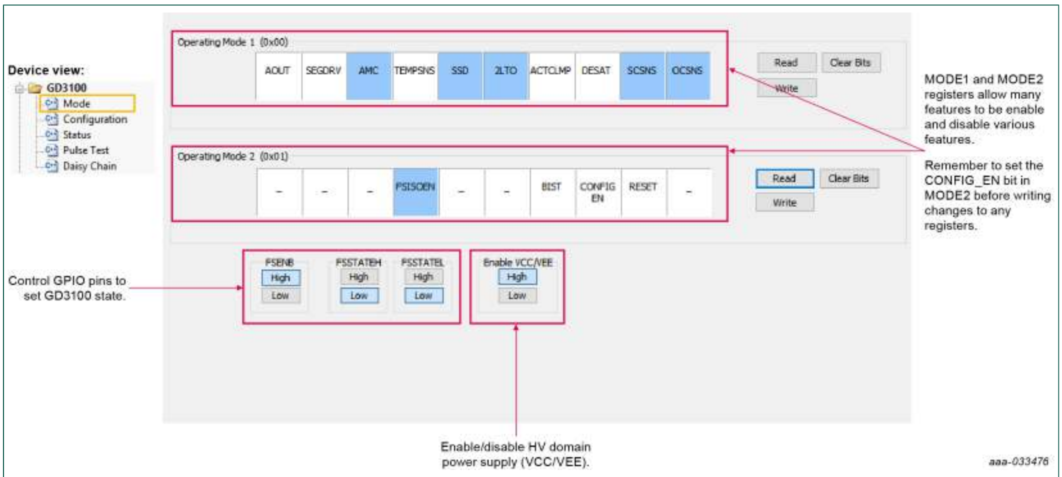

Figure 15. Mode registers and GPIO controls view

6.3.2 Configuration register

See GD3100 data sheet for configuration SPI register descriptions.

When attempting to change configuration parameters, ensure the CONFIG_EN bit in the MODE2 register is set to 1. READ operations send identical back-to-back commands so the response is obtained upon a single click of the **Read** button. WRITE operations are only performed once per click.

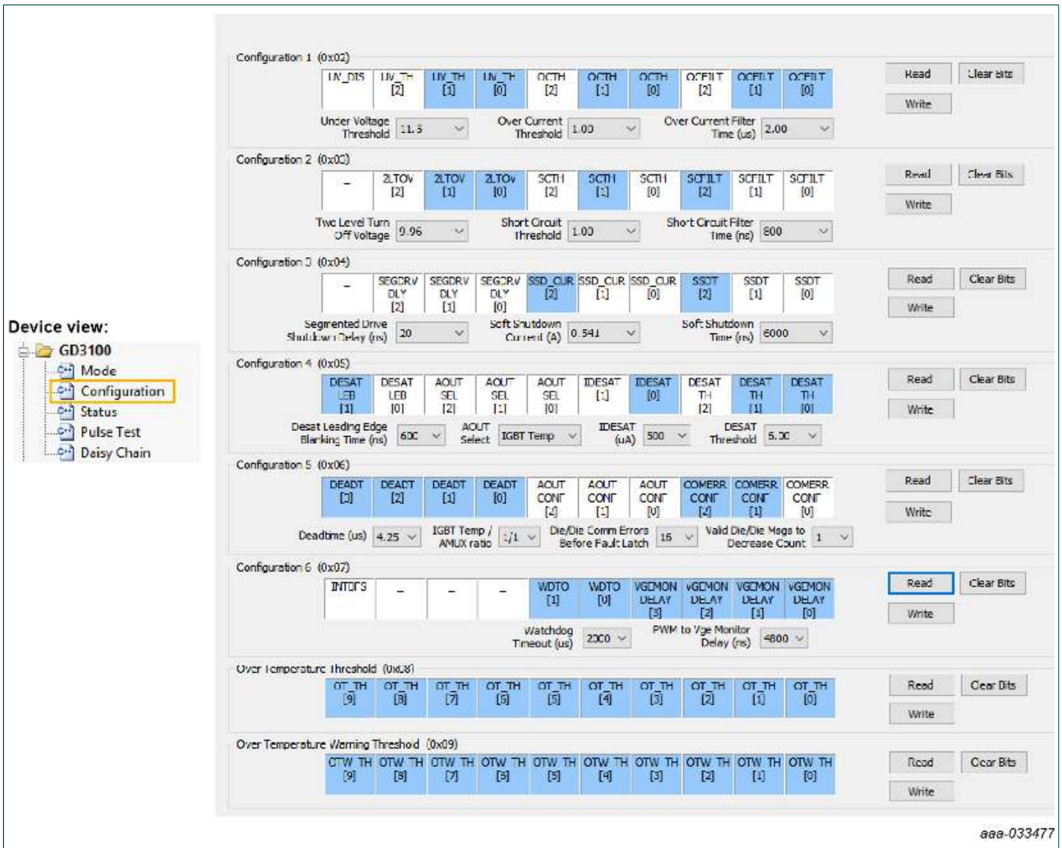

Figure 16. Configuration registers view

6.3.3 Status and mask register

See GD3100 data sheet for status and mask SPI register descriptions. INTB indicators mirror the status of the INTB pin on both high-side and low-side GD3100 simultaneously, but only one (either high-side or low-side) can be read at a time over SPI (selected by “SPI 0” or “SPI 1”) in this view.

Figure 17. Status, mask, and REQADC registers view

6.3.4 Pulse test

The Pulse test view allows a few simple waveforms to be applied to the PWM and PWMALT pins, to evaluate with an IGBT.

For double pulse test, short-circuit test, and short-circuit test 2, it is recommended to bypass dead time protection, as described in Section 4.4.4.2 "Configuring dead time application in hardware" so the desired pulse is not distorted by the dead time protection.

For a repeating PWM waveform provided by a timer pin on the KL25Z, use the "PWM Controls" to define frequency and duty cycle. The duty cycle is referenced to PMWH (for example, when duty cycle is set at 80 %, PWMH = 80 %, PWML = 20 %).

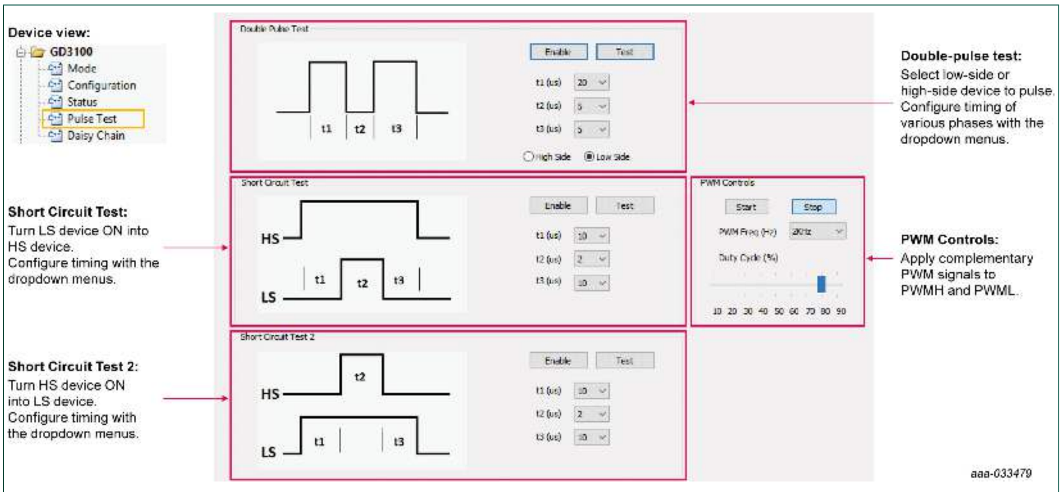

Figure 18. Pulse test view

6.3.5 Daisy chain

When FRDMGD3100HBIEVM is configured for daisy-chain (see Section 4.4.4.1 "SPI configuration options"), both GD3100 devices can be addressed in the same SPI frame. In daisy-chain configuration, both devices will be addressed by “SPI 0”. Neither device will be addressed if “SPI 1” is selected.

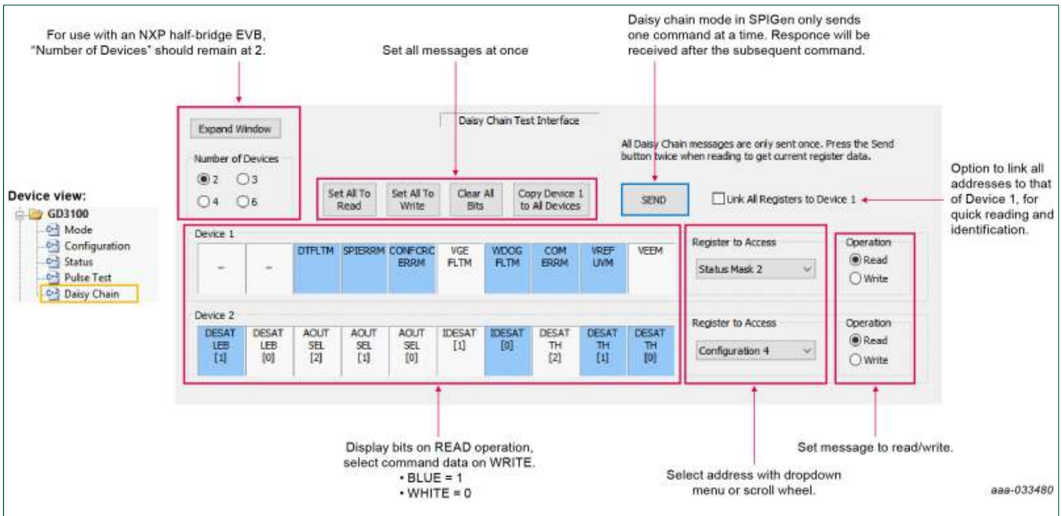

Figure 19. Daisy chain view

6.3.6 Single command

The Single command view contains a log of recent commands, displayed in hexadecimal format. Single SPI commands can be saved and recalled by name. Commands defined here are available for scripting in the Batch commands page. SPI words sent and received (initiated from any tab) are logged here in hexadecimal and can be saved and exported in a text file. Daisy-chain length command structure (n*24 bit length, where n > 1) are not supported by this view.

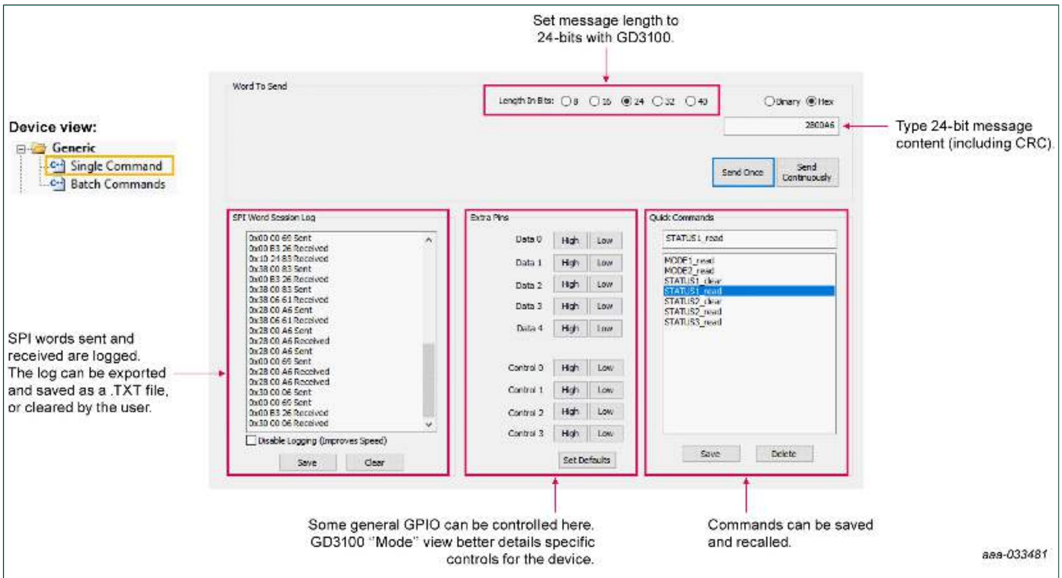

Figure 20. Single command view

6.3.7 Batch command

The Batch commands view allows creation of scripts containing commands defined by the Single command page. Batches can be named, saved, and recalled. This is useful for quickly initializing the device after powering up.

The batch commands sent can be logged and saved in a text file. The SPI words sent/ received can be viewed in hexadecimal and exported back in the Single commands view. Daisy-chain length command structure (n*24 bit length, where n > 1) are not supported by this view.

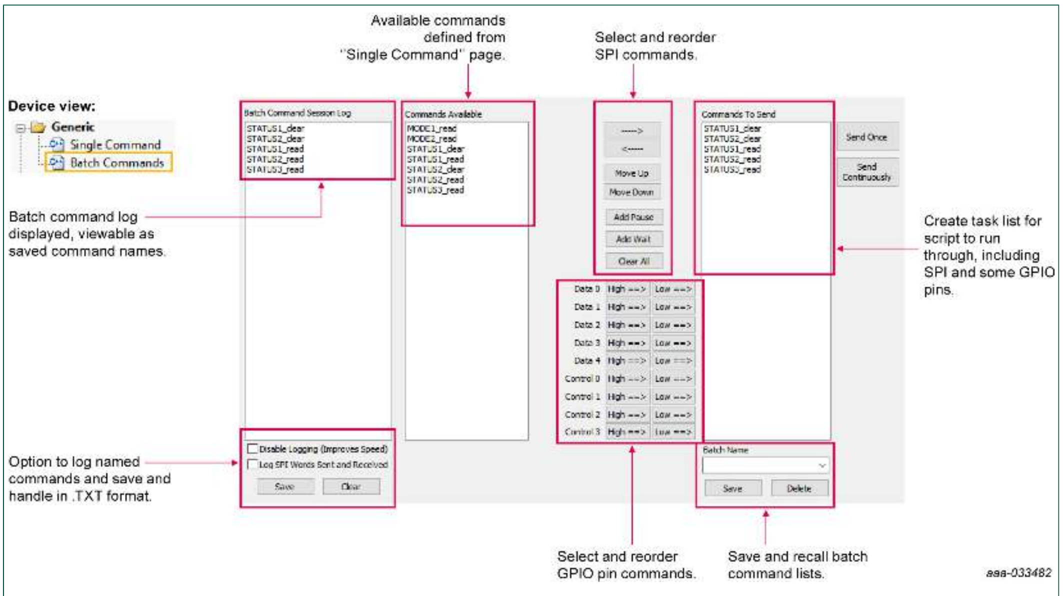

Figure 21. Batch commands view

6.4 Troubleshooting

Some common issues and troubleshooting procedures are detailed below. This is not an exhaustive list by any means, and additional debug may be needed:

Problem	Evaluation	Explanation	Corrective action(s)
No PWM output (no fault reported)	Check PWM jumper position on translator board	Incorrect PWM jumpers obstruct signal path but not report fault	Set PWMH (J235) and PWML (J236) jumpers properly, for desired control method: • KL25Z control configuration reviewed in Section 4.6.1 • External PWM control configuration reviewed in Section 4.6.2
	Check correct firmware is in use for translator board version	Firmware includes pin definitions and pinout for KL25Z corresponding to routing and pin allocation on specific translator board revision	Check firmware version in SPIGen, according to Figure 14. Match this to microcode needed for translator board revision, stated in Section 6.2, step 6.
	Check PWM control signal	Ensure that proper PWM signal is reaching GD3100	Monitor EXT_PWML (TP10) and EXT_PWMH (TP11) for commanded PWM state
	Check FSENB status (see GD3100 pin 15, STATUS3)	PWM is disabled when FSENB=L	Set pin FSENB=H (pin 15) to continue
	Check CONFIG_EN bit (MODE2)	PWM is disabled when CONFIG_EN=1	Write CONFIG_EN=0 to continue
No PWM output (fault reported)	Check VGE fault (VGE_FLT)	A short on IGBT gate, or too low of VGEMON delay setting causes VGE fault, locking out PWM control of the gate.	Clear VGE_FLT bit (STATUS2) to continue. Increase VGEMON delay setting (CONFIG6). If safe operating condition can be guaranteed, set VGE_FLTM (MSK2) bit to 0, to mask fault.
	Check for short-circuit fault (SC) in STATUS1 register	SC is a severe fault that disables PWM. SC fault cannot be masked	Clear SC fault to continue. Consider adjusting SC fault settings on GD3100: • Adjust short-circuit threshold setting (CONFIG2) • Adjust short-circuit filter setting (CONFIG2)

Problem	Evaluation	Explanation	Corrective action(s)
PWM output is good, but with persistent fault reported	Check for dead time fault (DTFLT) in STATUS2 register	Dead time is enforced, but fault indicates that PWM controls signals are in violation	Clear DTFLT fault bit (STATUS2). Check PWMHSEL (J32) and PWMLSEL (J31) are configured to bypass dead time faults. Consider adjusting dead time settings on GD3100: • Change mandatory PWM dead time setting (CONFIG5) • Mask dead time fault (MSK2)
	Check for overcurrent (OC) fault in STATUS1 register	OC fault latches, but does not disable PWM. OC fault cannot be masked.	Clear OC fault bit (STATUS1). Adjust OC fault detection settings on GD3100: • Adjust overcurrent threshold setting (CONFIG1) • Adjust overcurrent filter setting (CONFIG1)
PWM or FSSTATE rising edge has longer delay than falling edge	Check translator output voltage versus GD3100 VDD voltage	Low translator output voltage (compared with correct VDD at GD3100) causes the logic-high threshold at the GD3100 pin to be crossed later than commanded	Check translator output voltage selection (J233) is configured to the same level as the GD3100 VDD Check VCCSEL supply or translator outputs on the translator board for excessive loading or supply droop/ pulldown
WDOG_FLT reported on startup	Check VSUP and VCC are powered	On initialization, watchdog fault is reported when one die is powered up before the other	Check VSUP and VCC both have power applied. Clear WDOG_FLT bit (STATUS2) to continue.
SPIERR reported on startup	Check KL25Z/translator connection	On initialization, SPIERR can occur when the SPI bus is open, or when GD3100 IC is powered up before the translator (which provides CSB).	Clear SPIERR fault to continue. Reinitialize power to GD3100 after translator is powered (over USB).
SPIERR reported after SPI message	Check bit length of message sent	There is SPIERR if SCLK does not see a n*24 multiple of cycles	Use 24-bit message length for SPI messages
	Check CRC	SPIERR faults if CRC provided in sent message is not good	Use SPIGen to generate commands with valid CRC. The command can be copied in binary or hexadecimal and sent from another program.
	Check for sufficient dead time between SPI messages	SPIERR fault bit is set when the time between SPI messages (txfer_ delay) received is too short. Minimum required delay time is 19 µs.	Check time between CSB rising edge (old message end) and CSB falling edge (new message start) during normal SPI read, and ensure transfer delay dead time check. SPIERR can also be cleared in BIST.
VCCREGUV reported on startup	Check VCCREG potential	Caused by low VCC	Clear VCCREGUV fault bit (STATUS1). Tune VCC-GNDISO potential with power supply set resistor (R20).
VREFUV reported on startup	Check HV domain is powered correctly	Related to slow rise time of VCC supply on HV domain, or failed VREF regulator	Clear VREFUV bit (STATUS2). Reset HV domain supply if fault bit does not clear.
	Check VCC for undervoltage condition	Low VCC is visible indirectly through other HV domain faults	Tune VCC-GNDISO using R20 feedback

Problem	Evaluation	Explanation	Corrective action(s)
VCCOV fault reported on startup	Check position of VEEx_SEL (J1, J2) jumpers	VEEx_SEL jumpers set the VCC/VEE potential relative to each HV domain GND	Disable HV domain power supplies, and set correct VEExSEL jumpers. See Section 4.4.3.2 for details. Clear VCCOV bit (STATUS1) to continue.
	Check solder joint integrity of VEEx_ SEL (J1, J2) jumpers and other VEEx-GNDISOx components	VEEx_SEL jumper (J1, J2) short between 2-3, or low-impedance component failure can cause VCC-VEE potential to exceed VCCOV	Remove power. Check VEEx_SEL jumper integrity. Remove jumper and apply continuity check for 2-3 short. Check that Zener diode regulator is valid in diode check.
	Check VCC-GNDISO potential	PWM is disabled during a VCC overvoltage (20 V nom.)	Tune VCC-GNDISO potential to suitable level with power supply set resistor (R20). Clear VCCOV bit (STATUS1) to continue.
No PWM during short circuit test	Check PWMxSEL jumpers	Incorrect configuration of PWMALT pins prevent short-circuit test by enforcing dead time	For short-circuit test, set PWMLSEL (J31) and PWMHSEL (J32) to bypass dead time. See Section 4.4.4.2 for details.
Bad SPI data, appears to repeat previous response	Check VSUP/VDD for undervoltage condition	VDD_UV latches SPI buffer contents, preventing updated fault reporting.	Check voltage provided at VDD pin (pin 3). On each read, compare the address from the sent command and response (a difference indicates that the SPI response is latched due to inactive). Read multiple addresses to ensure a good comparison.
	Check VCC is enabled at PS_EN (J25) jumper	PS_EN can be enabled/disabled in hardware or software	Enable VCC/VEE from SPIGen. If using Rev B translator, set PS_EN (J25) to 2-3 to permanently enable the supply.
	Check VCC for undervoltage	Unpowered VCC prevents HV domain from updating data	Tune VCC-GNDISO using R20 feedback

7 Schematics, board layout and bill of materials

The board schematics, board layout and bill of materials are available at http://www.nxp.com/FRDMGD3100HBIEVM on the Overview tab under Get Started.

8 References

Following are URLs where you can obtain information on related NXP products and application solutions:

NXP.com support pages	Description	URL
FRDMGD3100HBIEVM	Tool summary page	http://www.nxp.com/FRDMGD3100HBIEVM
GD3100	Product summary page	http://www.nxp.com/GD3100

9 Revision history

Revision history

Revision	Date	Description
v.1	20180702	Initial version
v.2	20190403	• Section 4: complete rewrite • Global: various figures, tables updated to support new driver board revision (B) • Global: various figures, tables updated to support new translator board revision (C) • Section 5.2: updated text • Section 6.2: added SPIGen installation procedure • Section 6.1: added firmware installation procedure • Section 6.3: complete rewrite for newest release of SPIGen • Figure 14, Figure 15, Figure 16, Figure 17, Figure 18, Figure 19: updated for newest SPIGen (v7.2.2) release • Figure 20, Figure 21: added as general SPIGen support
v.3	20200210	• Figure 14, Figure 19: updated text • Section 6.2: added detail on firmware selection • Section 6.3.4: added detail on continuous PWM duty cycle definition • Section 6.4: added additional troubleshooting items

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