HFBR-5930/5930E

200 MBd Low-Cost SBCON Transceivers in 2 x 5 Package Style

Data Sheet

Description

The HFBR-5930/5930E transceiver from Avago provides the system designer with a product to implement the SBCON specification and to be compatible with IBM ESCON architecture.

This transceiver is supplied in the industry standard 2 x 5 DIP style with a MT-RJ fiber connector interface with an optional external connector shield (HFBR-5930E).

Transmitter Sections

The transmitter section of the HFBR-5930/5930E utilizes a 1300 nm InGaAsP LED. This LED is packaged in the optical subassembly portion of the transmitter section. It is driven by a custom silicon IC which converts differential PECL logic signals, ECL referenced (shifted) to a +3.3 V supply, into an analog LED drive current.

Receiver Sections

The receiver section of the HFBR-5930/5930E utilizes an InGaAs PIN photodiode coupled to a custom silicon transimpedance preamplifier IC. It is packaged in the optical subassembly portion of the receiver.

This PIN/preamplifier combination is coupled to a custom quantizer IC which provides the final pulse shaping for the logic output and the Signal Detect function. The Data output is differential. The Signal Detect output is single-ended. Both Data and Signal Detect outputs are PECL compatible, ECL referenced (shifted) to a +3.3 V power supply. The receiver outputs, Data Out and Data Out Bar, are squelched at Signal Detect Deassert.

Features

- Multisourced 2 x 5 package style with MT-RJ receptacle
- Single +3.3 V power supply
- Wave solder and aqueous wash process compatibility
- Manufactured in an ISO 9002 certified facility
- Compliant to SBCON 200 MBd specification

Applications

- Interconnection with IBM® compatible processors, directors and channel attachment units
  - Disk and tape drives
  - Communication controllers
- Data communication equipment
  - Local area networks
  - Point-to-point communication

Package

The overall package concept for the Avago transceiver consists of three basic elements; the two optical subassemblies, an electrical subassembly, and the housing as illustrated in the block diagram in Figure 1.

The package outline drawing and pin out are shown in Figures 2 and 3. The details of this package outline and pin out are compliant with the multisource definition of the 2 x 5 DIP. The low profile of the Avago transceiver design complies with the maximum height allowed for the MT-RJ connector over the entire length of the package.

The optical subassemblies utilize a high-volume assembly process together with low-cost lens elements which result in a cost-effective building block.

The electrical subassembly consists of a high volume multilayer printed circuit board on which the IC and various surface-mounted passive circuit elements are attached.

The receiver section includes an internal shield for the electrical and optical subassemblies to ensure high immunity to external EMI fields.

The outer housing including the MT-RJ ports is molded of filled nonconductive plastic to provide mechanical strength. The solder posts of the Avago design are isolated from the internal circuit of the transceiver.

The transceiver is attached to a printed circuit board with the ten signal pins and the two solder posts which exit the bottom of the housing. The two solder posts provide the primary mechanical strength to withstand the loads imposed on the transceiver by mating with the MT-RJ connectored fiber cables.

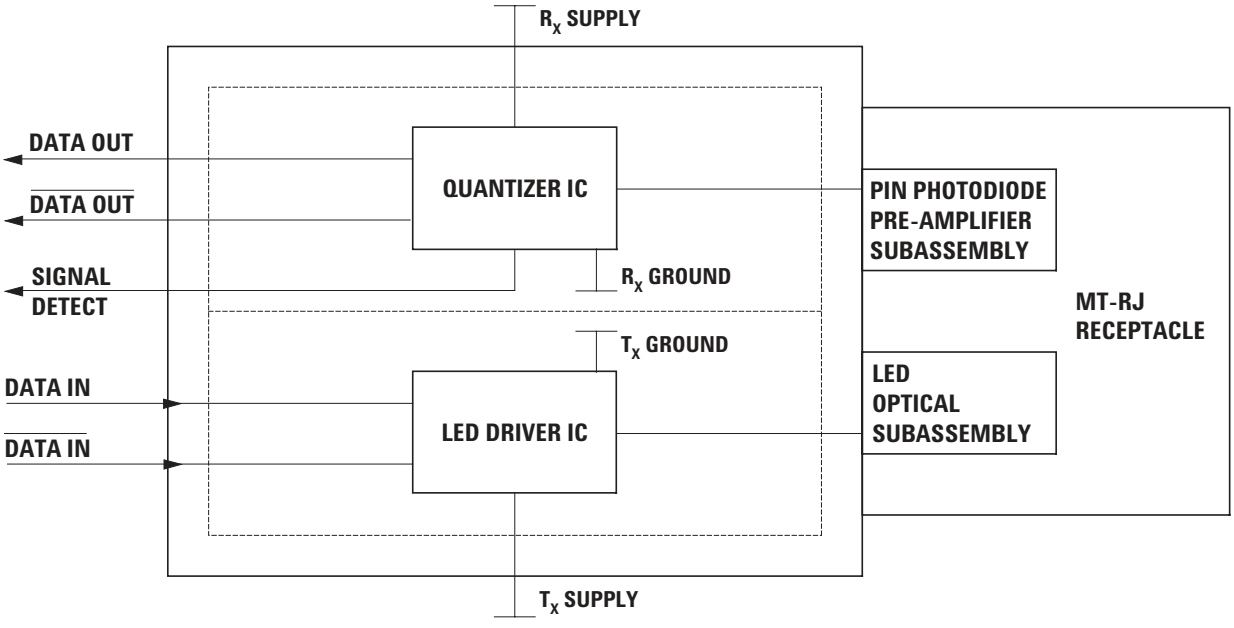
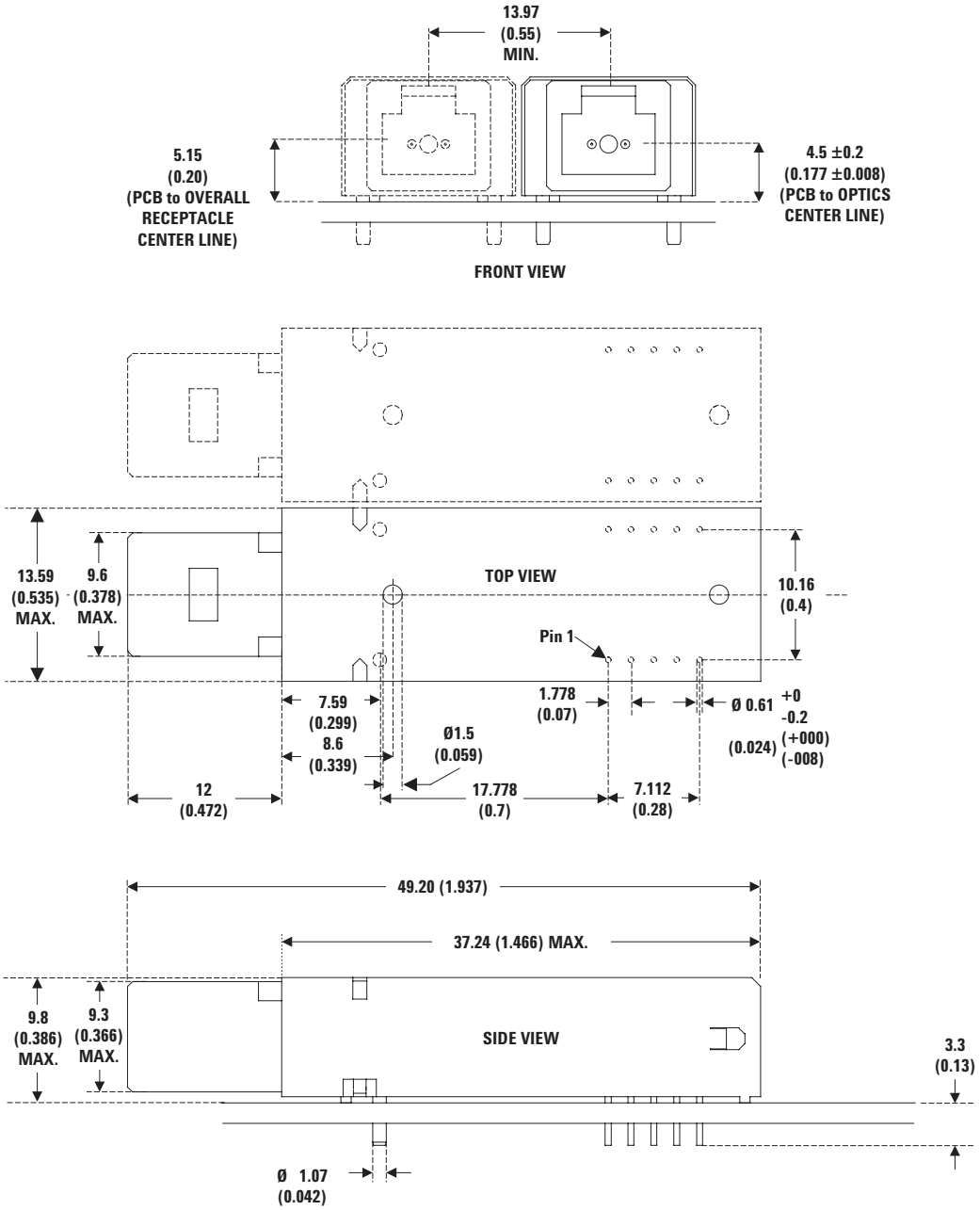


Figure 1. Block Diagram.



DIMENSIONS IN MILLIMETERS (INCHES)

NOTES:
1. THIS PAGE DESCRIBES THE MAXIMUM PACKAGE OUTLINE, MOUNTING STUDS, PINS AND THEIR RELATIONSHIPS TO EACH OTHER.
2. TOLERANCED TO ACCOMMODATE ROUND OR RECTANGULAR LEADS.
3. ALL 12 PINS AND POSTS ARE TO BE TREATED AS A SINGLE PATTERN.
4. THE MT-RJ HAS A 750 µm FIBER SPACING.
5. THE MT-RJ ALIGNMENT PINS ARE IN THE MODULE.
6. FOR SM MODULES, THE FERRULE WILL BE PC POLISHED (NOT ANGLED).
7. SEE MT-RJ TRANSCEIVER PIN OUT DIAGRAM FOR DETAILS.

Figure 2. Package Outline Drawing

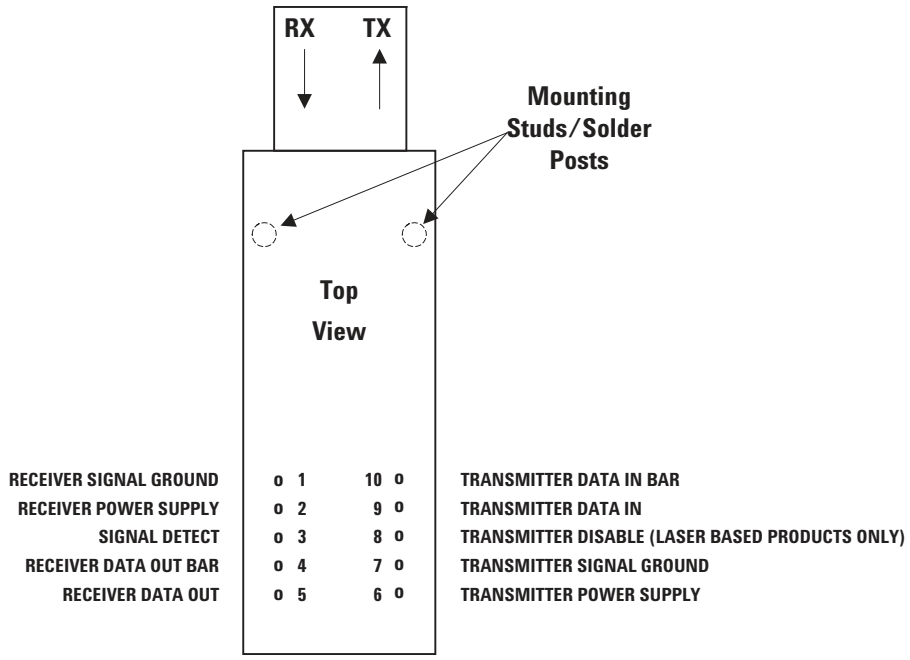


Figure 3. Pin Out Diagram.

Pin Descriptions:

Pin 1 Receiver Signal Ground V_{EE} RX:

Directly connect this pin to the receiver ground plane.

Pin 2 Receiver Power Supply V_{CC} RX:

Provide +3.3 V dc via the recommended receiver power supply filter circuit. Locate the power supply filter circuit as close as possible to the V_{CC} RX pin.

Pin 3 Signal Detect SD:

Normal optical input levels to the receiver result in a logic "1" output.

Low optical input levels to the receiver result in a fault condition indicated by a logic "0" output.

This Signal Detect output can be used to drive a PECL input on an upstream circuit, such as Signal Detect input or Loss of Signal-bar.

Pin 4 Receiver Data Out Bar RD-:

No internal terminations are provided. See recommended circuit schematic.

Pin 5 Receiver Data Out RD+:

No internal terminations are provided. See recommended circuit schematic.

Pin 6 Transmitter Power Supply V_{CC} TX:

Provide +3.3 V dc via the recommended transmitter power supply filter circuit. Locate the power supply filter circuit as close as possible to the V_{CC} TX pin.

Pin 7 Transmitter Signal Ground V_{EE} TX:

Directly connect this pin to the transmitter ground plane.

Pin 8 Transmitter Disable T_{DIS}:

No internal connection. Optional feature for laser based products only. For laser based products connect this pin to +3.3 V TTL logic high "1" to disable module. To enable module connect to TTL logic low "0".

Pin 9 Transmitter Data In TD+:

No internal terminations are provided. See recommended circuit schematic.

Pin 10 Transmitter Data In Bar TD-:

No internal terminations are provided. See recommended circuit schematic.

Mounting Studs/Solder Posts

The mounting studs are provided for transceiver mechanical attachment to the circuit board. It is recommended that the holes in the circuit board be connected to chassis ground.

Application Information

The Applications Engineering group is available to assist you with the technical understanding and design trade-offs associated with these transceivers. You can contact them through your Avago sales representative.

The following information is provided to answer some of the most common questions about the use of these parts.

Transceiver Optical Power Budget versus Link Length

Optical Power Budget (OPB) is the available optical power for a fiber optic link to accommodate fiber cable losses plus losses due to in-line connectors, splices, optical switches, and to provide margin for link aging and unplanned losses due to cable plant reconfiguration or repair.

Avago LED technology has produced 1300 nm LED devices with lower aging characteristics than normally associated with these technologies in the industry. The industry convention is 1.5 dB aging for 1300 nm LEDs. The 1300 nm Avago LEDs are specified to experience less than 1 dB of aging over normal commercial equipment mission life periods. Contact your Avago sales representative for additional details.

Recommended Handling Precautions

Avago recommends that normal static precautions be taken in the handling and assembly of these transceivers to prevent damage which may be induced by electrostatic discharge (ESD). The HFBR-5930/5930E series of transceivers meet MIL-STD-883C Method 3015.4 Class 2 products.

Care should be used to avoid shorting the receiver data or signal detect outputs directly to ground without proper current limiting impedance.

Solder and Wash Process Compatibility

The transceivers are delivered with protective process plugs inserted into the MT-RJ receptacle. This process plug protects the optical subassemblies during wave solder and aqueous wash processing and acts as a dust cover during shipping.

These transceivers are compatible with either industry standard wave or hand solder processes.

Shipping Container

The transceiver is packaged in a shipping container designed to protect it from mechanical and ESD damage during shipment or storage.

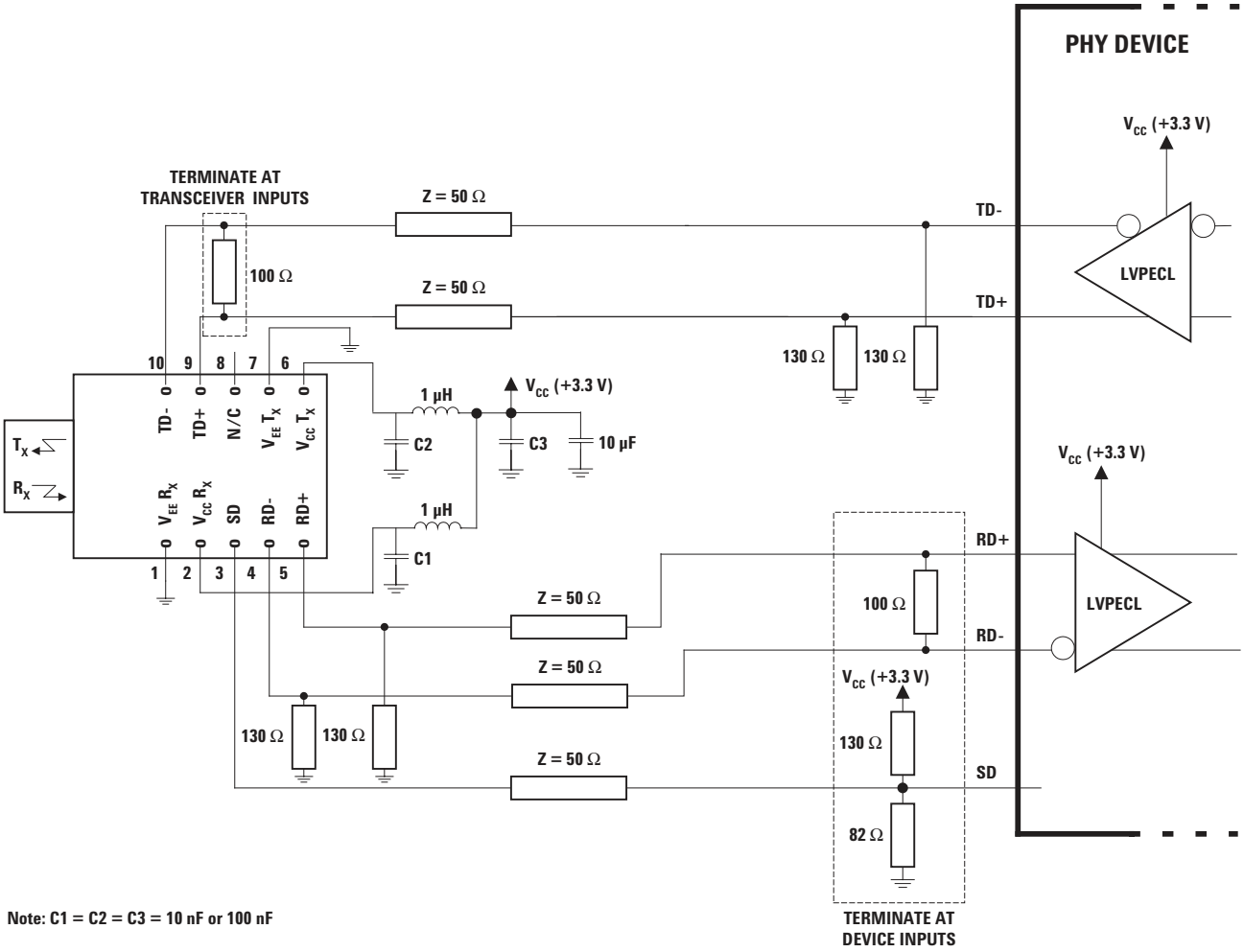


Figure 4. Recommended Decoupling and Termination Circuits

Board Layout - Decoupling Circuit, Ground Planes and Termination Circuits

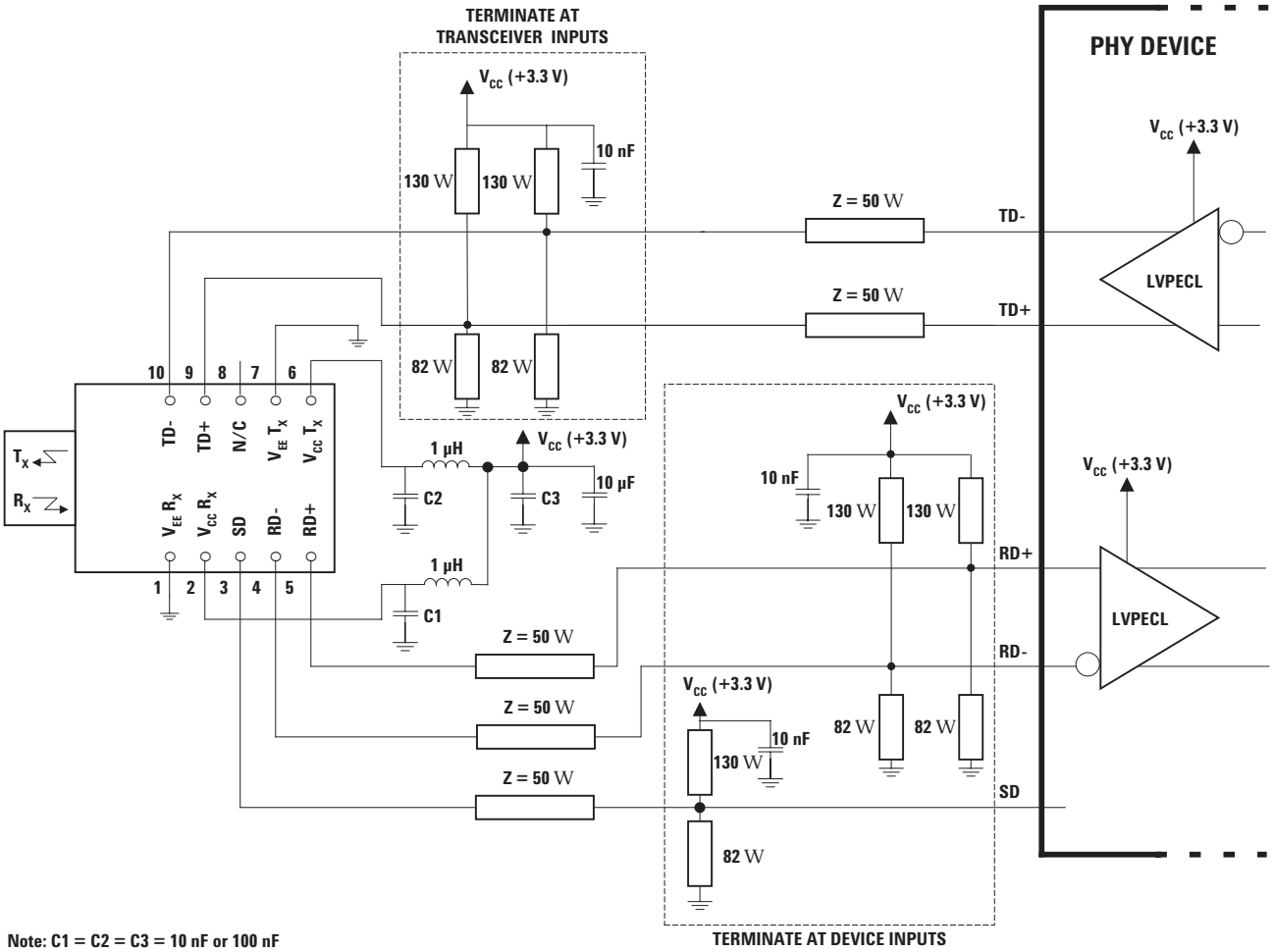
It is important to take care in the layout of your circuit board to achieve optimum performance from these transceivers. Figure 4 provides a good example of a schematic for a power supply decoupling circuit that works well with these parts. It is further recommended that a contiguous ground plane be provided in the circuit board directly under the transceiver to provide a low inductance ground for signal return current. This recommendation is in keeping with good high frequency board layout practices. Figures 4 and 5 show two recommended termination schemes.

Board Layout - Hole Pattern

The Avago transceiver complies with the circuit board "Common Transceiver Footprint" hole pattern defined in the original multisource announcement which defined the 2 x 5 package style. This drawing is reproduced in Figure 6 with the addition of ANSI Y14.5M compliant dimensioning to be used as a guide in the mechanical layout of your circuit board. Figure 7 illustrates the recommended panel opening and the position of the circuit board with respect to this panel.

Board Layout - Art Work

The Applications Engineering group has developed a Gerber file artwork for a multilayer printed circuit board layout incorporating the recommendations above. Contact your local Avago sales representative for details.



Note: C1 = C2 = C3 = 10 nF or 100 nF

Figure 5. Alternative Termination Circuits

Regulatory Compliance

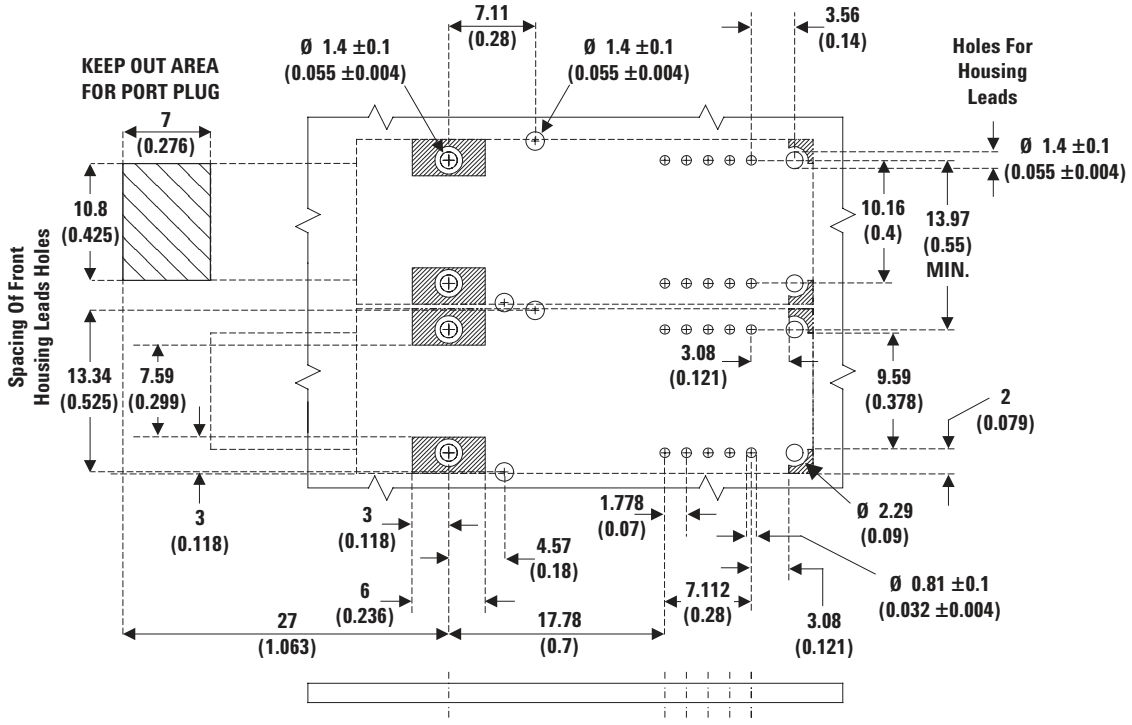
These transceiver products are intended to enable commercial system designers to develop equipment that complies with the various international regulations governing certification of Information Technology Equipment. See the Regulatory Compliance Table for details. Additional information is available from your Avago sales representative.

Electrostatic Discharge (ESD)

There are two design cases in which immunity to ESD damage is important.

The first case is during handling of the transceiver prior to mounting it on the circuit board. It is important to use normal ESD handling precautions for ESD sensitive devices. These pre-cautions include using grounded wrist straps, work benches, and floor mats in ESD controlled areas.

The second case to consider is static discharges to the exterior of the equipment chassis containing the transceiver parts. To the extent that the MT-RJ connector is exposed to the outside of the equipment chassis it may be subject to whatever ESD system level test criteria that the equipment is intended to meet.



DIMENSIONS IN MILLIMETERS (INCHES)

NOTES:

1. **THIS FIGURE DESCRIBES THE RECOMMENDED CIRCUIT BOARD LAYOUT FOR THE MT-RJ TRANSCEIVER PLACED AT .550 SPACING.**
2. **THE HATCHED AREAS ARE KEEP-OUT AREAS RESERVED FOR HOUSING STANDOFFS. NO METAL TRACES OR GROUND CONNECTION IN KEEP-OUT AREAS.**
3. **10 PIN MODULE REQUIRES ONLY 16 PCB HOLES, INCLUDING 4 PACKAGE GROUNDING TAB HOLES CONNECTED TO SIGNAL GROUND.**
4. **THE SOLDER POSTS SHOULD BE SOLDERED TO CHASSIS GROUND FOR MECHANICAL INTEGRITY AND TO ENSURE FOOTPRINT COMPATIBILITY WITH OTHER SFF TRANSCEIVERS.**

Figure 6. Recommended Board Layout Hole Pattern

Regulatory Compliance Table

Feature	Test Method	Performance
Electrostatic Discharge (ESD) to the Electrical Pins	MIL-STD-883C	Meets Class 2 (2000 to 3999 Volts). Withstand up to 2200 V applied between electrical pins.
Electrostatic Discharge (ESD) to the MT-RJ Receptacle	Variation of IEC 61000-4-2	Typically withstand at least 25 kV without damage when the MT-RJ Connector Receptacle is contacted by a Human Body Model probe.
Electromagnetic Interference (EMI)	FCC Class B CENELEC CEN55022 VCCI Class 2	Transceivers typically provide a 10 dB margin to the noted standard limits when tested at a certified test range with the transceiver mounted to a circuit card without a chassis enclosure.
Immunity	Variation of IEC 61000-4-3	Typically show no measurable effect from a 10 V/m field swept from 10 to 450 MHz applied to the transceiver when mounted to a circuit card without a chassis enclosure.
Eye Safety	AEL Class 1 EN60825-1 (+A11)	Compliant per Avago testing under single fault conditions. TUV Certification: Pending

Electromagnetic Interference (EMI)

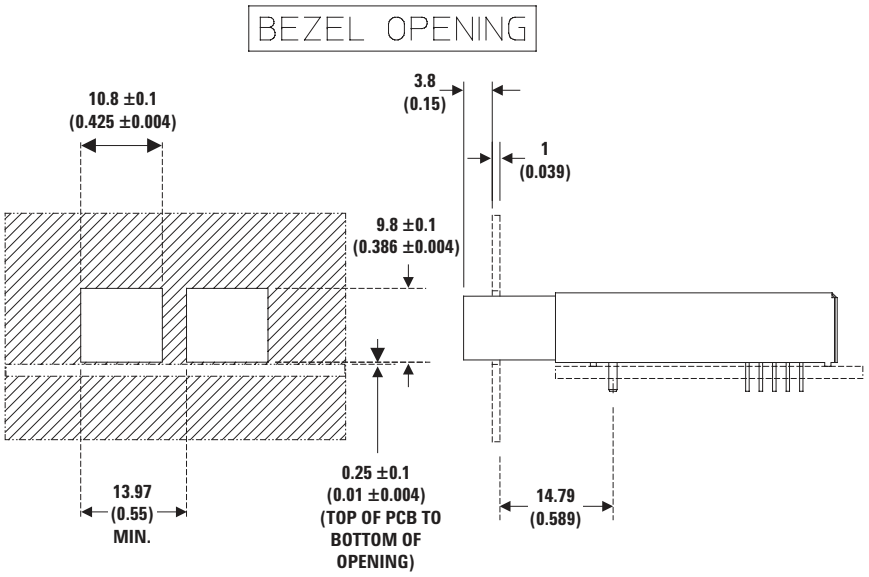
Most equipment designs utilizing this high speed transceiver from Avago will be required to meet the requirements of FCC in the United States, CENELEC EN55022 (CISPR 22) in Europe and VCCI in Japan.

This product is suitable for use in designs ranging from a desktop computer with a single transceiver to a concentrator or switch product with a large number of transceivers.

Immunity

Equipment utilizing these transceivers will be subject to radio-frequency electromagnetic fields in some environments. These transceivers have a high immunity to such fields.

For additional information regarding EMI, susceptibility, ESD and conducted noise testing procedures and results on the 1 x 9 Transceiver family, please refer to Application Note 1075, *Testing and Measuring Electromagnetic Compatibility Performance of the HFBR-510X/-520X Fiber Optic Transceivers.* Refer to Application Note 1166 *Minimizing Radiated Emissions of High-Speed Data Communications Systems*.



DIMENSIONS IN MILLIMETERS (INCHES)

Figure 7. Recommended Panel Mounting

Applications Support Materials

Contact your local Avago Component Field Sales Office for information on how to obtain PCB layouts and evaluation boards for the 2 x 5 transceivers.

Transceiver Reliability and Performance Qualification Data

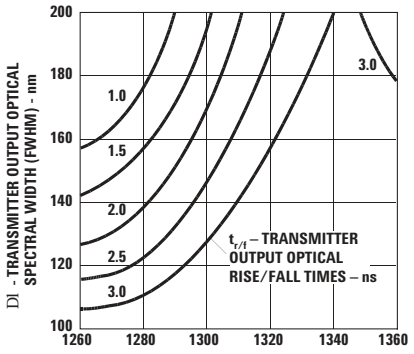
The 2 x 5 transceivers have passed Avago reliability and performance qualification testing and are undergoing ongoing quality and reliability monitoring. Details are available from your Avago sales representative.

These transceivers are manufactured at the Avago Singapore location which is an ISO 9002 certified facility.

Ordering Information

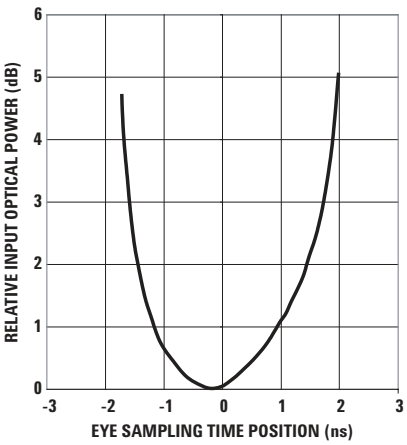
The HFBR-5930/5930E 1300 nm product is available for production orders through the Avago Component Field Sales Offices and Authorized Distributors world wide.

For technical information regarding this product, please visit Avago Semiconductor Products website at **www.Avago.com/view/fiber**. Use the quick search feature to search for this part number. You may also contact Avago Semiconductor Products Customer Response Center at 1-800-235-0312.



HFBR-5930 TRANSMITTER TEST RESULTS OF l_c, Dl AND $t_{r/f}$ ARE CORRELATED AND COMPLY WITH THE ALLOWED SPECTRAL WIDTH AS A FUNCTION OF CENTER WAVELENGTH FOR VARIOUS RISE AND FALL TIMES.

Figure 8. Transmitter Output Optical Spectral Width (FWHM) vs. Transmitter Output Optical Center Wavelength and Rise/Fall Times.



CONDITIONS:
1. T_A = +25° C
2. V_{CC} = 3.3 V dc
3. INPUT OPTICAL RISE/FALL TIMES = 1.0/2.1 ns.
4. INPUT OPTICAL POWER IS NORMALIZED TO CENTER OF DATA SYMBOL.
5. NOTE 15 AND 16 APPLY.

Figure 9. Relative Input Optical Power vs. Eye Sampling Time Position.

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause catastrophic damage to the device. Limits apply to each parameter in isolation, all other parameters having values within the recommended operating conditions. It should not be assumed that limiting values of more than one parameter can be applied to the product at the same time. Exposure to the absolute maximum ratings for extended periods can adversely affect device reliability.

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Reference
Storage Temperature	T_S	-40		+100	°C	
Lead Soldering Temperature	T_{SOLD}			+260	°C	
Lead Soldering Time	t_{SOLD}			10	Sec.	
Supply Voltage	V_{CC}	-0.5		3.6	V	
Data Input Voltage	V_I	-0.5		V_{CC}	V	
Differential Input Voltage	V_D			2.0	V	Note 1
Output Current	I_O			50	mA	

Recommended Operating Conditions

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Reference
Ambient Operating Temperature	T_A	0		+70	°C	
Supply Voltage	V_{CC}	3.135		3.465	V	
Data Input Voltage - Low	V_{IL} - V_{CC}	-1.81		-1.475	V	
Data Input Voltage - High	V_{IH} - V_{CC}	-1.165		-0.880	V	
Data and Signal Detect Output Load	R_L		50		Ω	Note 2

Transmitter Electrical Characteristics
(T_A = 0°C to +70°C, V_{CC} = 3.135 V to 3.465 V)

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Reference
Supply Current	I_{CC}		133	175	mA	Note 3
Power Dissipation	P_{DISS}		0.45	0.61	W	Note 4
Data Input Current - Low	I_{IL}	-350	-2		µA	
Data Input Current - High	I_{IH}		18	350	µA	

Receiver Electrical Characteristics
(T_A = 0°C to +70°C, V_{CC} = 3.135 V to 3.465 V)

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Reference
Supply Current	I_{CC}		65	125	mA	Note 5
Power Dissipation	P_{DISS}		0.25	0.43	W	Note 4
Data Output Voltage - Low	V_{OL} - V_{CC}	-1.86		-1.62	V	Note 6
Data Output Voltage - High	V_{OH} - V_{CC}	-1.10		0.86	V	Note 6
Data Output Rise Time	t_r	0.35		1.3	ns	Note 7
Data Output Fall Time	t_f	0.35		1.3	ns	Note 7
Signal Detect Output Voltage - Low	V_{OL} - V_{CC}	-1.88		-1.62	V	Note 6
Signal Detect Output Voltage - High	V_{OH} - V_{CC}	-1.10		-0.86	V	Note 6
Signal Detect Output Rise Time	t_r	0.35		2.2	ns	Note 7
Signal Detect Output Fall Time	t_f	0.35		2.2	ns	Note 7

Transmitter Optical Characteristics
(T_A = 0°C to +70°C, V_{CC} = 3.135 V to 3.465 V)

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Reference
Output Optical Power BOL62.5/125 µm, NA = 0.275 Fiber EOL	P_O	-19.5 -20.5	-16.0 -16.0	-14.0 -14.0	dBm avg.	Note 8
Optical Extinction Ratio		8			dB	Note 9
Center Wavelength	$_c$	1280		1380	nm	Figure 8
Spectral Width - FWHM			147	175	nm	Note 10 Figure 8
Optical Rise Time	t_r		1	1.7	ns	Note 11, 12 Figure 8
Optical Fall Time	t_f		1.3	1.7	ns	Note 11, 12 Figure 8
Output Optical Systematic Jitter	SJ		0.2	0.8	ns	Note 13

Receiver Optical Characteristics
(T_A = 0°C to +70°C, V_{CC} = 3.135 V to 3.465 V)

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Reference
Input Optical PowerMinimum at Window Edge	$P_{IN\ Min.}$ (W)			PinMin+1 dB	dBm avg.	Note 14 Figure 9
Input Optical PowerMinimum at Eye Center	$P_{IN\ Min.}$ (C)		-35	-29	dBm avg.	Note 15 Figure 9
Input Optical Power Maximum	$P_{IN\ Max.}$	-14			dBm avg.	Note 14
Operating Wavelength		1280		1380	nm	
Systematic Jitter	SJ		0.2	1.0	ns	Note 16
Eyewidth	t_{ew}	1.4			ns	Note 17
Signal Detect - Asserted	P_A	-44.5		-35.5	dBm avg.	Note 18
Signal Detect - Deasserted	P_D	-45		-36	dBm avg.	Note 19
Signal Detect - Hysteresis	P_A - P_D	0.5		4.0	dB	
Signal Detect Assert Time(off to on)	t_A	0.5		500	µs	Note 20
Signal Detect Deassert Time(on to off)	t_D	3		500	µs	Note 21

Notes:

1. This is the maximum voltage that can be applied across the Differential Transmitter Data Inputs to prevent damage to the input ESD protection circuit.
2. The outputs are terminated with 50 Ω connected to V_{CC} –2 V.
3. The power supply current needed to operate the transmitter is provided to differential ECL circuitry. This circuitry maintains a nearly constant current flow from the power supply. Constant current operation helps to prevent unwanted electrical noise from being generated and conducted or emitted to neighboring circuitry.
4. The power dissipation value is the power dissipated in the receiver itself. Power dissipation is calculated as the sum of the products of supply voltage and currents, minus the sum of the products of the output voltages and currents.
5. This value is measured with the outputs terminated into 50 Ω connected to V_{CC} –2 V and an Input Optical Power Level of –14.5 dBm average.
6. This value is measured with respect to V_{CC} with the output terminated into 50 Ω connected to V_{CC} –2 V.
7. The output rise time and fall times are measured between 20% and 80% levels with the output connected to V_{CC} – 2 V through 50 Ω.
8. These optical power values are measured with the following conditions:
   - The Beginning of Life (BOL) to theEnd of Life (EOL) optical power degradation is assumed to be 1.5 dB per the industry convention for long wavelength LEDs. The actual degradation observed in normal commercial environments will be <1.0 dB with Avago's 1300 nm LED products.
   - Over the specified operating voltage and temperature ranges.
   - Input Signal: 1010 data pattern, 200 Mb/s NRZ code.
9. The Extinction Ratio is a measure of the modulation depth of the optical signal. The data "0" output optical power is compared to the data "1" peak output optical and expressed in decibels. With the transmitter driven by a HALT Line State (12.5 Mhz square-wave) signal, the average optical power is measured. The data "1" peak power is then calculated by adding 3 dB to the measured average optical power. The data "0" output optical power is found by measuring the optical power when the transmitter is driven by a logic "0" input. The Extinction Ratio is the ratio of the optical power at the "0" level compared to the optical power at the "1" level expressed in decibels.
10. From an assumed Gaussian-shaped wavelength distribution, the relationship between FWHM and RMS values for Spectral Width is 2.35 x RMS = FWHM.
11. Input conditions: 100 MHz, square wave signal, input voltages are in the range specified for V_{IL} and V_{IH}.
12. Measured with electrical input signal rise and fall time of 0.35 to 1.3 ns (20-80%) at the transmitter input pins. Optical output rise and fall times are measured between 20% and 80% levels.
13. Transmitter Systematic Jitter is equal to the sum of Duty Cycle Distortion (DCD) and Data Dependent Jitter (DDJ). DCD is equivalent to Pulse-Width Distortion (PWD). Systematic Jitter is measured at the 50% signal level with 200 MBd, PRBS 2^7 –1 electrical input data pattern.
14. This specification is intended to indicate the performance of the receiver section of the transceiver when Input Optical Power signal characteristics are present per the following conditions. The Input Optical Power dynamic range from the minimum level (with a window time-width) to the maximum level is the range over which the receiver is guaranteed to provide output data with a Bit Error Ratio (BER) better than or equal to 10^{-15}.
   - At the Beginning of Life (BOL).
   - Over the specified operating temperature and voltage ranges.
   - Receiver data window time-width is 1.4 ns or greater and centered at mid-symbol.
   - Input signal is 200 MBd, Pseudo Random-Bit-Stream 2^7 –1 data pattern.
   - Transmitter cross-talk effects have been included in Receiver sensitivity. Transmitter should be running at 50% duty cycle (nominal) between 8 - 200 Mb/s, while Receiver sensitivity is measured.
15. All conditions of note 14 apply except that the measurement is made at the center of the symbol with no window time-width.
16. The receiver systematic jitter specification applies to optical powers between –14.5 dBm avg. to –27.0 dBm avg. at the receiver. Receiver Systematic Jitter is equal to the sum of Duty Cycle Distortion (DCD) and Data Dependent Jitter (DDJ). DCD is equivalent to Pulse-Width Distortion (PWD). Systematic Jitter is measured at the 50% signal level with 200 MBd, PRBS 2^7 –1 electrical output data pattern.
17. Eye-width specified defines the minimum clock time-position range, centered around the center of the 5 ns baud interval, at which the BER must be 10^{-12} or better. Test data pattern is PRBS 2^7 –1. The typical change in input optical power to open the eye to 1.4 nsec from a closed eye is less than 1.0 dB.
18. Status Flag switching thresholds:
    Direction of decreasing optical power:
    If Power >–36.0 dBm avg., then SF = 1 (high)
    If Power <–45.0 dBm avg., then SF = 0 (low)
    Direction of increasing optical power:
    If Power <–45.5 dBm avg., then SF = 0 (low)
    If Power >–35.5 dBm avg., then SF = 1 (high)
19. Status Flag Hysteresis is the difference in low-to-high and high-to-low switching thresholds. Thresholds must lie within optical power limits specified. The Hysteresis is desired to avoid Status Flag chatter when the optical input is near the threshold.
20. The Status Flag output shall be asserted within 500 µs after a step increase of the Input Optical Power. The step will be from a low Input Optical Power <–45.5 dBm avg., to >–35.5 dBm avg.
21. Status Flag output shall be de-asserted within 500 µs after a step decrease in the Input Optical Power. The Step will be from a high Input Optical Power >–36.0 dBm avg. to <–45.0 dBm avg.

For product information and a complete list of distributors, please go to our web site: **www.avagotech.com**

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