TPS2421-x 5-A, 20-V Integrated FET Hot Swap

1 Features

- Integrated Pass MOSFET
- Up to 20-V Bus Operation
- Programmable Fault Current
- Current Limit Proportionally Larger than Fault Current
- Programmable Fault Timer
- Internal MOSFET Power Limiting
- Latch-Off on Fault (TPS2421-1) and Retry (TPS2421-2) Versions
- SO-8 PowerPad™ Package
- –40°C to +125°C Junction Temperature Range
- UL2367 Recognized - File Number E169910

2 Applications

- RAID Arrays
- Telecommunications
- Plug-In Circuit Boards
- Disk Drives
- SSDs
- PCIE
- Fan Control

3 Description

The TPS2421 device provides highly integrated hot swap power management and superior protection in applications where the load is powered by busses up to 20 V. The TPS2421 device is well suited to standard bus voltages as low as 3.3 V because of the maximum-UV turnon threshold of 2.9 V. These devices are very effective in systems where a voltage bus must be protected to prevent shorts from interrupting or damaging the unit. The TPS2421 device is an easy to use devices in an 8-pin PowerPad™ SO-8 package.

The TPS2421 device has multiple programmable protection features. Load protection is accomplished by a non-current limiting fault threshold, a hard current limit, and a fault timer. The current dual thresholds allow the system to draw short high current pulses, while the fault timer is running, without causing a voltage droop at the load. An example of this is a disk drive startup. This technique is ideal for loads that experience brief high demand, but benefit from protection levels in-line with their average current draw.

Hotswap MOSFET protection is provided by power limit circuitry which protects the internal MOSFET against SOA related failures.

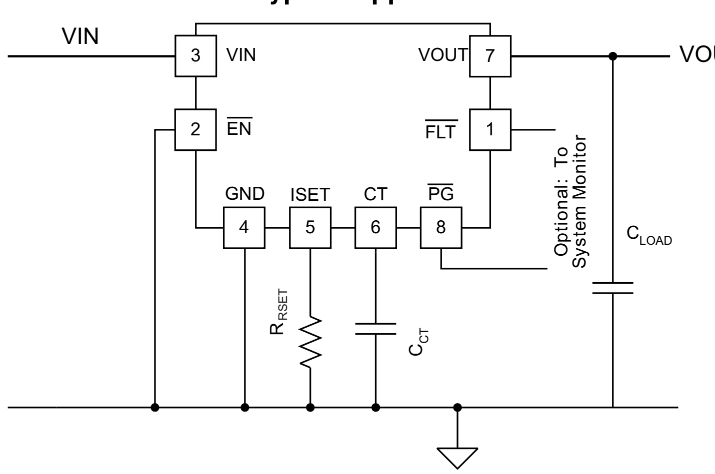
The TPS2421 device is available in latch-off on fault (TPS2421-1) and retry on fault (TPS2421-2).

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS2421-1	HSOP (8)	4.89 mm × 3.90 mm
TPS2421-2		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision J (October 2016) to Revision K — **Page**

- Updated the VIN, VOUT Unit in the *Electrical Characteristics* table 7

Changes from Revision I (January 2015) to Revision J — **Page**

- Updated *Maximum Allowable Load to Ensure Successful Startup* section 14
- Updated Equation 6 14

Changes from Revision H (January 2014) to Revision I — **Page**

- Changed the package and ordering information to the *Device Comparison Table* 5
- Added the I/O column to the *Pin Functions* table 5
- Added the *ESD Ratings* table and changed the CDM value From: 400V To: ±500V 6
- Replaced the Dissipation Ratings table with the *Thermal Information* table 6
- Added the *Detailed Description* section 11
- Changed the *PIN DESCRIPTION* section to the *Feature Description* section 12
- Added the *Application and Implementation* section 17
- Added the *Power Supply Recommendations* section 20
- Added Figure 23 21

Changes from Revision G (May 2013) to Revision H — **Page**

- Deleted minimum voltage from voltage range in the document title, features list and description 1
- Added 5-A to document title 1
- Changed *listed* to *recognized* in UL *FEATURES* bullet, also added specific UL number 1
- Added SSDs, PCIE, and Fan Control to the *APPLICATIONS* list 1

- Added maximum-UV turn-on threshold of 2.9 V sentence to the first paragraph of the *DESCRIPTION* 1
- Deleted capacitor, C_{VIN}, and diode from the *Typical Application* image. Also changed R_{SET} to R_{RSET} and C_{OUT} to C_{LOAD}. Removed voltage range and changed OUT to VOUT. Also removed note on the former C_{OUT} stating that this is only required in systems with lead and/or load inductance 1
- Changed C_{OUT} to C_{LOAD} and R_{SET} to R_{RSET} throughout document 1
- Changed current limit value of the ISET description from 125% to 150% in the *Pin Functions* table. Also removed *TPS2421 only* text form this description 5
- Changed C_{OUT} to C_{VOUT} for the power limit parameter in the *Electrical Characteristics* table 7
- Changed R_{SET} = 100 kW to R_{RSET} = 100 kΩ in the *FAULT CURRENT vs JUNCTION TEMPERATURE* graph 9
- Added note for TPS2421-1 to the *VIN* description in the *PIN DESCRIPTION* section 13
- Changed V_{IN} to V_{VIN} in the functional block diagram, Equation 6 14
- Changed *In* to V_{VIN} in Equation 17 18

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- Changed *In* to V_{VIN} in Equation 17 18

Changes from Revision F (April 2013) to Revision G — **Page**

- Deleted I_{SET}, C_T Voltage from the *Absolute Maximum Ratings*[(1)] table 6

Changes from Revision E (September 2011) to Revision F — **Page**

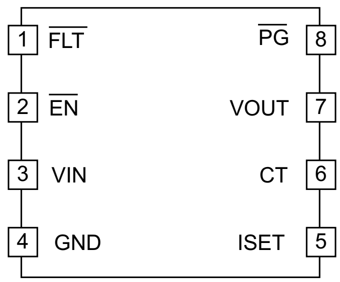
- Changed C_{CT} values From: MIN = 100 pF/µF To 0.1 nF and MAX From: 10 pF/µF To: -- in the *Recommended Operating Conditions* table 6
- Added R_{RSET} to the Recommended Operating Conditions table 6
- Changed the conditions statement of the Electrical Characteristics table 7
- Changed the TEST CONDITIONS for R_{ON} 7
- Changed I_{LIM} / I_{FLT} To: I_{LIM} / I_{SET} 7
- Changed the PIN DESCRIPTION section 12
- Changed the Application Information section. 17

5 Device Comparison Table

DEVICE	FEATURE
TPS2421-1	Latch-off
TPS2421-2	Auto-retry

6 Pin Configuration and Functions

TPS2421-x
DDA Package
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	$\overline{\text{FLT}}$	O	Fault low indicated the fault time has expired and the FET is switched off
2	$\overline{\text{EN}}$	I	Device is enabled when this pin is pulled low
3	VIN	I	Power In and control supply voltage
4	GND	—	GND
5	ISET	I/O	A resistor to ground sets the fault current, the current limit is 150% of the fault current
6	CT	I/O	A capacitor to ground sets the fault time
7	VOUT	O	Output to the load
8	$\overline{\text{PG}}$	O	Power Good low represents the output voltage is within 300 mV of the input voltage

7 Specifications

7.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)(2)

		MIN	MAX	UNIT
V_{VIN}, V_{VOUT}	Input voltage	–0.3	25	V
$\overline{EN}$	Input voltage	–0.3	6	V
$\overline{FLT}$, $\overline{PG}$	Voltage	–0.3	20	V
CT,(3) ISET(3)	Voltage	–0.3	3	V
I_{MAX}	Maximum continuous output current		9	A
$\overline{FLT}$, $\overline{PG}$	Output sink current		10	mA
T_J	Operating junction temperature	Internally Limited		
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to GND.
(3) Do not apply voltage to these pins.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

		MIN	MAX	UNIT
V_{VIN}, V_{VOUT}	Input voltage	3	20	V
$\overline{EN}$	Voltage	0	5	V
$\overline{FLT}$, $\overline{PG}$	Voltage	0	20	V
I_{OUT}	Continuous output current	0	6	A
$\overline{FLT}$, $\overline{PG}$	Output sink current	0	1	mA
C_{CT}		0.1		nF
R_{RSET}		49.9	200	kΩ
T_J	Junction temperature	–40	125	°C

7.4 Thermal Information

THERMAL METRIC(1)		TPS2421-x	UNIT
		DDA (HSOP)	
		8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	41.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	44.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	22.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	5.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	22.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

Unless otherwise noted: 3 V ≤ V_{VIN} ≤ 18 V, $\overline{EN}$ = 0 V, $\overline{PG}$ = $\overline{FLT}$ = open, R_{OUT} = open, R_{RSET} = 49.9 kΩ, –40°C ≤ T_J ≤ +125°C, No external capacitor connected to VOUT

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
VIN							
	UVLO	VIN rising		2.6	2.85	2.9	V
		Hysteresis			150		mV
	Bias current	$\overline{EN}$ = 2.4 V			25	100	µA
		$\overline{EN}$ = 0 V			3.9	5	mA
VIN, VOUT							
	R_{ON}	$R_{VIN-VOUT}$, $I_{VOUT} < I_{LIM}$, 1 A ≤ I_{VOUT} ≤ 4.5 A			33	50	mΩ
	Power limit TPS242x	V_{VIN}: 12 V, C_{VOUT} = 1000 µF, $\overline{EN}$: 3 V → 0 V		3	5	7.5	W
	Reverse diode voltage	$V_{VOUT} > V_{VIN}$, $\overline{EN}$ = 5 V, I_{VIN} = –1 A			0.77	1	V
ISET							
I_{SET}	Fault current threshold	I_{VOUT} ↑, I_{CT}: sinking → sourcing, pulsed test					A
		0°C ≤ T_J ≤ +85°C	R_{RSET} = 200 kΩ	0.8		1.2	
			R_{RSET} = 100 kΩ	1.8		2.2	
			R_{RSET} = 49.9 kΩ	3.6		4.4	
		–40°C ≤ T_J ≤ +125°C	R_{RSET} = 200 kΩ	0.75		1.25	
			R_{RSET} = 100 kΩ	1.75		2.25	
			R_{RSET} = 49.9 kΩ	3.6		4.4	
I_{LIM} / I_{SET}	Ratio I_{LIM} / I_{SET}	R_{RSET} = 200 kΩ		1.1	1.8	2.6	A
		R_{RSET} = 100 kΩ		1.1	1.5	2.1	
		R_{RSET} = 49.9 kΩ		1.1	1.4	1.6	
I_{LIM}	Current limit	I_{VOUT} rising, $V_{VIN–VOUT}$ = 0.3 V, pulsed test	R_{RSET} = 200 kΩ	1.1	1.8	2.4	A
			R_{RSET} = 100 kΩ	2.3	3	3.7	A
			R_{RSET} = 49.9 kΩ	4.6	5.5	6.3	A
CT							
	Charge-discharge current	I_{CT} sourcing, V_{CT} = 1 V, In current limit		29	35	41	µA
		I_{CT} sinking (–2), V_{CT} = 1 V, drive CT to 1 V, measure current		1	1.4	1.8	
	Threshold voltage	V_{CT} rising		1.3	1.4	1.5	V
		V_{CT} falling, drive CT to 1 V, measure current		0.1	0.16	0.3	
	ON/OFF fault duty cycle	V_{VOUT} = 0 V		2.8%	3.7%	4.6%	
$\overline{EN}$							
	Threshold voltage	$V_{\overline{EN}}$ falling		0.8	1	1.5	V
		Hysteresis		20	150	250	mV
	Input bias current	$V_{\overline{EN}}$ = 2.4 V		–2	0	0.5	µA
		$V_{\overline{EN}}$ = 0.2 V		–3	1	0.5	
	Turnon propagation delay	V_{VIN} = 3.3 V, I_{LOAD} = 1 A, $V_{\overline{EN}}$: 2.4 V → 0.2 V, V_{VOUT}: rising 90% × V_{VIN}			350	500	µs
	Turnoff propagation delay	V_{VIN} = 3.3 V, I_{LOAD} = 1 A, $V_{\overline{EN}}$: 0.2 V → 2.4 V, V_{VOUT}: ↓ 10% × V_{VIN}			30	50	

Electrical Characteristics (continued)

Unless otherwise noted: 3 V ≤ V_{VIN} ≤ 18 V, $\overline{EN}$ = 0 V, $\overline{PG}$ = $\overline{FLT}$ = open, R_{OUT} = open, R_{RSET} = 49.9 kΩ, –40°C ≤ T_J ≤ +125°C, No external capacitor connected to VOUT

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\overline{FLT}$						
V_{OL}	Low level output voltage	V_{CT} = 1.8 V, $I_{\overline{FLT}}$ = 1 mA		0.2	0.4	V
	Leakage current	$V_{\overline{FLT}}$ = 18 V			1	µA
$\overline{PG}$						
	PG threshold	$V_{(VIN–VOUT)}$ falling	0.4	0.5	0.75	V
		Hysteresis	0.1	0.25	0.4	V
V_{OL}	Low level output voltage	$I_{\overline{PG}}$ = 1 mA		0.2	0.4	V
	Leakage current	$V_{\overline{PG}}$ = 18 V			1	µA
THERMAL SHUTDOWN						
T_{SD}	Thermal shutdown	Junction temperature rising		160		°C
		Hysteresis		10		°C

7.6 Typical Characteristics

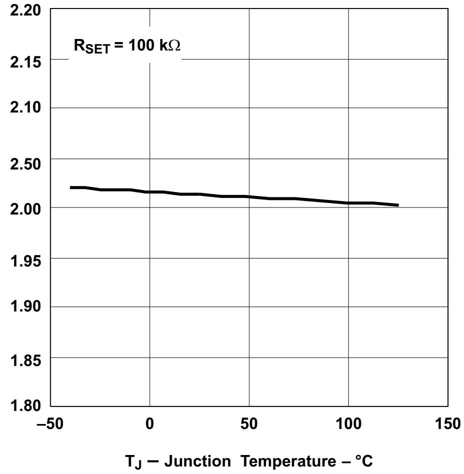


Figure 1. Fault Current vs Junction Temperature

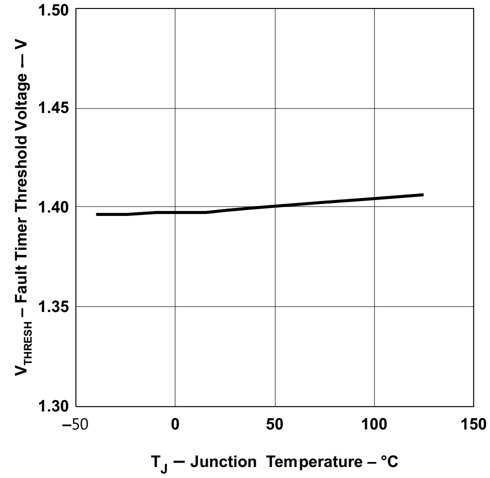


Figure 2. Fault Timer Threshold Voltage vs Junction Temperature

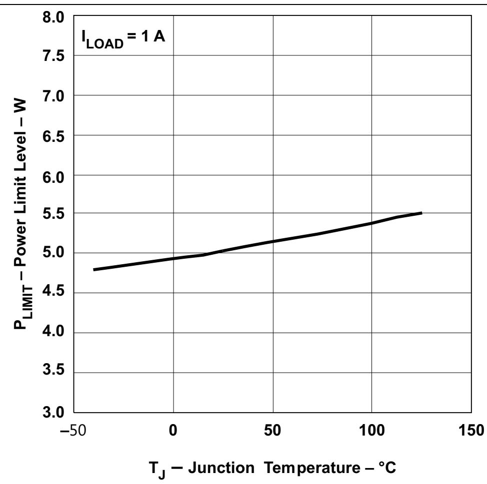


Figure 3. Power Limit vs Junction Temperature

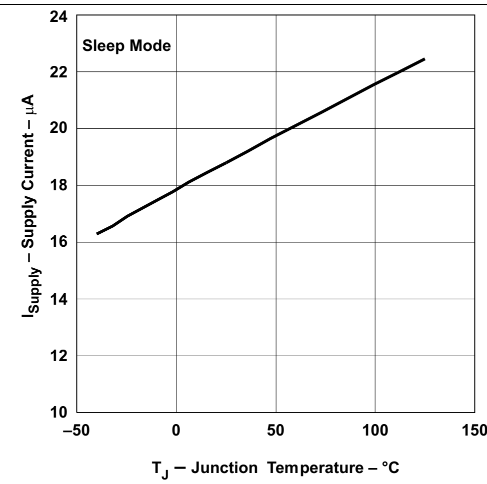


Figure 4. Supply Current vs Junction Temperature

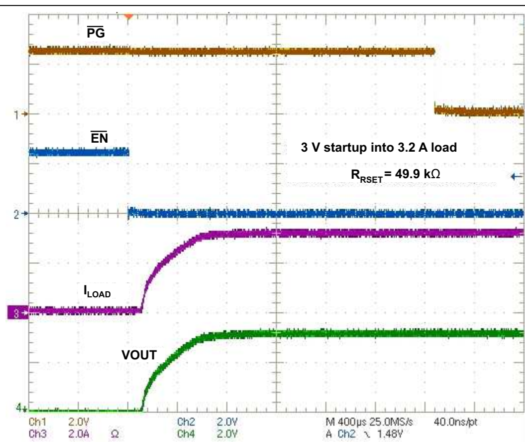


Figure 5. 3-V Startup into 1-Ω Load

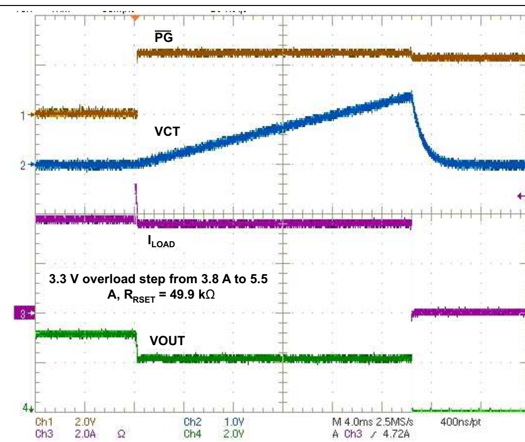


Figure 6. 3-V Firm Overload, Load Stepped from 3.8 A to 5.5 A

Typical Characteristics (continued)

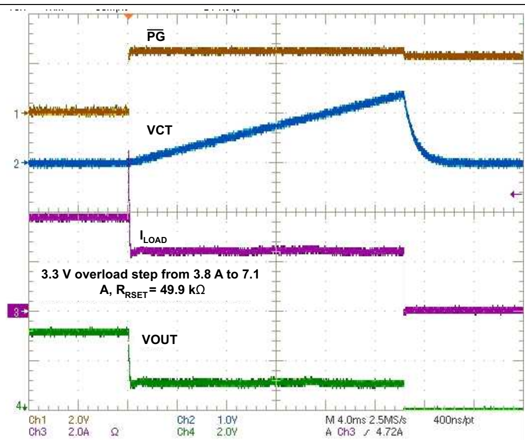


Figure 7. 3-V Hard Overload, Load Stepped from 3.8 A to 7.1 A

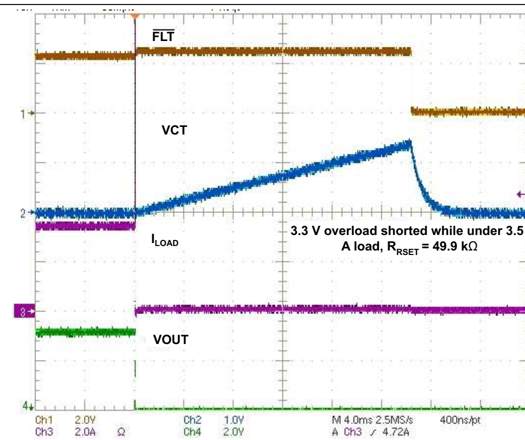


Figure 8. 3-V Output Shorted While Under 3.5-A Load

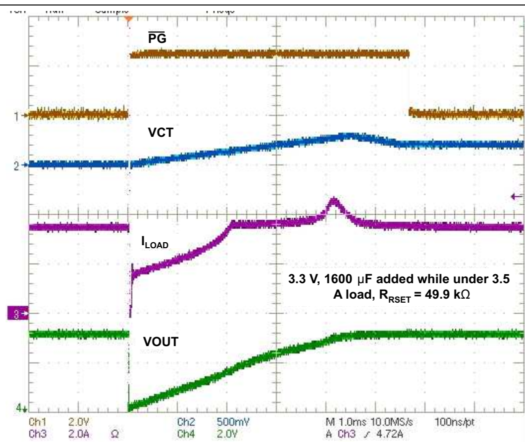


Figure 9. 3 V, 1600 μF Added to 3.5-A Load

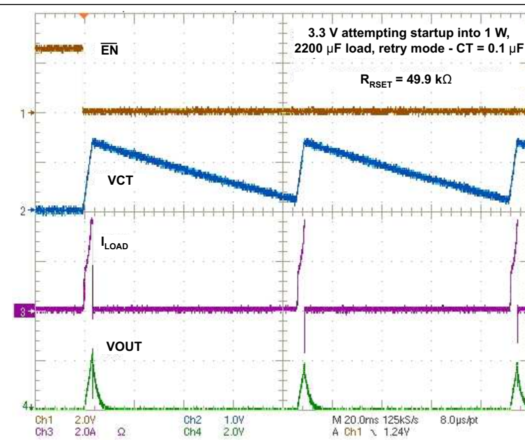


Figure 10. 3-V Retry Startup into 1-Ω, 2200-μF Load

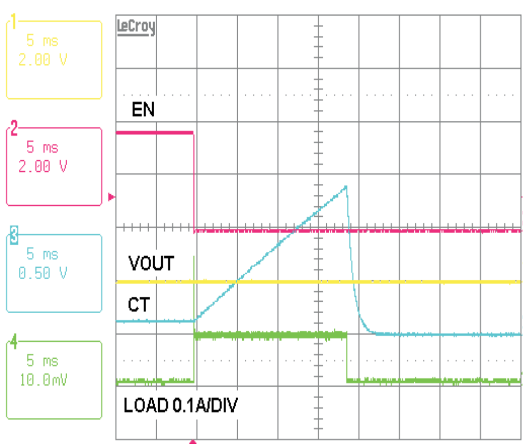


Figure 11. Startup into a Short Circuit Output

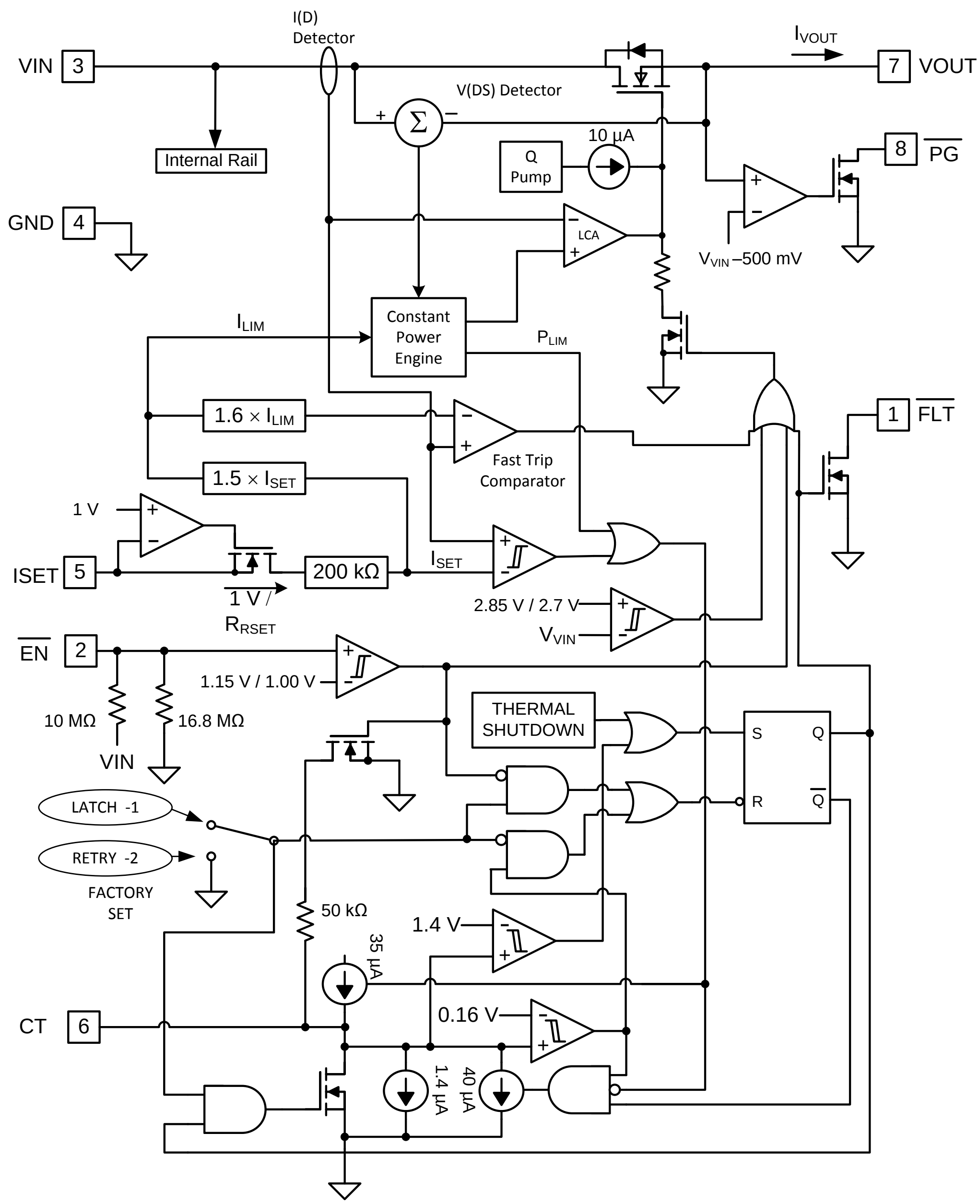
8 Detailed Description

8.1 Overview

The TPS2421 device provides highly integrated hot swap power management and superior protection in applications where the load is powered by busses up to 20 V.

The device has multiple programmable protection features. Load protection is accomplished by a non-current limiting fault threshold, a hard current limit, and a fault timer. Hotswap MOSFET protection is provided by power limit circuitry which protects the internal MOSFET against SOA related failures.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 CT

Connect a capacitor from CT to GND to set the fault time. The fault timer starts when I_{VOUT} exceeds I_{SET} or when SOA protection mode is active, charging the capacitor with 35 µA from GND towards an upper threshold of 1.4 V. If the capacitor reaches the upper threshold, the internal pass MOSFET is turned off. For the TPS2421-1 device, the MOSFET remains off until $\overline{EN}$ is cycled. For the TPS2421-2 device, the capacitor discharges at 1.4 µA to 0.16 V and then re-enable the pass MOSFET. If the upper threshold is not crossed, the capacitor discharges at 40 µA to 0.16 V and then to 0 V at 1.4 µA. When the device is disabled, CT is pulled to GND through a 50-kΩ resistor.

The timer period must be chosen long enough to allow the external load capacitance to charge. The nominal (not including component tolerances) fault timer period is selected using Equation 1 where T_{FAULT} is the minimum timer period in seconds and C_{CT} is in Farads.

$$C_{CT} = \frac{T_{FAULT}}{40 \text{ x } 10^3} \tag{1}$$

For the TPS2421-2 device, the second and subsequent retry timer periods are slightly shorter than the first retry period. CT nominal (not including component tolerances) discharge time, t_{SD} from 1.4 V to 0.16 V is shown in Equation 2, where C_{CT} is in Farads and t_{SD} is in seconds.

$$T_{SD} = 885.7 \times 10^3 \times C_{CT} \tag{2}$$

The nominal ratio of on to off times represents about a 3.7% duty cycle when a hard fault is present on the output.

8.3.2 FLT

Open-drain output that pulls low on any condition that causes the output to open. These conditions are either an overload with a fault time-out, or a thermal shutdown. $\overline{FLT}$ becomes operational before UV, when V_{VIN} is greater than 1 V. $\overline{FLT}$ pulses low momentarily prior to the onset of V_{VOUT} ramp up during IN or $\overline{EN}$ based startup.

8.3.3 GND

This is the most negative voltage in the circuit and is used as reference for all voltage measurements unless otherwise specified.

8.3.4 ISET

A resistor from this pin to GND sets both the fault current (I_{SET}) and current limit (I_{LIM}) levels. The current limit is internally set at 150% of the fault current. The fault timer described in the CT section starts when I_{VOUT} exceeds I_{SET}.

The internal MOSFET actively limits current if I_{VIN} reaches the current limit set point. The fault timer operation is the same in this mode as described previously.

The fault current value is programmed as shown in Equation 3:

$$R_{RSET} = \frac{200\,k\Omega}{I_{SET}} \tag{3}$$

$\overline{EN}$: When this pin is pulled low, the device is enabled. The input threshold is hysteretic, allowing the user to program a startup delay with an external RC circuit. $\overline{EN}$ is pulled to VIN with a 10-MΩ resistor and to GND with a 16.8-MΩ resistor. Because high impedance pullup and pulldown resistors are used to reduce current draw, any external FET controlling this pin must be low leakage.

8.3.5 VIN

Input voltage to the TPS2421 device. The recommended operating voltage range is 3 V to 20 V. Connect VIN to the power source.

Feature Description (continued)

NOTE

(For TPS2421-1 only) Brownout-type conditions (VIN < 2.85 V) prior to startup can trigger the fault logic and prevent startup. For more information go to E2E.TI.com.

8.3.6 VOUT

Output connection for the TPS2421 device. V_{VOUT} in the ON condition considering the ON resistance of the internal MOSFET, R_{ON} is shown in Equation 4:

$$V_{VOUT} = V_{VIN} - R_{ON} \times I_{VOUT} \quad (4)$$

Connect VOUT to the load.

8.3.7 $\overline{PG}$

Active low, Open Drain output, Power Good indicates that there is no fault condition and the output voltage is within 0.5 V of the input voltage. $\overline{PG}$ becomes operational before UV, whenever V_{VIN} is greater than 1 V.

8.4 Device Functional Modes

8.4.1 Startup

Large inrush current occurs when power is applied to discharged capacitors and load. During the inrush period, the TPS2421 device operates in power limit (or SOA protect mode) managing the current as V_{VOUT} rises. In SOA protect mode, the internal MOSFET power dissipation ($[V_{VIN} – V_{VOUT}] \times I_{VOUT}$) is regulated at 5 W typical while the fault timer starts and C_{CT} ramps up. As the charge builds on C_{LOAD}, the current increases towards I_{LIM}. When the capacitor is fully charged, I_{VOUT} drops to the dc load value, the fault timer stops, and C_{CT} ramps down. In order for the TPS2421 device to start properly, the fault timer duration must exceed C_{LOAD} startup time, t_{ON}. Startup time without additional dc loading is calculated using Equation 5 where P_{LIM} = 5 W (typical).

$$t_{ON} = \frac{C_{LOAD} \times P_{LIM}}{2 \times I_{LIM}^2} + \frac{C_{LOAD} \times V_{VIN}^2}{2 \times P_{LIM}} \quad (5)$$

When the load has a resistive component in addition to C_{LOAD}, the fault time must be extended because the resistive load current is unavailable to charge C_{LOAD}. Use Table 1 and Table 2 to predict startup time in the presence of resistive dc loading.

Refer to the TPS2421 Design Calculator Tool (SLUC427) for assistance with design calculations.

Table 1. Startup Time (ms) with DC Loading: V_{IN} = 5 V, P_{LIM} = 3 W, I_{LIM} = 5 A

R_{LOAD} (Ω)	C_{LOAD} = 100 µF	C_{LOAD} = 220 µF	C_{LOAD} = 470 µF	C_{LOAD} = 1000 µF
1000	0.43	0.95	2.03	4.33
10	0.5	1.11	2.36	5.03
5	0.61	1.34	2.87	6.1
3	0.91	2	4.28	9.11
2.5	1.31	2.88	6.14	13.07

Table 2. Startup Time (ms) with DC Loading: V_{IN} = 12 V, P_{LIM} = 3 W, I_{LIM} = 5 A

R_{LOAD} (Ω)	C_{LOAD} = 100 µF	C_{LOAD} = 220 µF	C_{LOAD} = 470 µF	C_{LOAD} = 1000 µF
10000	2.46	5.41	11.56	24.59
100	2.67	5.87	12.55	26.69
50	2.93	6.45	13.79	29.34
15	6.7	14.74	31.5	67.01
13	11.68	25.69	54.87	116.75

8.4.2 Maximum Allowable Load to Ensure Successful Startup

The power limiting function of the TPS2421 provides effective protection and limits the maximum allowable resistive load (R_{MIN}) during startup to ensure SOA of the device. Load resistance lower than R_{MIN} can cause the output to shut off due to CT timeout or thermal shutdown. The equation for maximum load R_{MIN} as a function of V_{IN}, P_{LIM} and I_{LIM} is given by Equation 6:

$$R_{LOAD} > R_{MIN} = \max\left(\frac{V_{IN}^2}{4 \times P_{LIM(min)}}, \frac{V_{IN}}{I_{LIM(min)} \times K}\right) = \max\left(\frac{V_{IN}^2}{12}, \frac{V_{IN}}{I_{LIM(min)} \times K}\right)$$

where

- K = 0.15 for R_{RSET} = 200 kΩ
- K = 0.3 for R_{RSET} = 100 kΩ
- K = 0.5 for R_{RSET} = 49.9 kΩ
- $I_{LIM(min)}$ is the current limit minimum specification given in the EC Table (6)

The device fails to start if $R_{LOAD} < R_{MIN}$. It either enters thermal shutdown or CT timer may timeout. The load resistance during startup (R_{LOAD}) must be higher than R_{MIN} for a successful startup. Ensure that R_{LOAD} is > R_{MIN} per Equation 6.

8.4.2.1 Enable Pin Considerations

For the case when $\overline{EN}$ is simply connected to GND, the TPS2421 device starts ramping the voltage on VOUT as VIN rises above UVLO (approximately 2.85 V typical). If IN does not ramp monotonically, the TPS2421 may momentarily turnoff then on during startup if IN falls below approximately 2.7 V. To avoid this problem, $\overline{EN}$ assertion can be delayed until IN is sufficiently above UVLO. A simple approach is shown in Figure 12. The 100-kΩ pullup resistor de-asserts $\overline{EN}$ when VIN is above approximately 1.75 V maximum which is well below the minimum UVLO of approximately 2.6 V. The Zener diode ensures that $\overline{EN}$ remains below 5 V. User control to enable the TPS2421 device is applied at the ON node to turn on the FET once IN has risen sufficiently above UVLO.

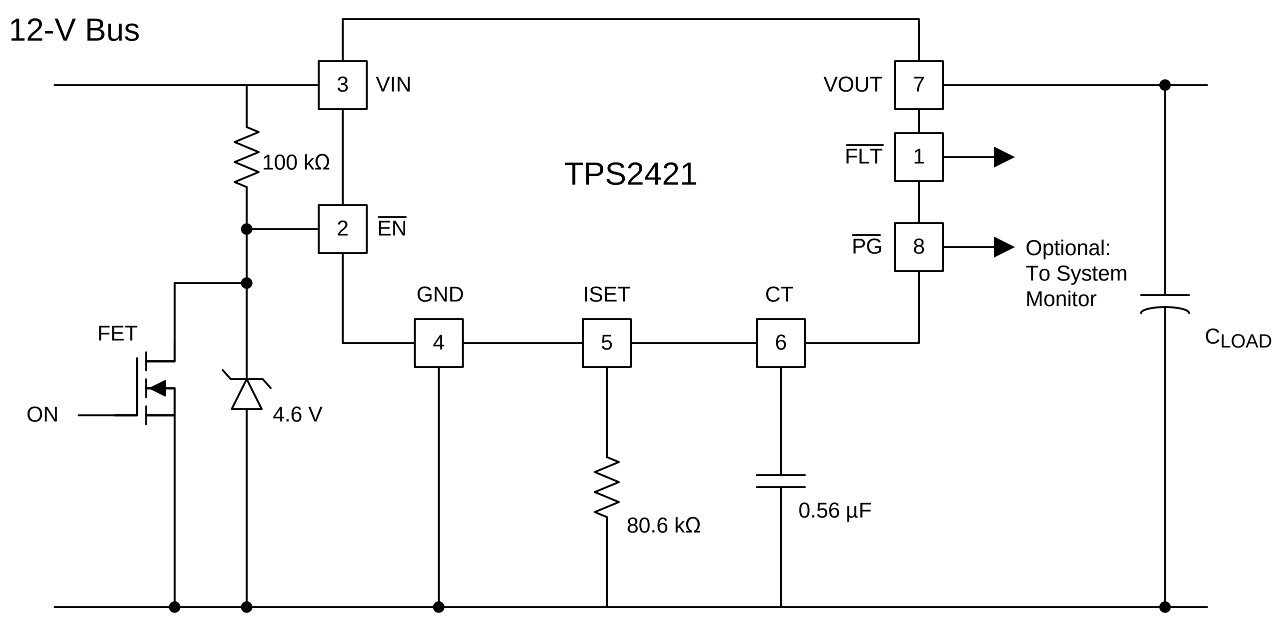


Figure 12. EN Delay Circuit

8.4.2.2 Fault Timer

The fault timer is active when the TPS2421 device is in SOA protect mode or the current is above I_{SET}. Figure 13 illustrates operation during non-faulted startup (C_{LOAD} = 470 µF and I_{VOUT} = 1 A in a 12 V system). C_{CT} charges at approximately 35 µA until TPS2421 device exits SOA protect mode, discharges quickly (approximately 40 µA) to approximately 0.16 V, and then decays slowly (approximately 1.4 µA) towards zero.

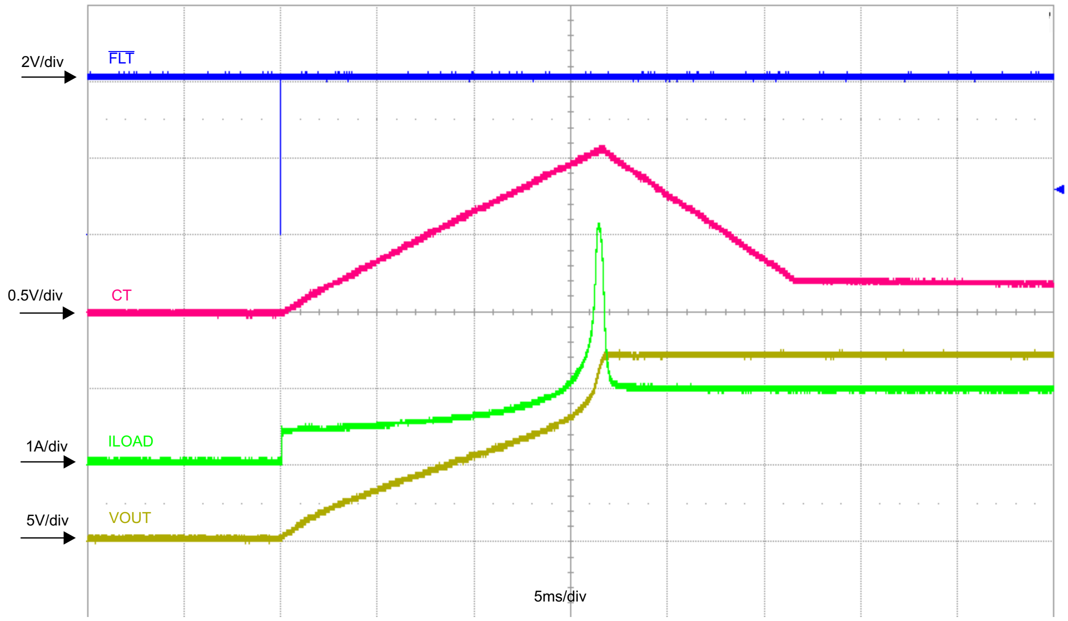


Figure 13. Fault Timer Operation During Startup

C_{CT} can be chosen for fault-free startup including expected C_{LOAD} and C_{CT} capacitance tolerance as shown in Equation 7.

$$C_{CT} = \frac{(1 + C_{LOAD\_TOL} + C_{CT\_TOL}) \times t_{ON}}{40000} \quad (7)$$

8.4.2.3 Normal Operation

When load current exceeds I_{SET} during normal operation the fault timer starts. If load current drops below I_{SET} before the fault timer expires, normal operation continues. If load current stays above the I_{SET} threshold the fault timer expires and a fault is declared. When a fault is declared a TPS2421-1 device turns off an can be restarted by cycling power or toggling the $\overline{EN}$ signal. A TPS2421-2 device attempts to turn on at a 3.7% duty cycle until the fault is cleared. When I_{LIM} is reached during a fault the device goes into current limit and the fault timer keeps running.

8.4.2.4 Startup into a Short

The controller attempts to power on into a short for the duration of the timer. Figure 11 shows a small current resulting from power limiting the internal MOSFET. This occurs only once for theTPS2421-1 device. For the TPS2421-2 device, the cycle repeats at a 3.7% duty cycle as shown in Figure 10.

8.4.3 Shutdown Modes

8.4.3.1 Hard Overload - Fast Trip

When a hard overload causes the load current to exceed approximately 1.6 × I_{LIM} the TPS2421 immediately shuts off current to the load without waiting for the fault timer to expire. After such a shutoff the TPS2421 device enters startup mode and attempts to apply power to the load. If the hard overload was caused by a transient, then normal startup can be expected. If the hard overload is caused by a persistent, continuous failure then the TPS2421 device enters into current limit during the restart attempt and either latches off (TPS2421-1) or attempts retry (TPS2421-2).

8.4.3.2 Overcurrent Shutdown

Overcurrent shutdown occurs when the output current exceeds I_{SET} for the duration of the fault timer. Figure 18 shows a step rise in output current which exceeds the I_{SET} threshold but not the I_{LIM} threshold. The increased current is on for the duration of the timer. When the timer expires, the output is turned off.

8.5 Programming

8.5.1 Fault (I_{SET}) and Current-Limit (I_{LIM}) Thresholds

The I_{SET} and I_{LIM} thresholds is user programmable with a single external resistor connected to ISET and the I_{LIM} threshold is internally set according to the I_{LIM}/I_{SET} ratio specified in the electrical characteristics table. The TPS2421 device uses an internal regulation loop to provide a regulated voltage on the ISET pin. The fault and current-limit thresholds are proportional to the current sourced out of ISET. The recommended 1% resistor range is 49.9 kΩ ≤ R_{RSET} ≤ 200 kΩ to ensure the rated accuracy. Many applications require that minimum fault and current limits are known or that maximum current limit is bounded. Considering the tolerance of the fault and current limit thresholds, as well as R_{RSET} when selecting values is important. See the *Electrical Characteristics* table for specific fault and current limit settings.

Using the data for I_{SET} and I_{LIM} from the *Electrical Characteristics*, equations are generated and used for other set points. Equation 8 and Equation 9 are used to calculate minimum and maximum I_{SET} where $R_{RSET,max}$ and $R_{RSET,min}$ include R_{RSET} tolerances. Equation 10 and Equation 11 calculate $R_{RSET,max}$ and $R_{RSET,min}$ where R_{TOL} is the 1% resistor tolerance.

$$I_{SET,min} = \frac{185.58}{R_{RSET,max}} - 0.13 \quad (8)$$

$$I_{SET,max} = \frac{213.68}{R_{RSET,min}} + 0.13 \quad (9)$$

$$R_{RSET,min} = (1 + R_{TOL}) \times \frac{213.68}{I_{SET,max} - 0.13} \quad (10)$$

$$R_{RSET,max} = (1 - R_{TOL}) \times \frac{185.58}{I_{SET,min} + 0.13} \quad (11)$$

Equation 12 and Equation 13 are used to calculate minimum and maximum I_{LIM} where $R_{RSET,max}$ and $R_{RSET,min}$ include R_{RSET} tolerances.

$$I_{LIM,min} = \frac{232.19}{R_{RSET,max}} - 0.06 \quad (12)$$

$$I_{LIM,max} = \frac{259.26}{R_{RSET,min}} + 1.11 \quad (13)$$

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS2421 is an integrated FET hot swap device. It is typically used for Hot-Swap and Power rail protection applications. It operates from 3 V to 20 V with programmable fault current limit, and fault Timer.

The following design procedure can be used to select component values for the device. This section presents a simplified discussion of the design process.

9.2 Typical Application

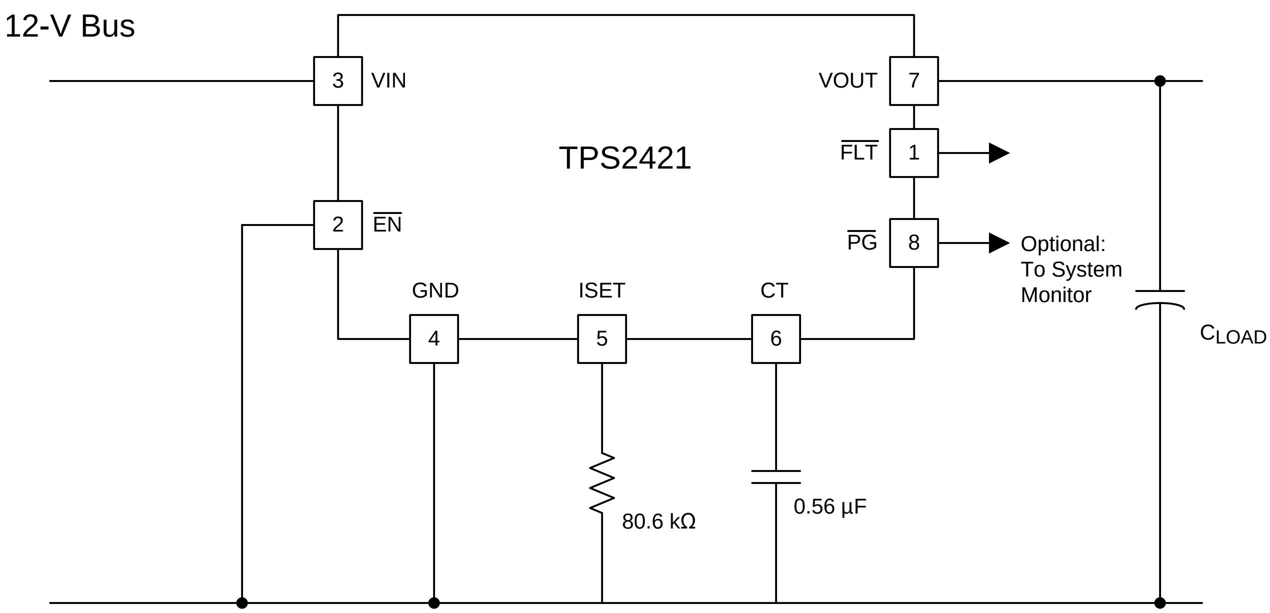


Figure 14. Design Example Schematic

9.2.1 Design Requirements

A typical design is shown in Figure 14 with the following requirements:

- Nominal input voltage, V_{VIN}: 12 V
- Maximum expected load current, I_{VOUT}: 2.1 A
- Load capacitance, C_{LOAD}: 220 µF
- Expected resistive load, R_{LOAD} during startup: 15 Ω
- Example calculations are shown in the TPS2421 Design Calculator Tool (SLUC427).

Typical Application (continued)

9.2.2 Detailed Design Procedure

1. Calculate maximum R_{RSET} to ensure that minimum I_{SET} is above maximum operating load current using Equation 11 as shown below in Equation 14.

$$R_{RSET,max} = 0.99 \times \frac{185.58}{2.1 + 0.13} = 82.39 k\Omega \quad (14)$$

   - Choose a standard 1% value below $R_{RSET,max}$ for R_{RSET} = 80.6 kΩ
   - $I_{SET,min}$ = 2.15 A using Equation 8 meets the maximum operating current requirement of 2.1 A without starting the fault timer during maximum steady state operation for R_{RSET} = 80.6 kΩ, 1%.
   - $I_{SET,max}$ = 4.359 A using Equation 9 for R_{RSET} = 80.6 Ω, 1%.
2. Calculate minimum and maximum I_{LIM}.
   - $I_{LIM,min}$ = 2.792 A and $I_{LIM,max}$ = 4.359 A using Equation 12 and Equation 13 for R_{RSET} = 80.6 kΩ, 1%.
3. Minimum R_{LOAD} at startup using Equation 6 is 12 Ω. Because R_{LOAD} = 15 Ω is present during circuit startup, use t_{ON} = 15 ms from Table 2 for C_{LOAD} = 220 µF and R_{LOAD} = 15 Ω.
   - Calculate C_{CT} = 0.48 µF including C_{LOAD} and C_{CT} tolerances (C_{LOAD_TOL} = 20% and C_{CT_TOL} = 10%) using Equation 15.

$$C_{CT} = \frac{(1 + C_{LOAD\_TOL} + C_{T\_TOL}) \times t_{ON}}{40000} = \frac{(1 + 0.2 + 0.1) \times 0.012}{40000} = 0.48\ \mu F \quad (15)$$

9.2.2.1 Transient Protection

The need for transient protection in conjunction with hot-swap controllers must always be considered. When the TPS2421 device interrupts current flow, input inductance generates a positive voltage spike on the input and output inductance generates a negative voltage spike on the output. Such transients can easily exceed twice the supply voltage if steps are not taken to address the issue. Typical methods for addressing transients include;

- Minimizing lead length/inductance into and out of the device
- Voltage Suppressors (TVS) on the input to absorb inductive spikes
- Schottky diode across the output to absorb negative spikes
- A combination of ceramic and electrolytic capacitors on the input and output to absorb energy
- Use PCB GND planes

Equation 16 estimates the magnitude of these voltage spikes:

$$V_{SPIKE(absolute)} = V_{NOM} + I_{LOAD} \times \sqrt{L/C}$$

where

- V_{NOM} is the nominal supply voltage
- I_{LOAD} is the load current
- C is the capacitance present at the input or output of the TPS2421 device
- L equals the effective inductance seen looking into the source or the load (16)

Calculating the inductance due to a straight length of wire is shown in Equation 17.

$$L_{straightwire} \approx 0.2 \times L \times V_{VIN} \left(\frac{4 \times L}{D} - 0.75 \right) (nH)$$

where

- L is the length of the wire
- D is diameter of the wire (17)

Typical Application (continued)

Some applications may require the addition of a TVS to prevent transients from exceeding the absolute ratings if sufficient capacitance cannot be included.

9.2.3 Application Curves

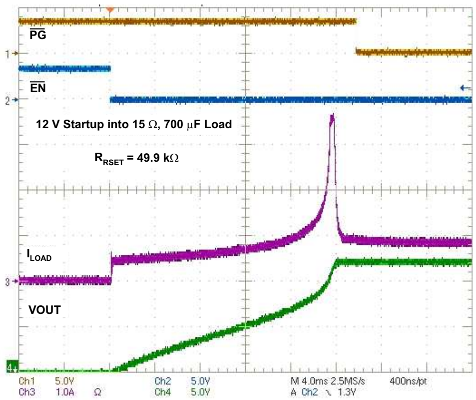


Figure 15. 12-V Startup into 15-Ω, 700-µF Load

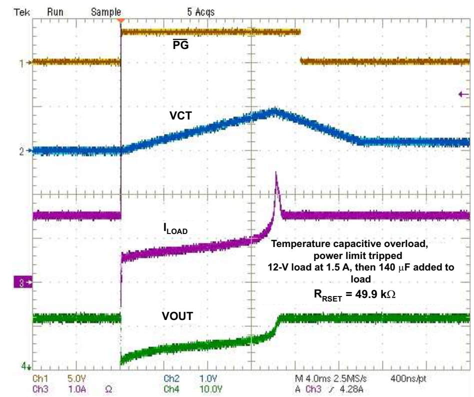


Figure 16. 12 V, 140 µF Added to 8-Ω Load

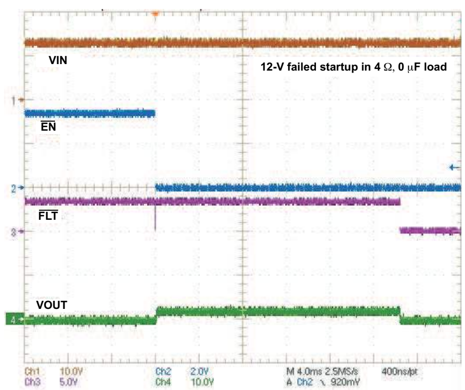


Figure 17. 12-V Faulted Startup into 4-Ω Load

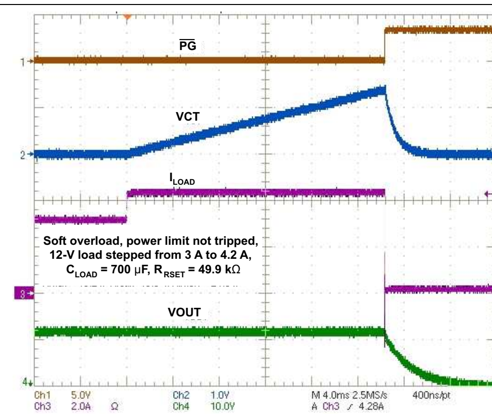


Figure 18. 12-V Soft Overload, 3 A to 4.2 A, Power Limit Not Tripped

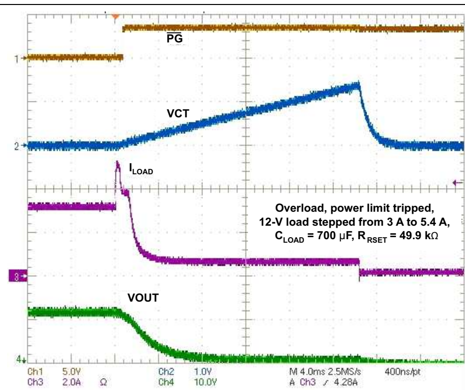


Figure 19. 12-V Firm Overload, 3 A to 5.4 A, Power Limit Tripped

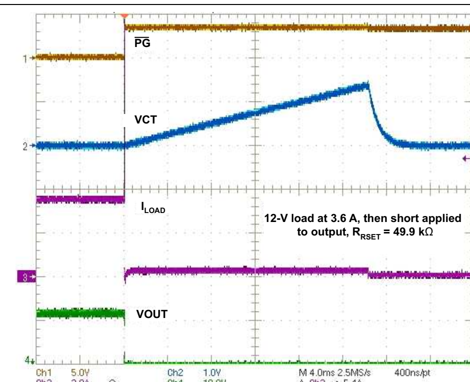


Figure 20. 12-V Hard Overload, 3.6-A Load then Short

Typical Application (continued)

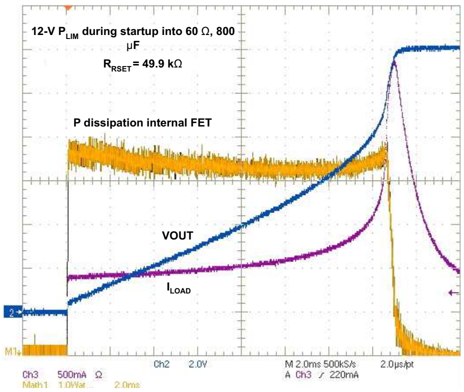


Figure 21. Power Dissipation During 12-V Startup into 60 Ω, 800 µF

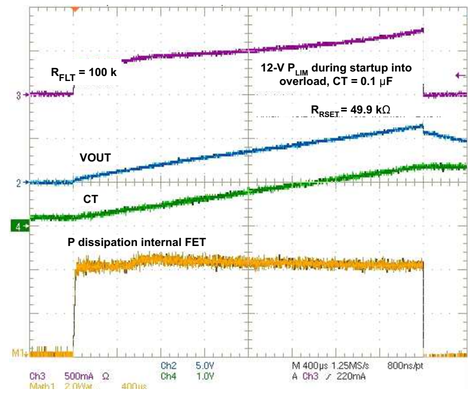


Figure 22. Power Dissipation During 12-V Startup into 15 Ω, 140 µF

10 Power Supply Recommendations

10.1 PowerPad™

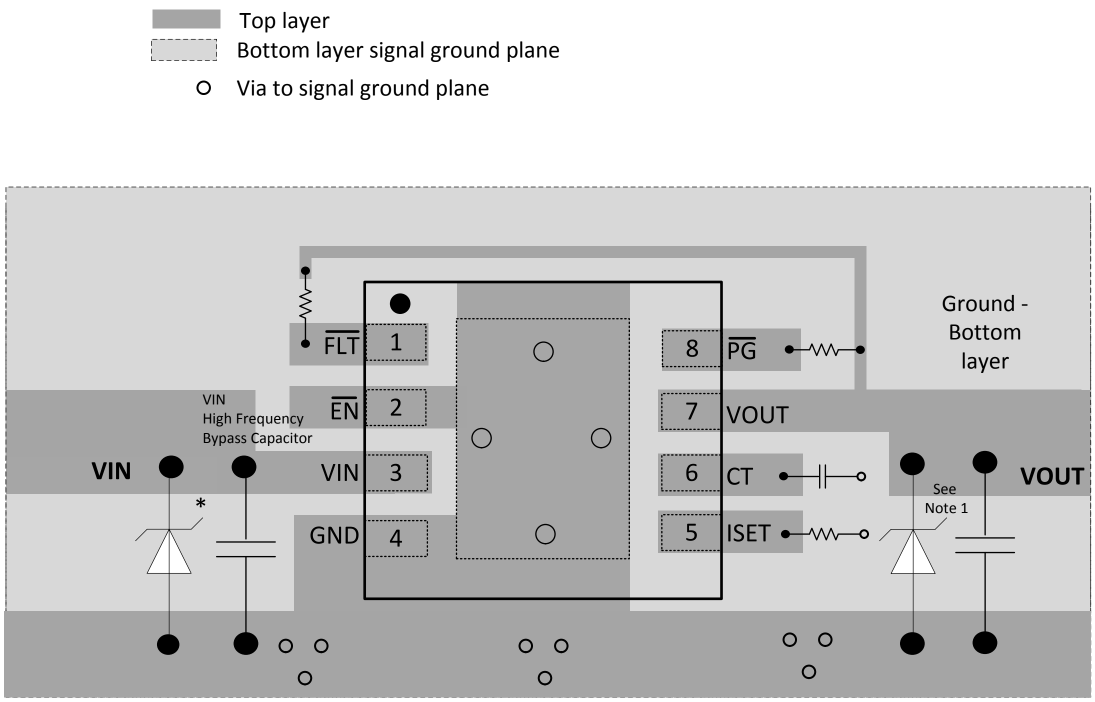
When properly mounted the PowerPad package provides significantly greater cooling ability than an ordinary package. To operate at rated power the PowerPAD must be soldered directly to the PC board GND plane directly under the device. The PowerPAD is at GND potential and can be connected using multiple vias to inner layer GND. Other planes, such a the bottom side of the circuit board can be used to increase heat sinking in higher current applications. Refer to Technical Briefs: *PowerPad™ Thermally Enhanced Package* (SLMA002) and *PowerPad™ Made Easy* (SLMA004) or more information on using this PowerPad™ package. These documents are available at www.ti.com (Search by Keyword).

11 Layout

11.1 Layout Guidelines

- Locate all TPS2421 support components, R_{RSET}, C_{CT}, or any input or output voltage clamps, close to their connection pin.
- Connect the other end of the component to the inner layer GND without trace length.
- The trace routing the R_{RSET} resistor to the TPS2421 device must be as short as possible to reduce parasitic effects on fault and current-limit accuracy.

11.2 Layout Example



(1) Optional: Needed only to suppress the transients caused by inductive load switching.

Figure 23. Layout

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

Using the TPS2420, TPS2421-1, TPS2421-2

12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 3. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS2421-1	Click here	Click here	Click here	Click here	Click here
TPS2421-2	Click here	Click here	Click here	Click here	Click here

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates—including silicon errata—go to the product folder for your device on ti.com. In the upper right-hand corner, click the *Alert me* button. This registers you to receive a weekly digest of product information that has changed (if any). For change details, check the revision history of any revised document.

12.4 Community Resource

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.5 Trademarks

PowerPad, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

12.6 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS2421-1DDA	ACTIVE	SO PowerPAD	DDA	8	75	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	2421-1	Samples
TPS2421-1DDAR	ACTIVE	SO PowerPAD	DDA	8	2500	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	2421-1	Samples
TPS2421-2DDA	ACTIVE	SO PowerPAD	DDA	8	75	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	2421-2	Samples
TPS2421-2DDAR	ACTIVE	SO PowerPAD	DDA	8	2500	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	2421-2	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

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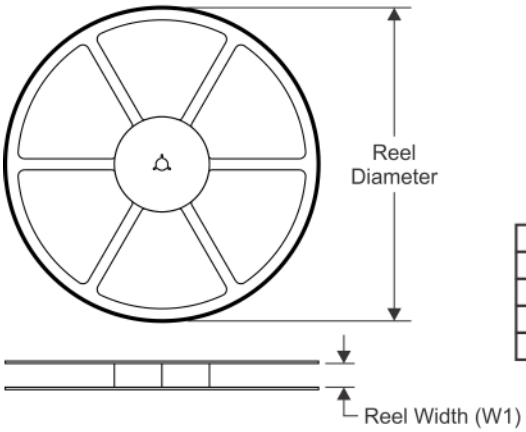
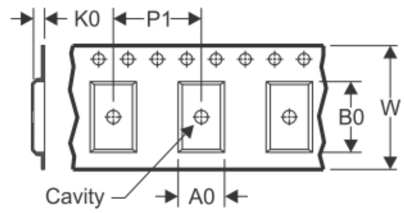
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

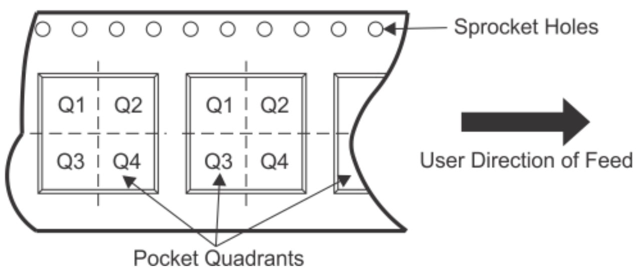


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

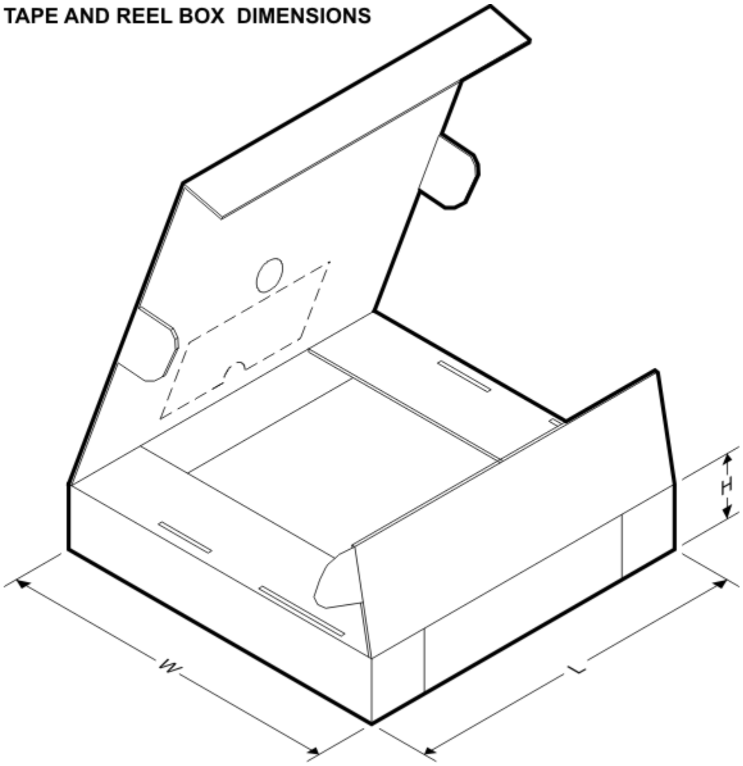
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS2421-1DDAR	SO Power PAD	DDA	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
TPS2421-2DDAR	SO Power PAD	DDA	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1

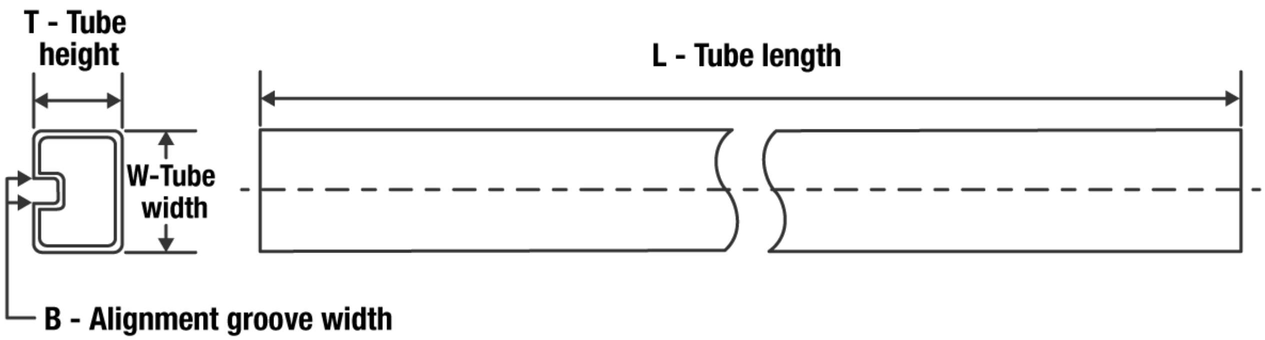
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS2421-1DDAR	SO PowerPAD	DDA	8	2500	364.0	364.0	27.0
TPS2421-2DDAR	SO PowerPAD	DDA	8	2500	364.0	364.0	27.0

TUBE

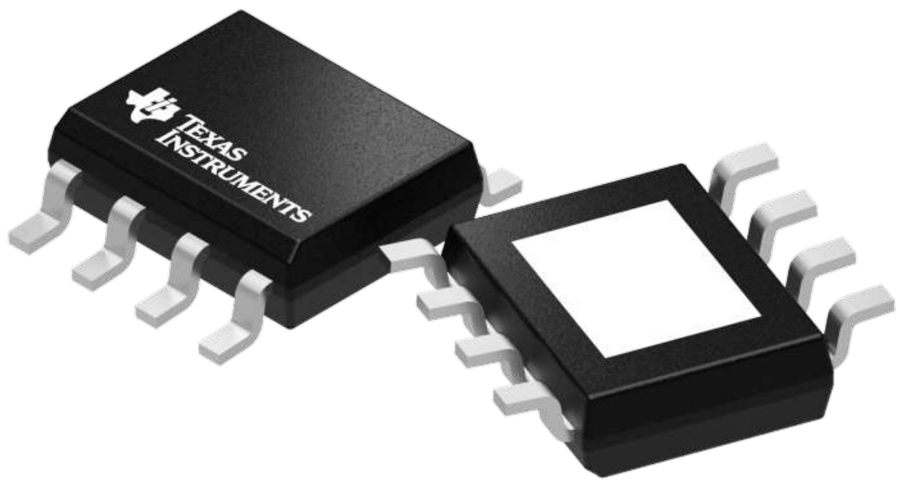


*All dimensions are nominal

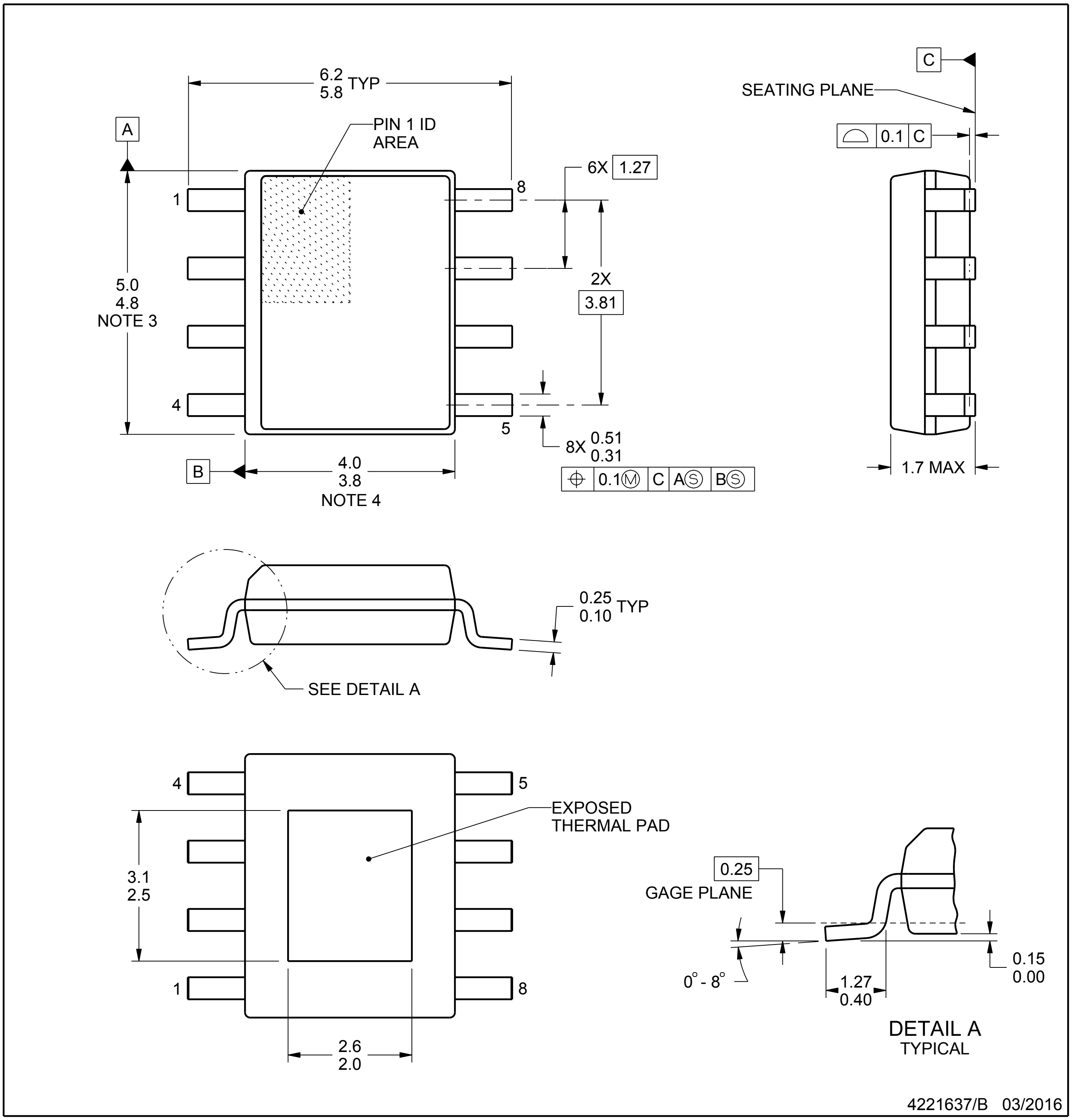
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPS2421-1DDA	DDA	HSOIC	8	75	390	7.8	3800	3.5
TPS2421-1DDA	DDA	HSOIC	8	75	517	7.87	635	4.25
TPS2421-2DDA	DDA	HSOIC	8	75	517	7.87	635	4.25
TPS2421-2DDA	DDA	HSOIC	8	75	390	7.8	3800	3.5

DDA 8 PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



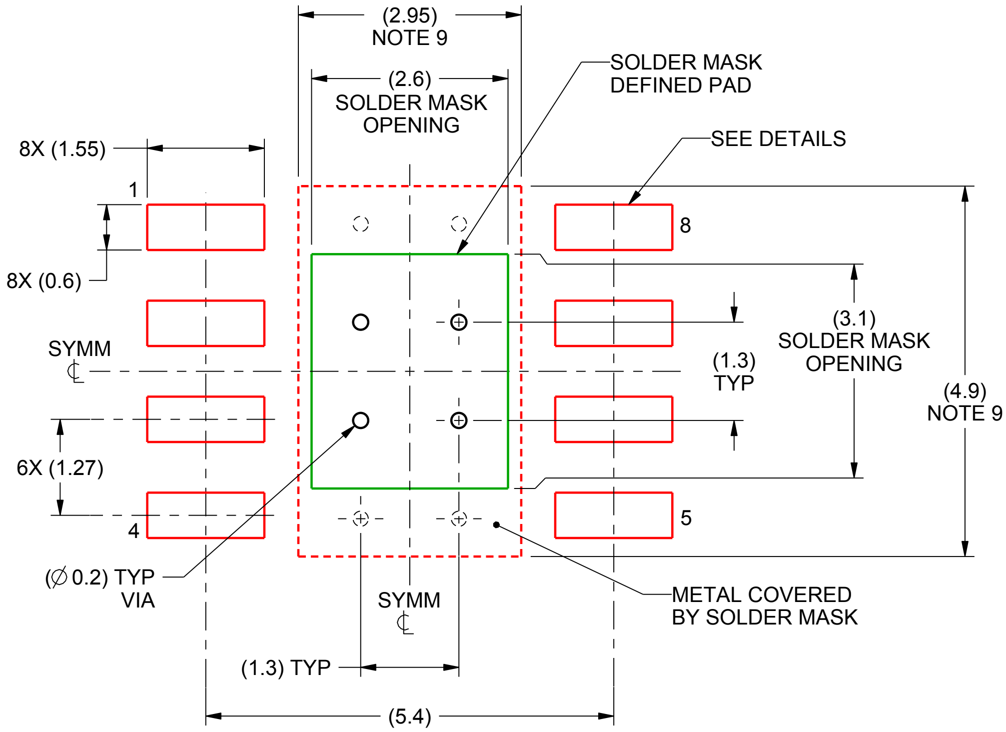
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



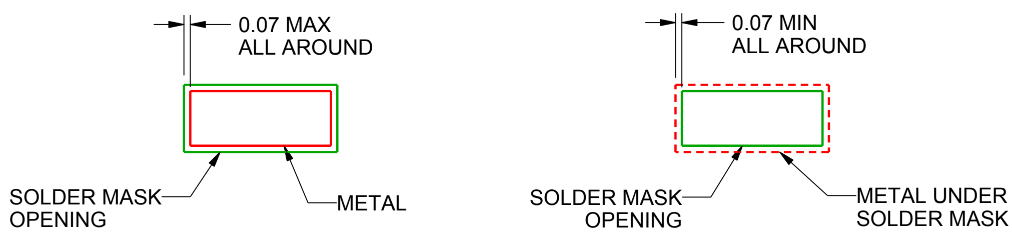
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MS-012, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X



NON SOLDER MASK
DEFINED

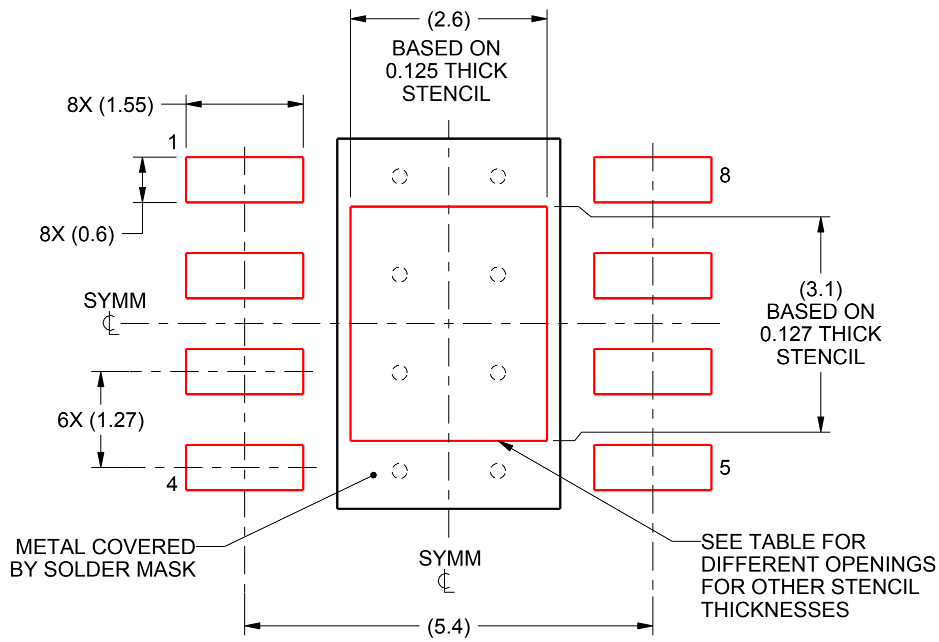
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4221637/B 03/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.91 X 3.47
0.125	2.6 X 3.1 (SHOWN)
0.150	2.37 X 2.83
0.175	2.20 X 2.62

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NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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