



# FDMC86520L

## N-Channel Power Trench<sup>®</sup> MOSFET

60 V, 22 A, 7.9 mΩ

### Features

- Max  $r_{DS(on)}$  = 7.9 mΩ at  $V_{GS} = 10$  V,  $I_D = 13.5$  A
- Max  $r_{DS(on)}$  = 11.7 mΩ at  $V_{GS} = 4.5$  V,  $I_D = 11.5$  A
- Low Profile - 1 mm max in Power 33
- 100% UIL Tested
- RoHS Compliant

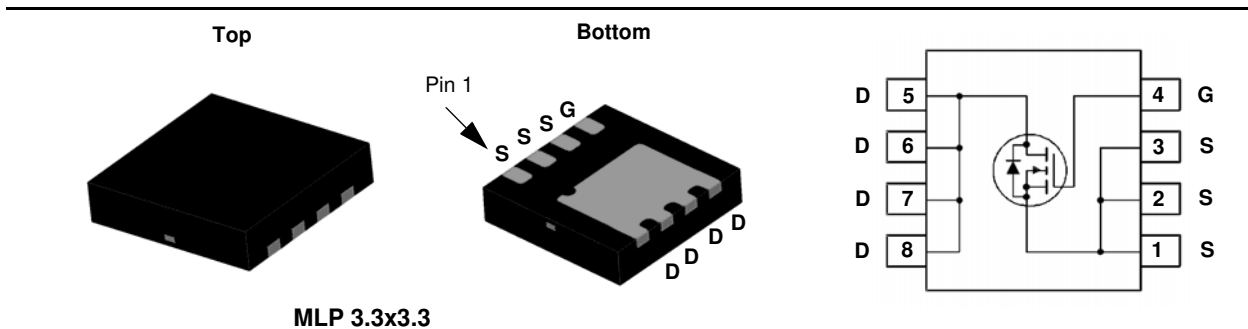


### General Description

This N-Channel MOSFET has been designed specifically to improve the overall efficiency and to minimize switch node ringing of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low  $r_{DS(on)}$ , fast switching speed and body diode reverse recovery performance.

### Applications

- Primary Switch in isolated DC-DC
- Synchronous Rectifier
- Load Switch



### MOSFET Maximum Ratings $T_A = 25$ °C unless otherwise noted

Symbol	Parameter	Ratings	Units	
$V_{DS}$	Drain to Source Voltage	60	V	
$V_{GS}$	Gate to Source Voltage	±20	V	
$I_D$	Drain Current -Continuous	$T_C = 25$ °C	A	
	-Continuous	$T_A = 25$ °C (Note 1a)		
	-Pulsed	60		
$E_{AS}$	Single Pulse Avalanche Energy	(Note 3)	79	mJ
$P_D$	Power Dissipation	$T_C = 25$ °C	40	W
	Power Dissipation	$T_A = 25$ °C (Note 1a)	2.3	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	°C	

### Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	3.1	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a) 53	

### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMC86520L	FDMC86520L	Power 33	13 "	12 mm	3000 units

## Electrical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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### Off Characteristics

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250\text{ }\mu\text{A}$ , $V_{GS} = 0\text{ V}$	60			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$		29		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 48\text{ V}$ , $V_{GS} = 0\text{ V}$			1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{ V}$ , $V_{DS} = 0\text{ V}$			$\pm 100$	nA

### On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$ , $I_D = 250\text{ }\mu\text{A}$	1	1.7	3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$		-7		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{ V}$ , $I_D = 13.5\text{ A}$		6.5	7.9	m $\Omega$
		$V_{GS} = 4.5\text{ V}$ , $I_D = 11.5\text{ A}$		9.1	11.7	
		$V_{GS} = 10\text{ V}$ , $I_D = 13.5\text{ A}$ , $T_J = 125\text{ }^\circ\text{C}$		9	11	
$g_{FS}$	Forward Transconductance	$V_{DS} = 5\text{ V}$ , $I_D = 13.5\text{ A}$		49		S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 30\text{ V}$ , $V_{GS} = 0\text{ V}$ , $f = 1\text{ MHz}$		3420	4550	pF
$C_{oss}$	Output Capacitance			638	850	pF
$C_{rss}$	Reverse Transfer Capacitance			25	40	pF
$R_g$	Gate Resistance			0.5		$\Omega$

### Switching Characteristics

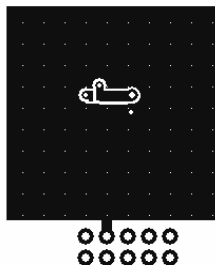
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 30\text{ V}$ , $I_D = 13.5\text{ A}$ , $V_{GS} = 10\text{ V}$ , $R_{GEN} = 6\text{ }\Omega$		15	30	ns	
$t_r$	Rise Time			5.2	10	ns	
$t_{d(off)}$	Turn-Off Delay Time			32	55	ns	
$t_f$	Fall Time			3.4	10	ns	
$Q_{g(TOT)}$	Total Gate Charge		$V_{GS} = 0\text{ V to } 10\text{ V}$		45	64	nC
$Q_{g(TOT)}$	Total Gate Charge	$V_{GS} = 0\text{ V to } 4.5\text{ V}$	$V_{DD} = 30\text{ V}$ , $I_D = 13.5\text{ A}$		21	30	nC
$Q_{gs}$	Total Gate Charge				9.6		nC
$Q_{gd}$	Gate to Drain "Miller" Charge				4.9		nC

### Drain-Source Diode Characteristics

$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}$ , $I_S = 13.5\text{ A}$ (Note 2)		0.82	1.3	V
		$V_{GS} = 0\text{ V}$ , $I_S = 2\text{ A}$ (Note 2)		0.71	1.2	
$t_{rr}$	Reverse Recovery Time	$I_F = 13.5\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$		38	62	ns
$Q_{rr}$	Reverse Recovery Charge			21	34	nC

#### NOTES:

- $R_{\theta JA}$  is determined with the device mounted on a 1 in<sup>2</sup> pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



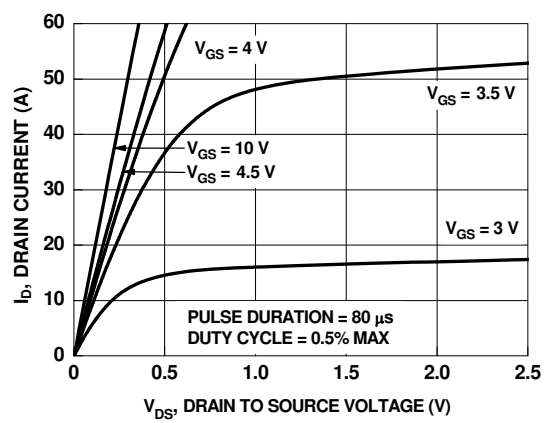
53  $^\circ\text{C}/\text{W}$  when mounted on a  
1 in<sup>2</sup> pad of 2 oz copper



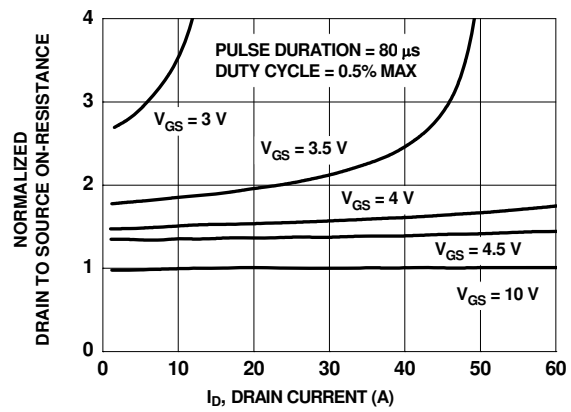
125  $^\circ\text{C}/\text{W}$  when mounted on  
a minimum pad of 2 oz copper

- Pulse Test: Pulse Width < 300  $\mu\text{s}$ , Duty cycle < 2.0%.
- Starting  $T_J = 25\text{ }^\circ\text{C}$ ; N-ch: L = 0.3 mH,  $I_{AS} = 23\text{ A}$ ,  $V_{DD} = 54\text{ V}$ ,  $V_{GS} = 10\text{ V}$ .

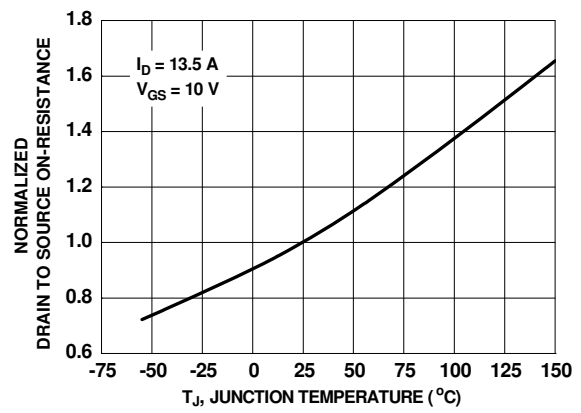
**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



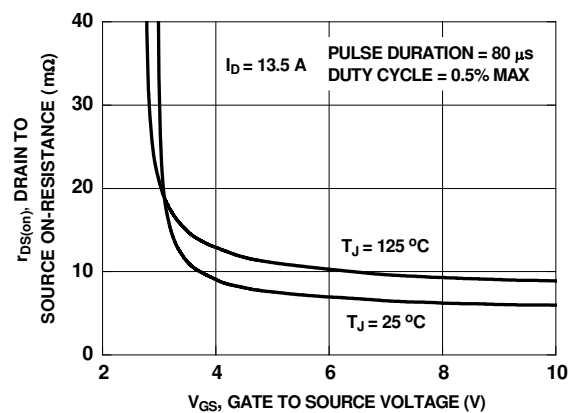
**Figure 1. On Region Characteristics**



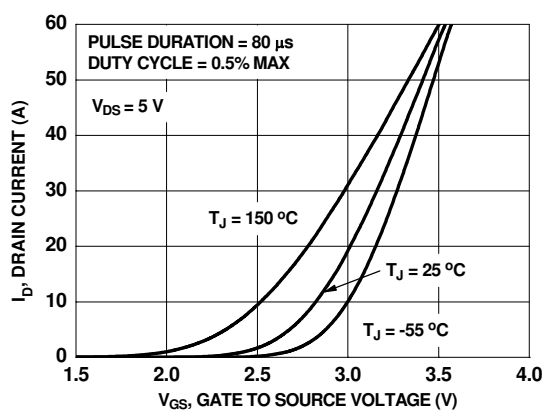
**Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage**



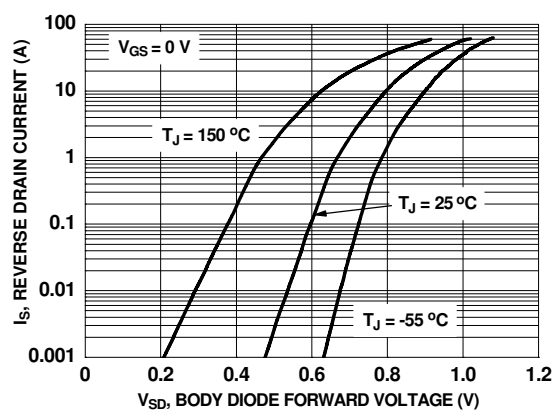
**Figure 3. Normalized On Resistance vs. Junction Temperature**



**Figure 4. On-Resistance vs. Gate to Source Voltage**

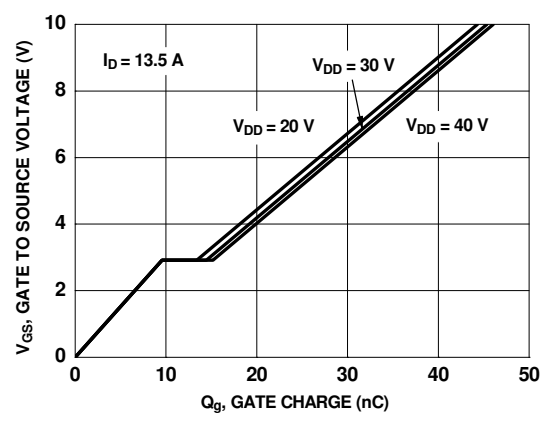


**Figure 5. Transfer Characteristics**

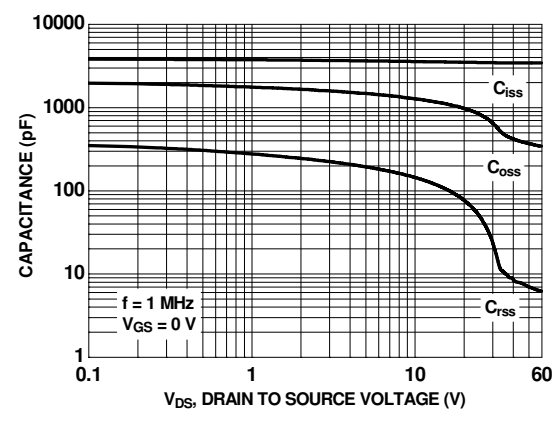


**Figure 6. Source to Drain Diode Forward Voltage vs. Source Current**

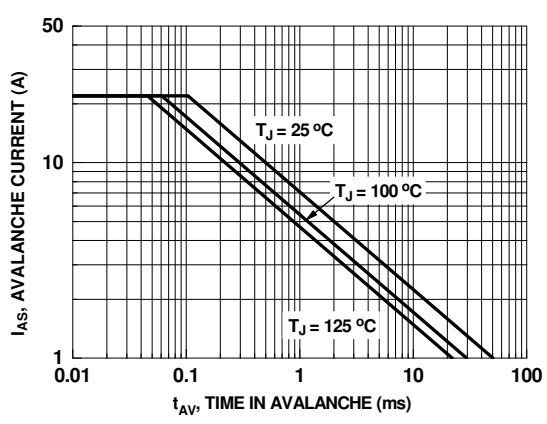
**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



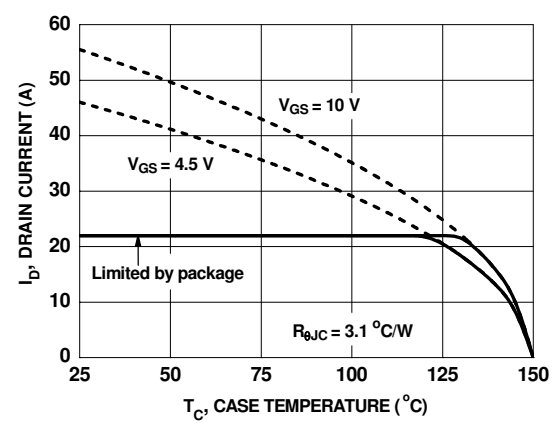
**Figure 7. Gate Charge Characteristics**



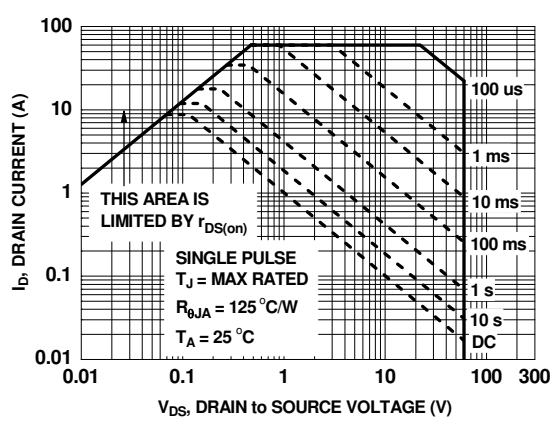
**Figure 8. Capacitance vs. Drain to Source Voltage**



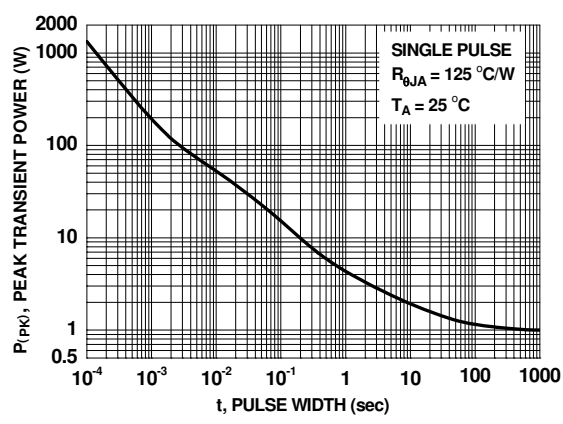
**Figure 9. Unclamped Inductive Switching Capability**



**Figure 10. Maximum Continuous Drain Current vs. Case Temperature**

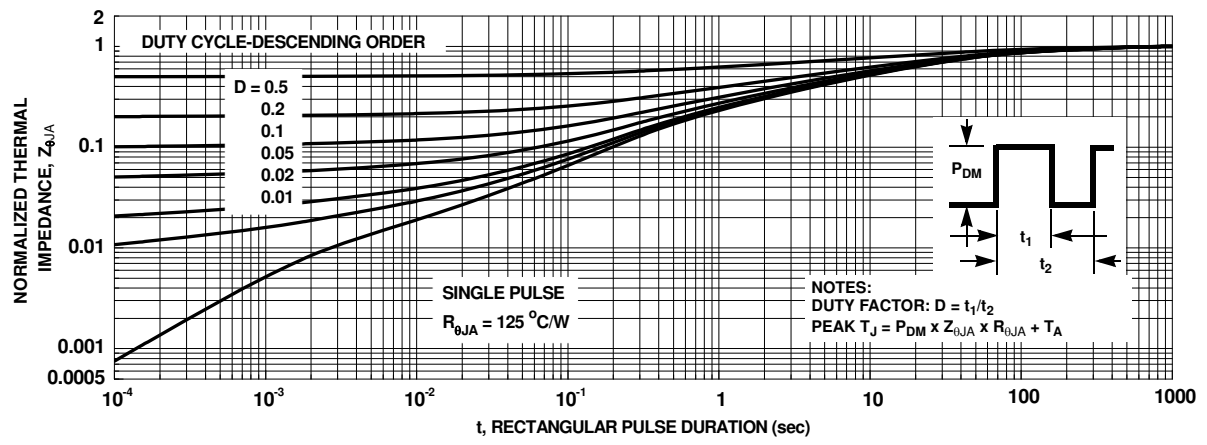


**Figure 11. Forward Bias Safe Operating Area**



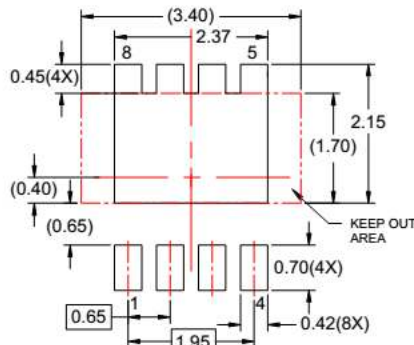
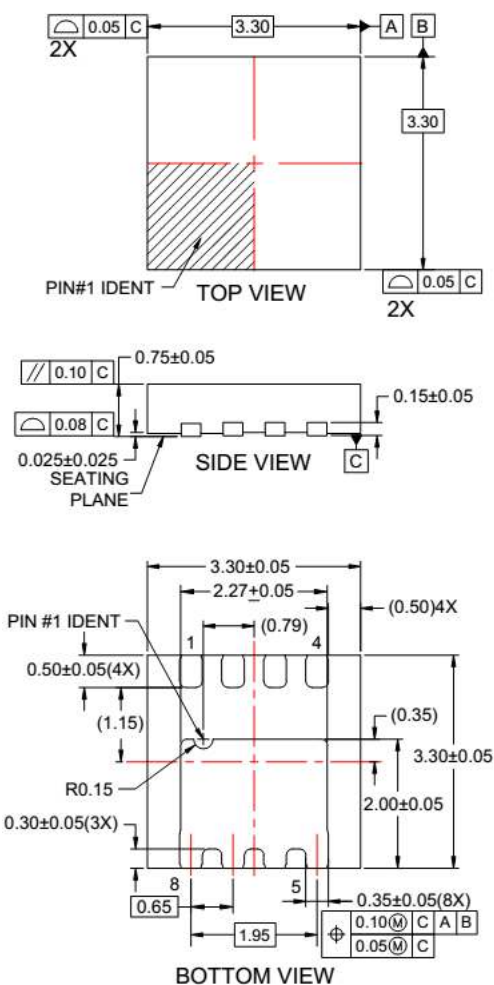
**Figure 12. Single Pulse Maximum Power Dissipation**

**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



**Figure 13. Junction-to-Ambient Transient Thermal Response Curve**

## Dimensional Outline and Pad Layout



RECOMMENDED LAND PATTERN

### NOTES:

- A. DOES NOT CONFORM TO JEDEC REGISTRATION MO-229
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
- D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.
- E. DRAWING FILENAME: MKT-MLP08Srev3.








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