*User's Guide*

# *LM2727 Buck Controller Evaluation Module User's Guide*

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# 1 Introduction

The LM2727 evaluation board has been designed for a wide variety of components in order to show the flexibility of the LM2727 chips. The input voltage limitations are the same as the chip: 2.2 $V_{DC}$ to 16 $V_{DC}$. The regulated output voltage range is from 0.6 V up to 85% of the input voltage. Output current is limited by the components chosen, however, the size of this board and the limitation to SOIC-8 MOSFETs means a realistic limit of about 10 A.

The example design steps 12 V down to 3.3 V at 4 A, with a switching frequency of 800 kHz. This design can be modified by following the *Design Considerations* section of the *LM2727/LM2737 N-Channel FET Synchronous Buck Regulator Controller for Low Output Voltages* data sheet.

The board is four layers, consisting of signal/power traces on top and bottom, with one internal ground plane and an internal split power plane. All planes are 1-oz. copper, and the board is 62-mil FR4 laminate.

# 2 Boot Voltage

The default circuit that comes with the LM2727 demo board uses a bootstrap diode and small capacitor (D1 and $C_{BOOT}$) to provide enough gate-to-source voltage on the high-side MOSFET to drive the FET. If a separate rail is available that is more than twice the value of $V_{IN}$, this higher voltage can be connected directly to the BOOT pin, through the BOOT connector, with a 0.1-µF bypass capacitor, $C_C$. In this case, D1 and $C_{BOOT}$ should be removed from the board. Do not connect both $C_C$ and $C_{BOOT}$/D1 at the same time.

# 3 Dual MOSFET Footprints

The LM2727 demo board has two extra footprints for dual N-channel MOSFETs in SOIC-8 packages. Footprint Q3 corresponds to devices with footprints such as the Si4816DY "LITTLEFOOT Plus" from Vishay Siliconix. Footprint Q4 corresponds to devices with footprints such as the Si4826DY, also from Vishay Siliconix.

# 4 Low-Side Diode

A footprint D2 is available for a Schottky diode to be placed in parallel with the low-side FET. This can improve efficiency because a discrete Schottky will have a lower forward voltage than the bodu diode of the low-side FET. The footprint fits SMA size devices. If desired, the low side FET can be removed entirely, and the LM2727 will run as an asynchronous buck controller.

# 5 Additional Footprints

The 1206 footprints Rc2 and Cc3 are available for designs with more complex compensation needs.

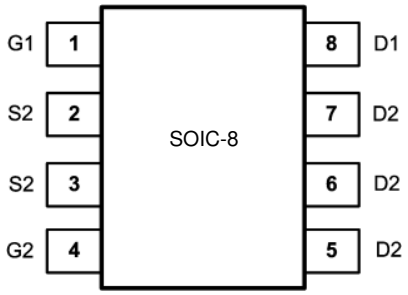


**Figure 5-1. Pinout for Dual FET for Footprint Q3**

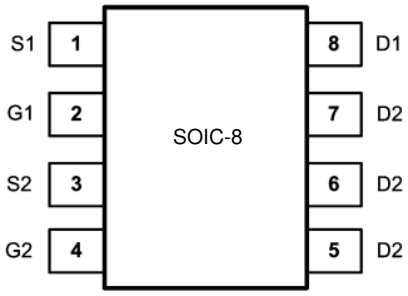


**Figure 5-2. Pinout for Dual FET for Footprint Q4**

## 6 Layout Optimization

The LM2727 PCB layout could be improved with several techniques used in switching converter design. The traces that run from the HG and LG pins of the IC to the gates of the high-side and low-side MOSFETs should be shorter and thicker, reducing their parasitic inductance and resistance. The mid-frequency decoupling capacitor, $C_{INX}$, should be placed as close to the pins of the high-side MOSFET as possible. The bulk input capacitors, $C_{IN1}$ and $C_{IN2}$, should also be placed close, keeping the loop between the input capacitors and the high-side MOSFET small. Likewise, the Schottky diode D2 should be located as close as possible to the pins of the low-side MOSFET. The local capacitors $C_{IN}$, $C_{BOOT}$, and $C_C$ (if used) should be close to the pins of the LM2727 IC. These techniques help reduce parasitic inductance throughout the PCB.

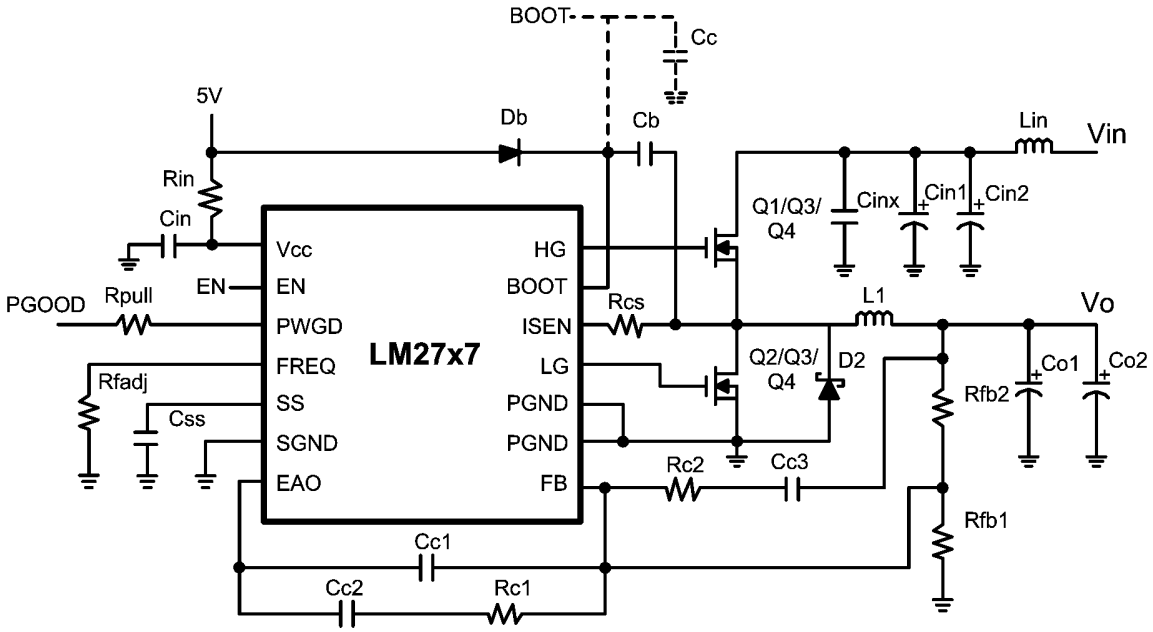


**Figure 6-1. Circuit Schematic**

**Table 6-1. Bill of Materials for Typical Application Circuit**

| ID | Part Number | Type | Size | Parameters | Qty. | Vendor |
|---|---|---|---|---|---|---|
| U1 | LM2727 | Synchronous Controller | TSSOP-14 | | 1 | NSC |
| Q1 | Si4884DY | N-MOSFET | SOIC-8 | 13.5 mΩ, at 4.5 V, 15.3 nC | 1 | Vishay |
| Q2 | Si4884DY | N-MOSFET | SOIC-8 | 13.5 mΩ, at 4.5 V, 15.3 nC | 1 | Vishay |
| Db | BAT-54 | Schottky Diode | SOT-23 | 30 V | 1 | ON |
| Lin | P1168.162T | Inductor | 12 × 12 × 4.5 mm | 1.6 µH, 8.5 A, 5.4 mΩ | 1 | Pulse |
| L1 | P1168.162T | Inductor | 12 × 12 × 4.5 mm | 1.6 µH, 8.5 A, 5.4 mΩ | 1 | Pulse |
| Cin1 | C4532X5R1E106M | Capacitor | 1812 | 10 µF, 25 V, 3.3 Arms | 2 | TDK |
| Cinx | C3216X7R1E105K | Capacitor | 1206 | 1 µF, 25 V | 1 | TDK |
| Co1 | 6TPB470M | Capacitor | 7.3 × 4.3 × 3.8 mm | 470 µF, 2.5 V, 55 mΩ | 2 | Sanyo |
| Cin | C3216X7R1E225K | Capacitor | 1206 | 2.2 µF, 25 V | 1 | TDK |
| Css | VJ1206X123KXX | Capacitor | 1206 | 12 nF, 25 V | 1 | Vishay |
| Cc1 | VJ1206A3R9KXX | Capacitor | 1206 | 3.9 pF, 10% | 1 | Vishay |
| Cc2 | VJ1206A391KXX | Capacitor | 1206 | 390 pF, 10% | 1 | Vishay |
| Rin | CRCW1206100J | Resistor | 1206 | 10 Ω, 5% | 1 | Vishay |
| Rfadj | CRCW12063052F | Resistor | 1206 | 30.5 kΩ, 1% | 1 | Vishay |
| Rc1 | CRCW12069532F | Resistor | 1206 | 95.3 kΩ, 1% | 1 | Vishay |
| Rfb1 | CRCW12064871F | Resistor | 1206 | 4.87 kΩ, 1% | 1 | Vishay |
| Rfb2 | CRCW12062181F | Resistor | 1206 | 21.8 kΩ, 1% | 1 | Vishay |
| Rcs | CRCW1206272J | Resistor | 1206 | 2.7 kΩ, 5% | 1 | Vishay |

# 7 PCB Layout

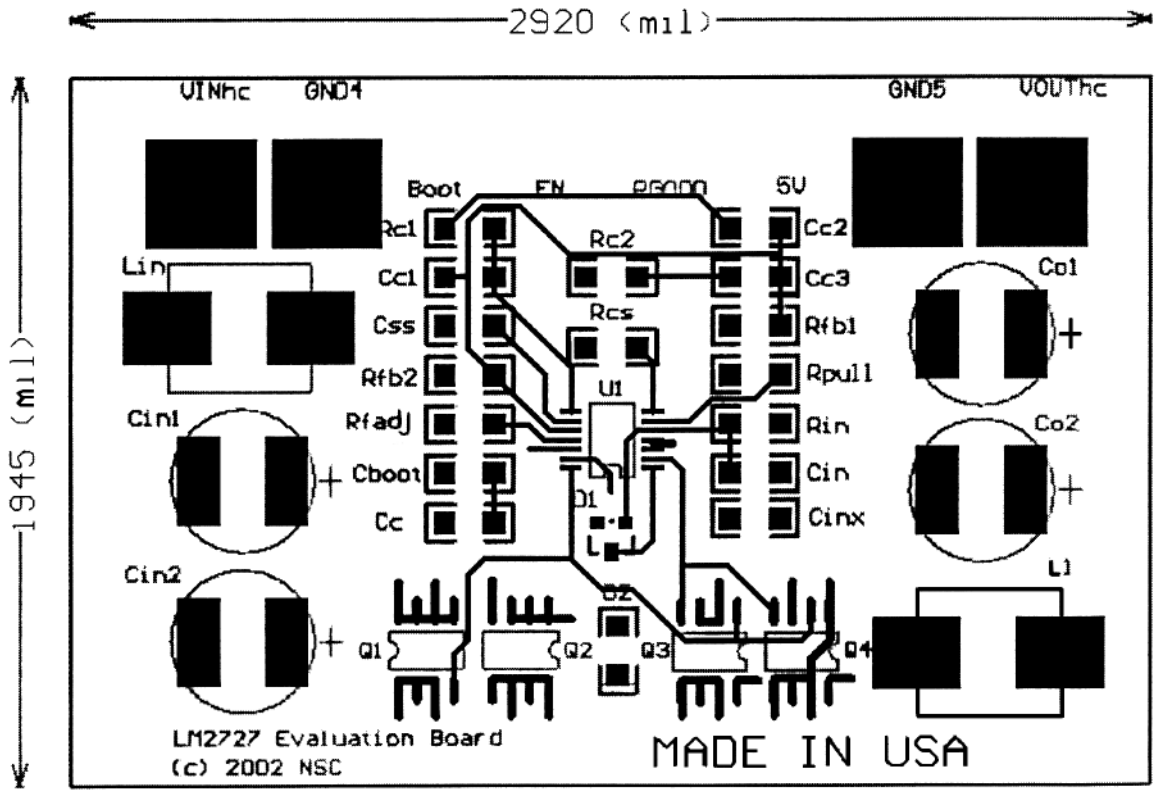


**Figure 7-1. PCB Top Layer and Top Overlay**

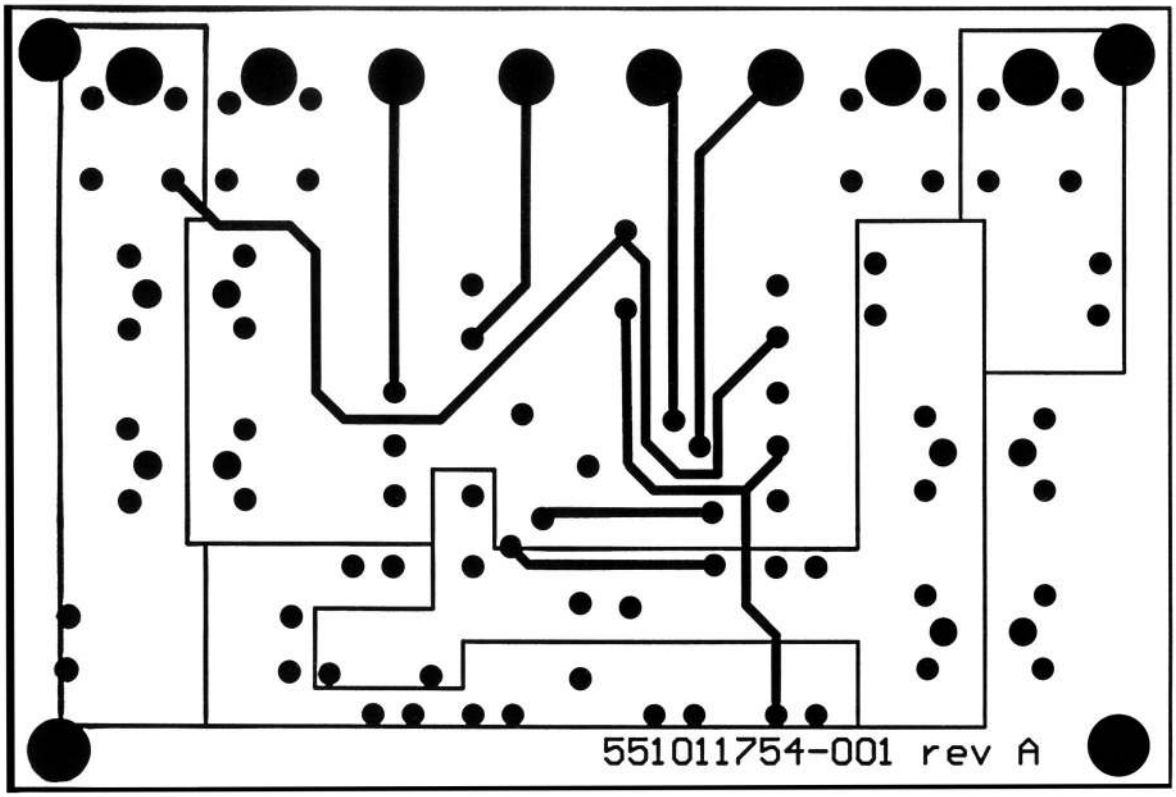


**Figure 7-2. PCB Bottom Layer and Internal Power Plane**

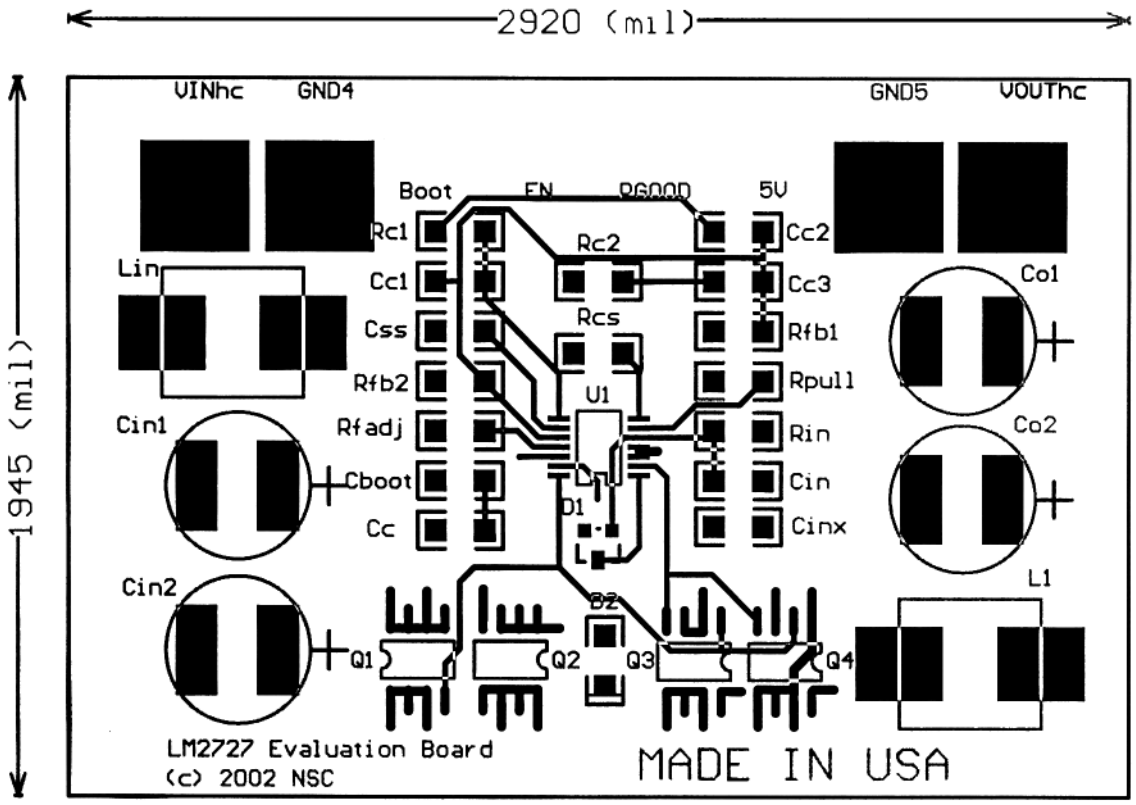


**Figure 7-3. PCB Overall**

## 8 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision C (April 2013) to Revision D (February 2022) | Page |
|---|---|
| • Updated the numbering format for tables, figures, and cross-references throughout the document. | 2 |
| • Updated the user's guide title. | 2 |

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