

TPS54388EVM User's Guide

The TPS54388-Q1 DC-DC converter is designed to provide up to a 3-A output from an input voltage source of 2.95 V to 6 V. [Table 1](#) lists the ratings for the input-voltage and output-current range of the evaluation module (EVM). This evaluation module is designed to demonstrate the small printed-circuit-board (PCB) areas that can be achieved when designing with the TPS54388-Q1 regulator. The switching frequency is externally set at a nominal 2000 kHz. The high-side and low-side MOSFETs are incorporated inside the TPS54388-Q1 device to achieve high efficiencies and to maintain a low junction temperature at high output currents. The compensation components are external to the integrated circuit (IC) and have been selected to optimize the transient performance of the device. An external divider allows for an adjustable output voltage. Additionally, the TPS54388-Q1 device provides adjustable slow-start and undervoltage lockout inputs. The absolute-maximum input voltage is 7 V for the TPS54388EVM.

Table 1. Input Voltage and Output Current Summary

EVM	Input Voltage Range	Output current Range
TPS54388EVM	$V_{IN} = 3\text{ V to }6\text{ V}$	0 A to 3 A

Contents

1	Performance-Specification Summary	2
2	Test Setup and Results	3
3	Board Layout	8
4	Schematic and Bill of Materials	11

List of Figures

1	TPS54388EVM Efficiency.....	4
2	TPS54388EVM Load Regulation	4
3	TPS54388EVM Line Regulation	5
4	TPS54388EVM Load Transient.....	5
5	TPS54388EVM Loop-Response Measurement.....	6
6	TPS54388EVM Output Ripple	6
7	TPS54388EVM Startup Relative to V_{IN}	7
8	TPS54388EVM Startup Relative to Enable.....	7
9	TPS54388EVM Top-Side Layout	8
10	TPS54388EVM Bottom-Side Layout	9
11	TPS54388EVM Top-Side Assembly.....	9
12	TPS54388EVM Bottom-Side Assembly	10
13	TPS54388EVM Schematic	11

List of Tables

1	Input Voltage and Output Current Summary	1
2	TPS54388EVM Performance-Specification Summary	2
3	Common Output-Voltage Options	2
4	EVM Connectors and Test Points	3
5	TPS54388EVM Bill of Materials	12

1 Performance-Specification Summary

Table 2 lists a summary of the TPS54388EVM performance specifications. Specifications are given for an input voltage of $V_{IN} = 5\text{ V}$ and an output voltage of 1.2 V, unless otherwise specified. The ambient temperature is 25°C for all measurements, unless otherwise noted.

Table 2. TPS54388EVM Performance-Specification Summary

SPECIFICATION	TEST CONDITION	MIN	TYP	MAX	UNIT
V_{IN} operating voltage range		3	5	6	V
V_{IN} start voltage			2.84		V
V_{IN} stop voltage			2.68		V
Output voltage set point			1.2		V
Output current range	$V_{IN} = 3\text{ V to }6\text{ V}$	0		3	A
Line regulation	$I_O = 1\text{ A}, V_{IN} = 3\text{ V to }6\text{ V}$		±0.1%		
Load regulation	$V_{IN} = 3.3\text{ V}, I_O = 0\text{ A to }3\text{ A}$		±0.15%		
Load transient response	$I_O = 0.75\text{ A to }2.25\text{ A}$	Voltage change		-30	mV
		Recovery time		70	µs
	$I_O = 2.25\text{ A to }0.75\text{ A}$	Voltage change		30	mV
		Recovery time		80	µs
Loop bandwidth	$V_{IN} = 5\text{ V}, I_O = 2.25\text{ A}$		88		kHz
Phase margin	$V_{IN} = 5\text{ V}, I_O = 2.25\text{ A}$		42		°
Output ripple voltage	$I_O = 3\text{ A}$		10		mVpp
Output rise time			4		ms
Operating frequency			2000		kHz
Maximum efficiency	$V_{IN} = 3.3\text{ V}, I_O = 1.6\text{ A}$		86%		

1.1 Modifications

This EVM is designed to provide access to the features of the TPS54388-Q1 device. Some modifications can be made to the module.

1.1.1 Output Voltage Set-Point

The voltage dividers R_5 and R_7 set the output voltage. To change the output voltage of the EVM, changing the value of resistor R_5 is necessary. Changing the value of R_5 changes the output voltage above 0.8 V. The value of R_5 for a specific output voltage is calculated using Equation 1.

$$R_5 = 80.6\text{ k}\Omega \times \frac{V_{OUT} - V_{REF}}{V_{REF}} \quad (1)$$

Table 3 lists the R_5 values for some common output voltages. Note that V_{IN} must be in a range so that the minimum on-time is greater than 75 ns, and the maximum duty cycle is less than 92%. The values given in Table 3 are standard values and are not the exact value calculated using Equation 1.

Table 3. Common Output-Voltage Options

Output Voltage (V)	R_5 Value (kΩ)
1	20
1.2	40.2
1.5	71.5
1.8	100
2.5	174
3.3	249

1.1.2 Slow-Start Time

The slow-start time is adjusted by changing the value of C_{15} . Equation 2 calculates the required value of C_{15} for a desired slow-start time.

$$C_{15} \text{ (nF)} = \frac{T_{SS} \text{ (ms)} \times I_{SS} \text{ (\mu A)}}{V_{REF} \text{ (V)}}$$

where

- $I_{SS} = 2 \mu\text{A}$ (2)

C_{15} is set to 0.01 μF on the EVM for a default slow-start time of 4 ms.

1.1.3 Adjustable Undervoltage Lockout

The undervoltage lockout (UVLO) is adjusted externally using R_3 and R_4 . The EVM is set for a start voltage of 2.84 V and a stop voltage of 2.68 V using $R_3 = 25.5 \text{ k}\Omega$ and $R_2 = 20 \text{ k}\Omega$. Use Equation 3 and Equation 4 along with notes included in the TPS54388-Q1 data sheet ([SLVSAF1](#)) to calculate required resistor values for different start and stop voltages.

$$R_3 = \frac{0.944 \times V_{START} - V_{STOP}}{1.71 \times 10^{-6}} \quad (3)$$

$$R_4 = \frac{1.18 \times R_3}{V_{STOP} - 1.18 + R_3 \times 3.5 \times 10^{-6}} \quad (4)$$

2 Test Setup and Results

This section describes how to properly connect, set up, and use the TPS54388EVM evaluation module. Test results typical of this evaluation module are also included. This section covers efficiency, output voltage regulation, load transients, loop response, output ripple, and startup.

2.1 Input and Output Connections

The TPS54388EVM is provided with input and output connectors and test points as shown in Table 4. A power supply capable supplying 3 A must be connected to J1 through a pair of 20-AWG wires. The load must be connected to J2 through a pair of 20-AWG wires. The maximum load-current capability must be at least 3 A to use the full capability of this EVM. Wire lengths must be minimized to reduce losses in the wires. Test-point TP1 provides a place to monitor the V_{IN} input voltages with TP2 providing a convenient ground reference. TP3 monitors the output voltage with TP4 as the ground reference.

Table 4. EVM Connectors and Test Points

Reference Designator	Function
J1	V_{IN} (see Table 1 for V_{IN} range)
J2	V_{OUT} , 1.2 V at 2 A maximum
JP1	2-pin header for enable. Connect EN to ground to disable, open to enable
TP1	V_{IN} test point at V_{IN} connector
TP2	GND test point at V_{IN}
TP3	V_{OUT} test point at V_{OUT} connector
TP4	GND test point at V_{OUT}
TP5	Test point between voltage divider network and output. Used for loop response measurements
TP6	COMP test point

2.2 Efficiency

Figure 1 shows the efficiency for the TPS54388EVM at two different input voltages and at an ambient temperature of 25°C.

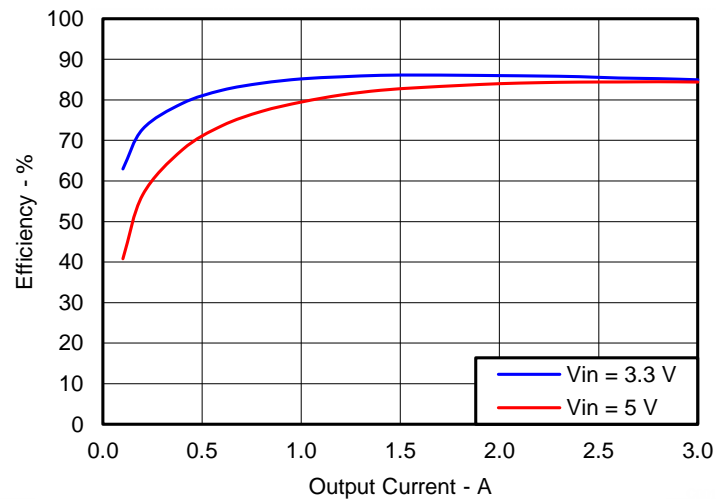


Figure 1. TPS54388EVM Efficiency

2.3 Output-Voltage Load Regulation

Figure 2 shows the load regulation for the TPS54388EVM at two different input voltages.

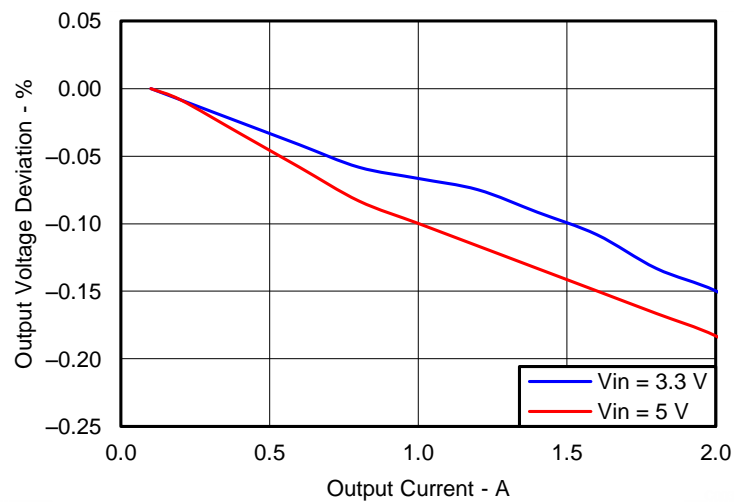


Figure 2. TPS54388EVM Load Regulation

2.4 Output-Voltage Line Regulation

Figure 3 shows the line regulation for the TPS54388EVM at room temperature and $I_{LOAD} = 1.5\text{ A}$.

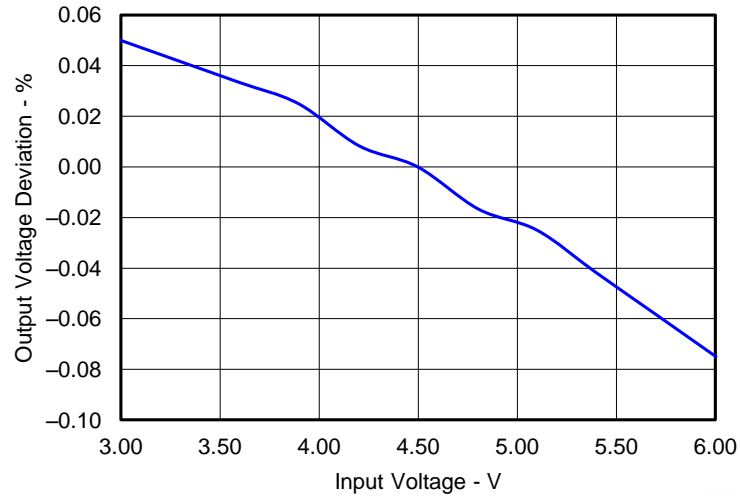


Figure 3. TPS54388EVM Line Regulation

2.5 Load Transients

Figure 4 shows the TPS54388EVM response to a load step. The current step is from 25% to 75% of maximum rated load at 5 V input.

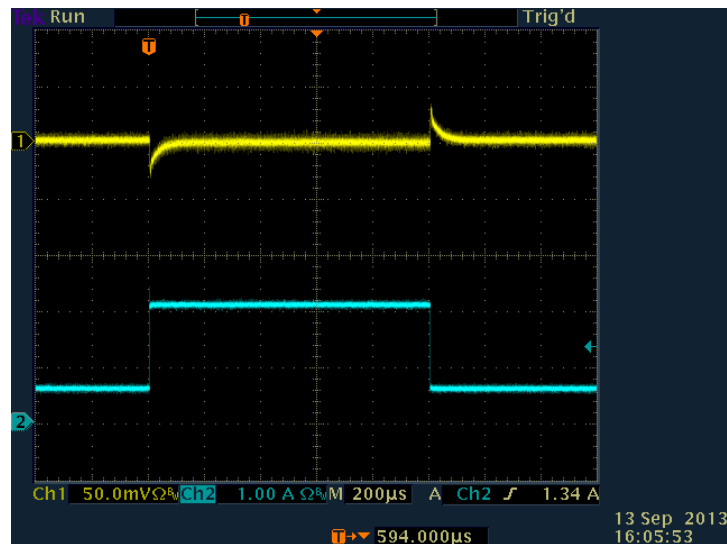


Figure 4. TPS54388EVM Load Transient

2.6 Loop Response

Figure 5 shows the TPS54388EVM loop-response characteristics. Gain and phase plots are shown for a V_{IN} voltage of 5 V and a load current of 2.25 A.

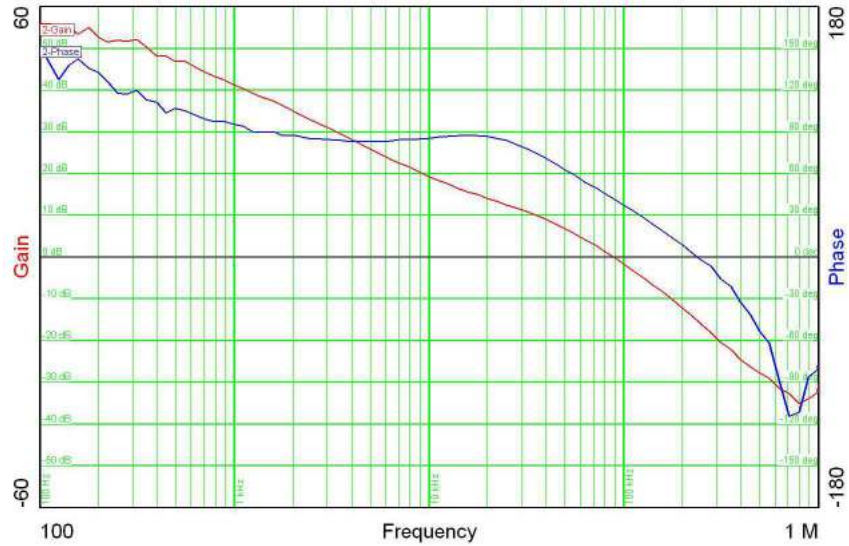


Figure 5. TPS54388EVM Loop-Response Measurement

2.7 Output-Voltage Ripple

Figure 6 shows the TPS54388EVM output-voltage ripple. The output current is the rated full-load current of 3 A and $V_{IN} = 5$ V. The ripple voltage is measured directly across the output capacitors.

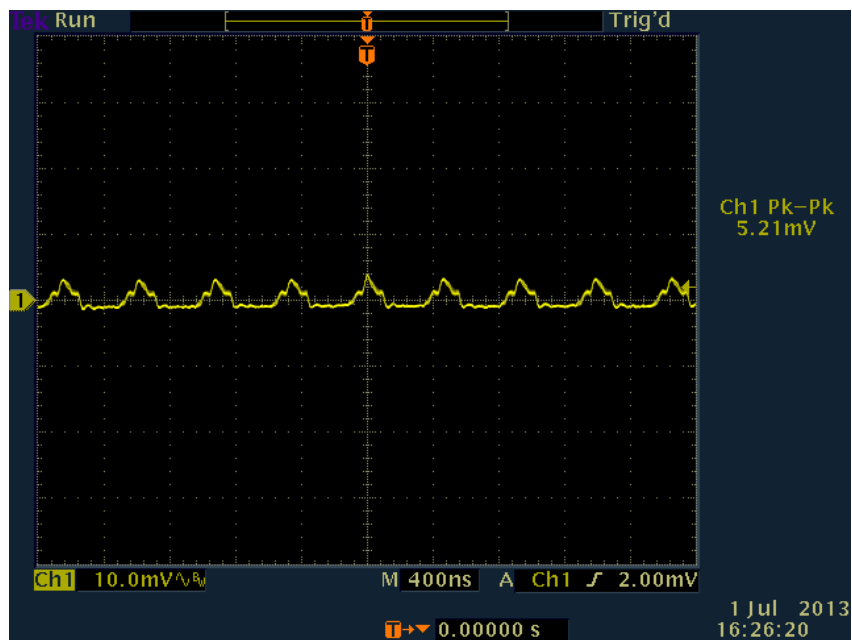


Figure 6. TPS54388EVM Output Ripple

2.8 Power Up

Figure 7 and Figure 8 show the start-up waveforms for the TPS54388EVM. In Figure 8, the output voltage ramps up as soon as the input voltage reaches the UVLO threshold as set by the R_3 and R_4 resistor divider network. In Figure 9, the input voltage is applied initially and the output is inhibited by using a jumper at JP1 to tie EN to GND. When the jumper is removed, EN is released. When the EN voltage reaches the enable-threshold voltage, the start-up sequence begins, and the output voltage ramps up to the externally set value of 1.2 V. The input voltage for these plots is 5 V and the load is 1 Ω .

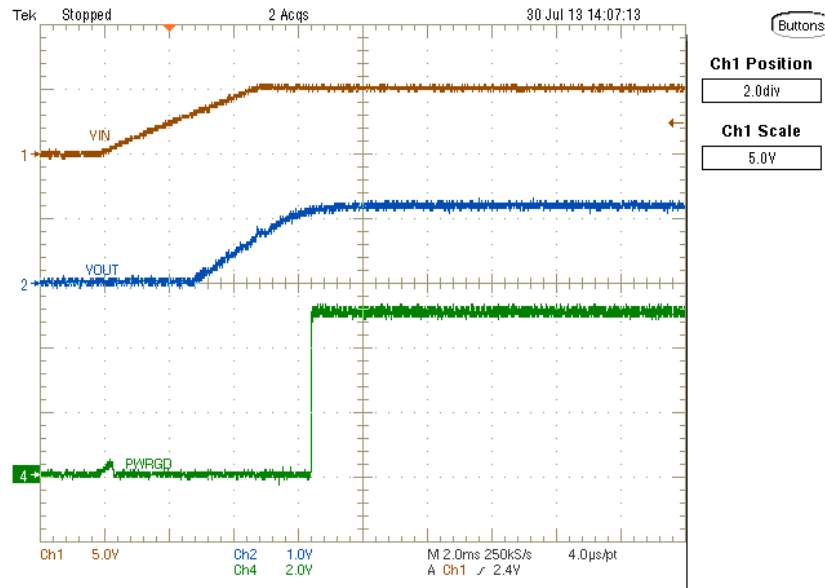


Figure 7. TPS54388EVM Startup Relative to V_{IN}

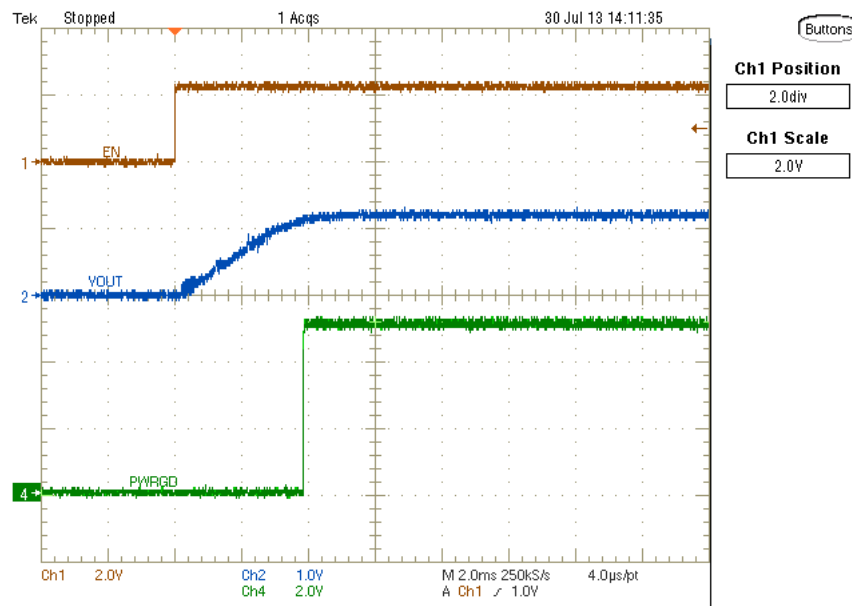


Figure 8. TPS54388EVM Startup Relative to Enable

3 Board Layout

This section provides a description of TPS54388EVM board layout and layer illustrations.

3.1 Layout

Figure 9, Figure 10, Figure 11, and Figure 12 show the board layout of the TPS54388EVM.

The top-side layer of the EVM contains the main traces for V_{IN} , V_{OUT} , and V_{PH} . Also on the top-side layer are connections for the remaining pins of the TPS54388-Q1 device and a large area filled with ground. The bottom-side layer contains some components and another large area filled with ground. The top-side ground areas are connected to the bottom ground plane with multiple vias placed around the board including four vias directly under the TPS54388-Q1 device to provide a thermal path from the top-side ground area to the bottom-side ground plane.

The input decoupling capacitors (C2, C3, C4, and C5) and bootstrap capacitor (C11) are all located as close to the IC as possible. In addition, the voltage set-point resistor divider components are also located close to the IC on the bottom of the board. For the TPS54388-Q1 device, an additional input bulk-capacitor can be required depending on the EVM connection to the input supply.

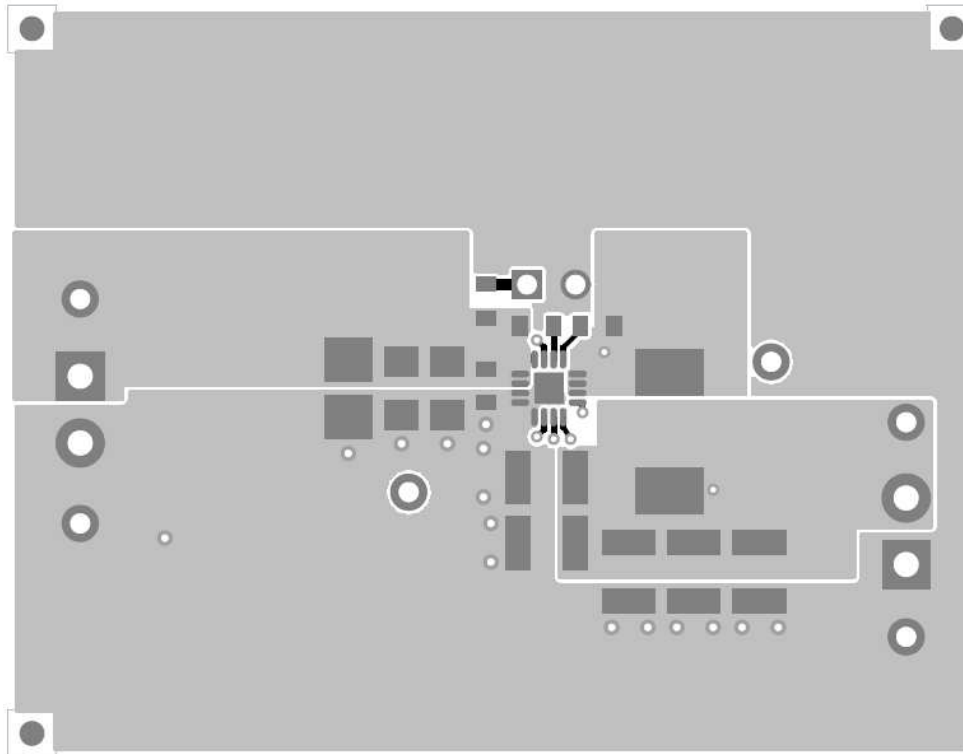


Figure 9. TPS54388EVM Top-Side Layout

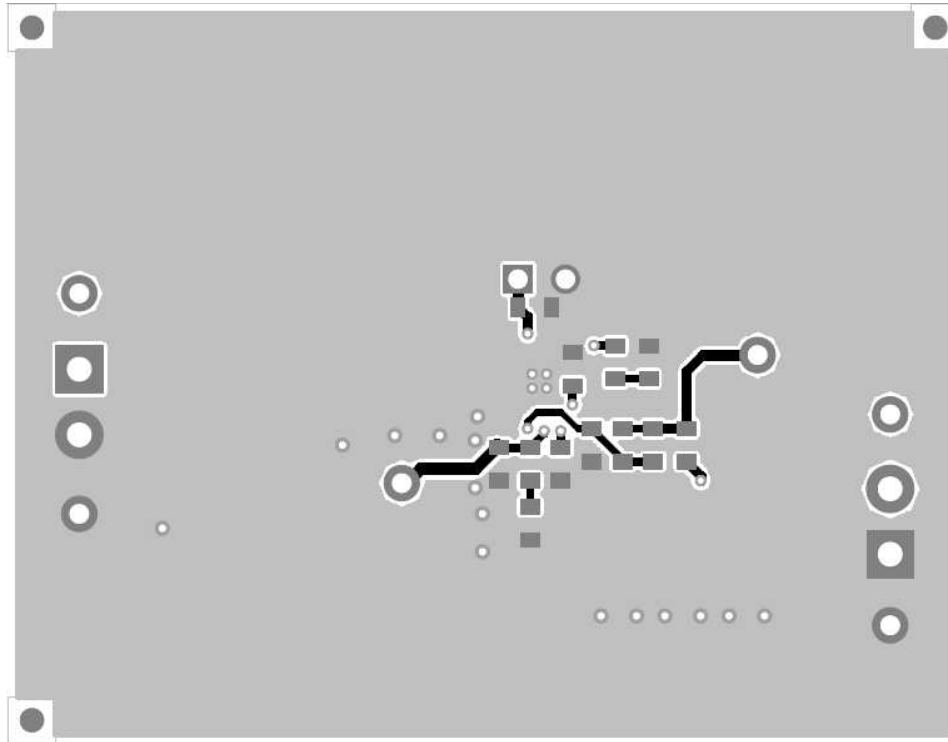


Figure 10. TPS54388EVM Bottom-Side Layout

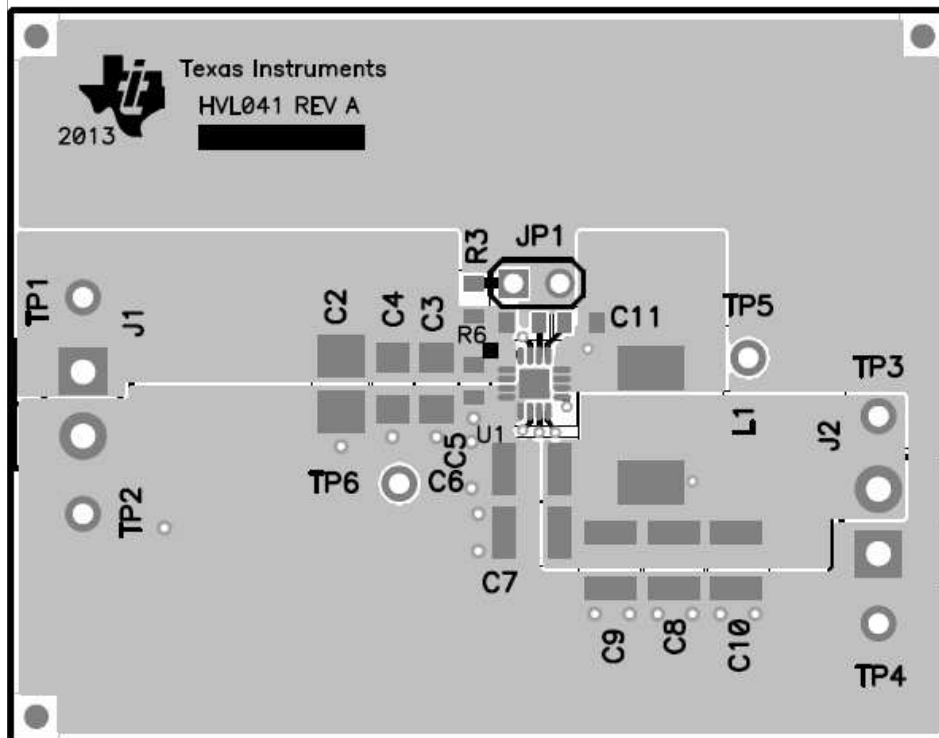


Figure 11. TPS54388EVM Top-Side Assembly

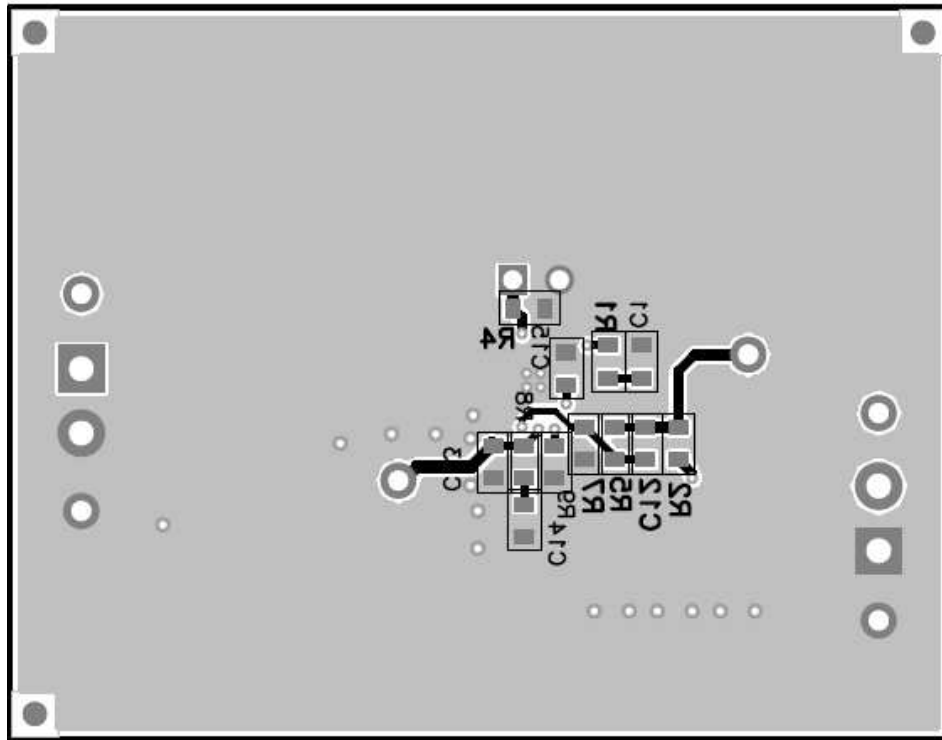


Figure 12. TPS54388EVM Bottom-Side Assembly

4 Schematic and Bill of Materials

4.1 Schematic

Figure 13 is the schematic of the TPS54388EVM.

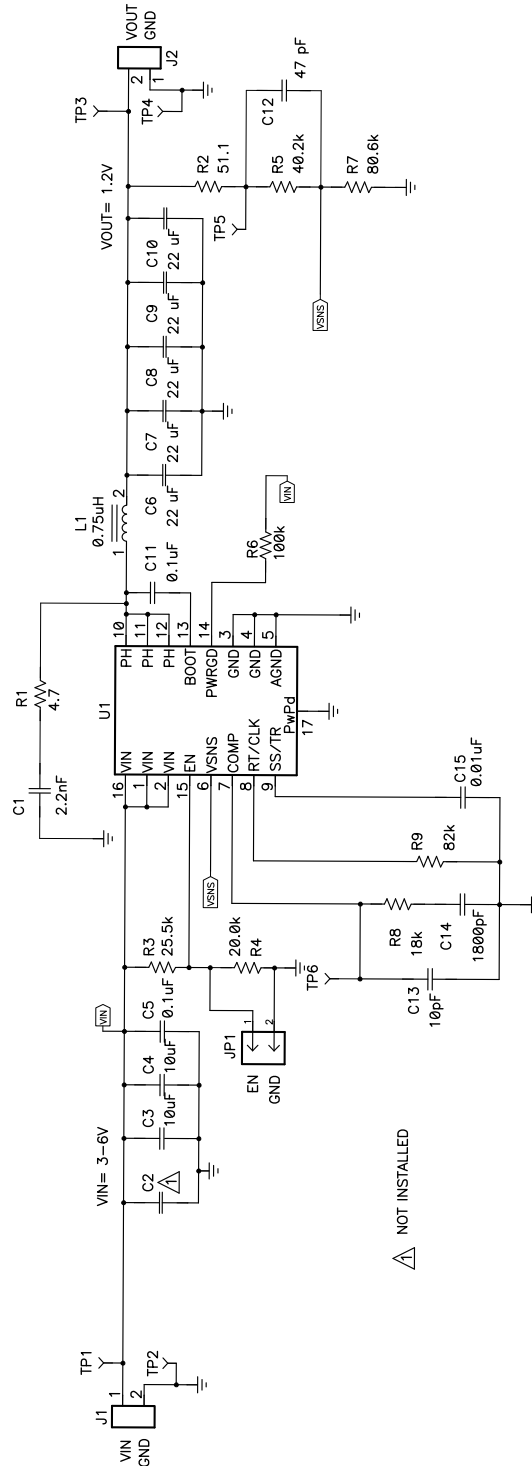


Figure 13. TPS54388EVM Schematic

4.2 Bill of Materials

Table 5 lists the bill of materials for the TPS54388EVM.

Table 5. TPS54388EVM Bill of Materials

Count	RefDes	Value	Description	Size	Part Number	MFR
1	C1	2.2 nF	Capacitor, Ceramic, 16 V, X7R, 10%	603	GRM188R71C222KA01D-ND	Murata
0	C2	Open	Capacitor, Ceramic	Multi sizes	Engineering Only	Standard
2	C3, C4	10 μ F	Capacitor, Ceramic, 10 V, X5R, 20%	1206	C3216X5R1A106M160AB	TDK
2	C5, C11	0.1 μ F	Capacitor, Ceramic, 25 V, X5R, 10%	603	C1608X5R1H104K080AA	TDK
5	C6, C7, C8, C9, C10	22 μ F	Capacitor, Ceramic, 10 V, X5R, 20%	1210	C3225X5R1A226M230AA	TDK
0	C12	47 pF	Capacitor, Ceramic, 50 V, C0G, 5%	603	C1608C0G1H470J080AA	TDK
1	C13	10 pF	Capacitor, Ceramic, 50 V, C0G	603	C1608C0G1H100D080AA	TDK
1	C14	1800 pF	Capacitor, Ceramic, 50 V, X7R, 10%	603	GRM188R71H182KA01D	Murata
1	C15	0.01 μ F	Capacitor, Ceramic, 16 V, X7R, 15%	603	GRM188R71C103KA01D	Murata
2	J1, J2	ED555/2DS	Terminal Block, 2-pin, 6-A, 3.5 mm	0.27 \times 0.25 inch	ED555/2DS	OST
1	JP1	PEC02SAAN	Header, Male 2-pin, 100-mil spacing	0.100 inch \times 2	PEC36SAAN	Sullins
1	L1	0.75 μ H	Inductor, SMT, 10 A, 7.5 m Ω	0.255 \times 0.270 inch	FDV0630-R75M	TOKO
1	R1	4.7	Resistor, Chip, 1/16 W, 1%	603	CRCW06034R70FNEA	Vishay
1	R2	51.1	Resistor, Chip, 1/16 W, 1%	603	3-1879335-7	TE
1	R3	25.5k	Resistor, Chip, 1/16 W, 1%	603	9-1879337-8	TE
1	R4	20.0k	Resistor, Chip, 1/16 W, 1%	603	8-1879337-8	TE
1	R5	40.2k	Resistor, Chip, 1/16 W, 1%	603	1-1879338-8	TE
1	R6	100k	Resistor, Chip, 1/16 W, 1%	603	5-1879338-6	TE
1	R7	80.6k	Resistor, Chip, 1/16 W, 1%	603	4-1879338-7	TE
1	R8	18.0k	Resistor, Chip, 1/16 W, 1%	603	8-1879337-4	TE
1	R9	82k	Resistor, Chip, 1/16 W, 1%	603	1623002-2	TE
4	TP1, TP2, TP5, TP6	5000	Test Point, Red, Thru Hole Color Keyed	0.100 \times 0.100 inch	5000	Keystone
2	TP3, TP4	5001	Test Point, Black, Thru Hole Color Keyed	0.100 \times 0.100 inch	5001	Keystone
1	—	—	Shunt, 100-mil, Black	0.1	929950-00	3M
1	U1	TPS54388-Q1	IC, DC-DC Converter, 2.95 V to 6 V, 3 A	QFN-16	TPS54388QRTERQ1	TI
1	—	—	PCB, 2 inch \times 1.5 inch \times 0.062 inch	—	HVL041-003	Any

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products

Audio	www.ti.com/audio
Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
OMAP Applications Processors	www.ti.com/omap
Wireless Connectivity	www.ti.com/wirelessconnectivity

Applications

Automotive and Transportation	www.ti.com/automotive
Communications and Telecom	www.ti.com/communications
Computers and Peripherals	www.ti.com/computers
Consumer Electronics	www.ti.com/consumer-apps
Energy and Lighting	www.ti.com/energy
Industrial	www.ti.com/industrial
Medical	www.ti.com/medical
Security	www.ti.com/security
Space, Avionics and Defense	www.ti.com/space-avionics-defense
Video and Imaging	www.ti.com/video

TI E2E Community

e2e.ti.com