



N-CHANNEL ENHANCEMENT MODE MOSFET

Product Summary

BVDSS	Rds(on)	I _D T _A = +25°C
	0.6Ω @ V _{GS} = 4.5V	1.1A
20V	0.8Ω @ VGS = 2.5V	0.96A
	1.0Ω @ VGS = 1.8V	0.86A
	1.6Ω @ V _{GS} = 1.5V	0.68A

Features and Benefits

- Low On-Resistance
- Very low Gate Threshold Voltage, 1.0V Max.
- Low Input Capacitance
- Fast Switching Speed
- ESD Protected Gate
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- The DMN2451UFDQ is suitable for automotive applications requiring specific change control; this part is AEC-Q101 qualified, PPAP capable, and manufactured in IATF 16949 certified facilities.

https://www.diodes.com/quality/product-definitions/

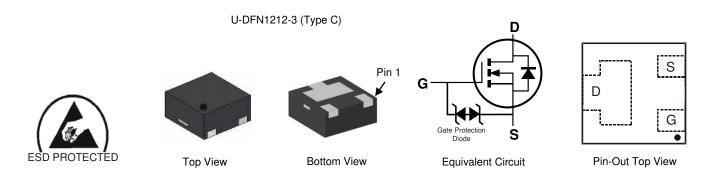
Description and Applications

This MOSFET is designed to minimize the on-state resistance $(R_{DS(ON)})$ yet maintain superior switching performance, making it ideal for high-efficiency power management applications.

- Power Management Functions
- Battery Operated Systems and Solid-State Relays
- Load Switch

Mechanical Data

- Case: U-DFN1212-3
- Case Material: Molded Plastic;
 UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish NiPdAu over Copper Leadframe; Solderable per MIL-STD-202, Method 208 @4
- Terminal Connections: See Diagram
- Weight: 0.005 grams (Approximate)



Ordering Information (Note 4)

Part Number	Case	Packaging
DMN2451UFDQ-7	U-DFN1212-3 (Type C)	3,000/Tape & Reel
DMN2451UFDQ-13	U-DFN1212-3 (Type C)	10,000/Tape & Reel

Notes:

- 1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
- 2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
- 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
- 4. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/.



Marking Information

U-DFN1212-3 (Type C)



CN2= Product Type Marking Code YWX = Date Code Marking Y = Year (ex: 1 = 2021)

W = Week (ex: a = Week 27; z Represents Week 52 and 53)

X = Internal Code (ex: U = Monday)

Date Code Key

Г	Vaar	0010		0001	0000	0000	0004	0005	0000	0007	0000	0000	0000
L	Year	2018	•••	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030
	Code	8		1	2	3	4	5	6	7	8	9	0

Week	1-26	27-52	53
Code	A-Z	a-z	Z

Internal Code	Sun	Mon	Tue	Wed	Thu	Fri	Sat
Code	Т	U	V	W	Χ	Υ	Z

Maximum Ratings (@TA = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit		
Drain-Source Voltage	V_{DSS}	20	V		
Gate-Source Voltage	Vgss	±12	V		
Continuous Drain Current (Note 6) V _{GS} = 4.5V	Steady State	T _A = +25°C T _A = +70°C	I _D	1.1 0.9	Α
Continuous Drain Current (Note 6) V _{GS} = 2.5V	lo	0.96 0.77	Α		
Pulsed Drain Current (10µs Pulse, Duty Cycle = 1%)	I _{DM}	3	Α		
Maximum Body Diode Forward Current (Note 6)			ls	1.2	Α

Thermal Characteristics (@TA = +25°C, unless otherwise specified.)

Characteristic		Symbol	Value	Unit
Total Power Dissipation (Note 5)		P _D	0.5	W
Thermal Resistance, Junction to Ambient (Note 5)	Steady State	RθJA	253	°C/W
Total Power Dissipation (Note 6)		PD	1.1	W
Thermal Resistance, Junction to Ambient (Note 6)	Steady State	Reja	111	°C/W
Thermal Resistance, Junction to Case (Note 6)		R ₀ JC	29	°C/W
Operating and Storage Temperature Range		TJ, TSTG	-55 to +150	°C

Notes:

^{5.} Device mounted on FR-4 PC board, with minimum recommended pad layout, single sided.6. Device mounted on FR-4 substrate PC board, 2oz copper, with thermal vias to bottom layer 1-inch square copper plate.



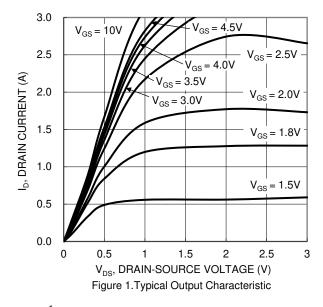
Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Тур	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 7)						
Drain-Source Breakdown Voltage	BV _{DSS}	20	_	_	V	$V_{GS} = 0V, I_D = 250\mu A$
Zero Gate Voltage Drain Current T _J = +25°C	IDSS	_	_	100	nA	$V_{DS} = 20V$, $V_{GS} = 0V$
Gate-Source Leakage	I _{GSS}		_	±1.0	μΑ	$V_{GS} = \pm 4.5V, V_{DS} = 0V$
ON CHARACTERISTICS (Note 7)						
Gate Threshold Voltage	V _{GS(TH)}	0.45		1.0	V	$V_{DS} = V_{GS}$, $I_D = 250\mu A$
		_	0.2	0.6		$V_{GS} = 4.5V, I_D = 200mA$
Static Drain-Source On-Resistance	D	_	0.3	0.8		$V_{GS} = 2.5V, I_D = 200mA$
Static Drain-Source On-Resistance	RDS(ON)	_	0.5	1.0	Ω	$V_{GS} = 1.8V, I_D = 100mA$
		_	0.9	1.6		V _{GS} = 1.5V, I _D = 50mA
Diode Forward Voltage	VsD	_	0.7	1.2	V	$V_{GS} = 0V, I_{S} = 500mA$
DYNAMIC CHARACTERISTICS (Note 8)						
Input Capacitance	Ciss	_	52	_	pF	V 40V V 0V
Output Capacitance	Coss		4.8	_	pF	V _{DS} =16V, V _{GS} = 0V, f = 1.0MHz
Reverse Transfer Capacitance	Crss		3.1	_	pF	1 = 1.0WHZ
Gate Resistance	Rg	_	95	_	Ω	$V_{DS} = 0V, V_{GS} = 0V, f = 1.0MHz$
Total Gate Charge	Qg	_	0.7	_	nC	45777
Gate-Source Charge	Qgs	_	0.09	_	nC	$V_{GS} = 4.5V, V_{DS} = 10V,$ $I_{D} = 250mA$
Gate-Drain Charge	Q _{gd}	_	0.05	_	nC	ID = 250IIIA
Turn-On Delay Time			3.7	_	ns	
Turn-On Rise Time		_	2.4	_	ns	$V_{DD} = 10V, V_{GS} = 4.5V,$
Turn-Off Delay Time	tD(OFF)		20.9	_	ns	$R_L = 47\Omega$, $R_G = 10\Omega$,
Turn-Off Fall Time	tF	_	5.6	_	ns	$I_D = 200 \text{mA}$

Notes:

^{7.} Short duration pulse test used to minimize self-heating effect. 8. Guaranteed by design. Not subject to production testing.





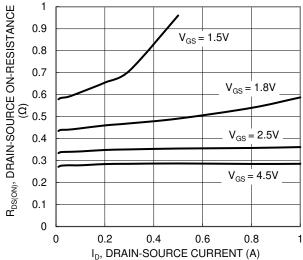


Figure 3. Typical On-Resistance vs. Drain Current and Gate Voltage

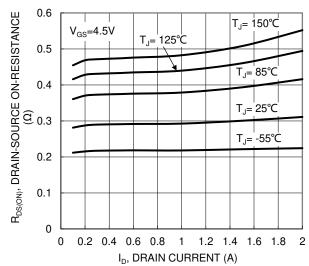
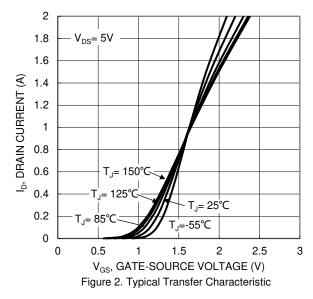
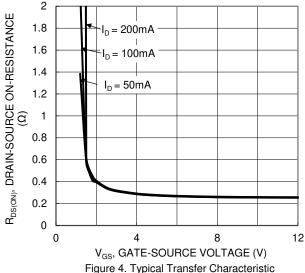


Figure 5. Typical On-Resistance vs. Drain Current and Temperature





2 R_{DS(ON)}, DRAIN-SOURCE ON-RESISTANCE (NORMALIZED) 1.8 $V_{GS} = 4.5V, I_D = 200mA$ 1.6 $V_{GS} = 2.5V, I_D = 200 mA$ 1.4 1.2 1 $V_{GS} = 1.8V, I_{D} = 100mA$ 0.8 $V_{GS} = 1.5V, I_D = 50mA$ 0.6 0.4 -50 -25 25 50 75 100 125 150 T_J, JUNCTION TEMPERATURE (°C)

Figure 6. On-Resistance Variation with Temperature





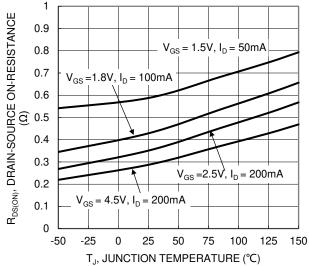


Figure 7. On-Resistance Variation with Temperature

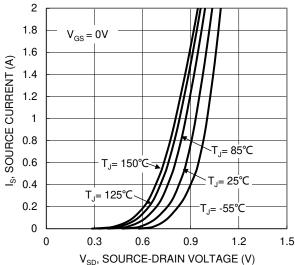
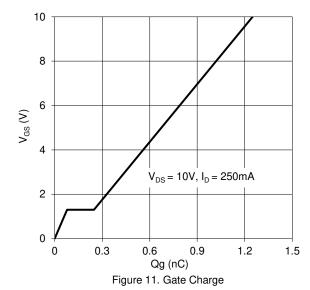
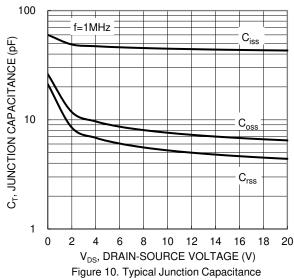


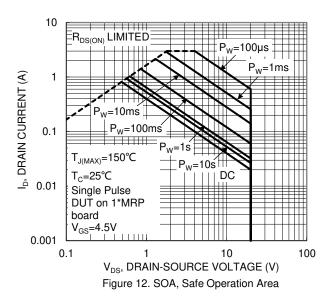
Figure 9. Diode Forward Voltage vs. Current



1.2 $V_{GS(TH)}$, GATE THRESHOLD VOLTAGE (V) 1 $I_D = 1 \text{mA}$ 8.0 0.6 $I_{D} = 250 \mu A$ 0.4 0.2 0 -25 0 25 50 75 100 125 -50 150 T_J, JUNCTION TEMPERATURE (°C)

Figure 8. Gate Threshold Variation vs. JunctionTemperature







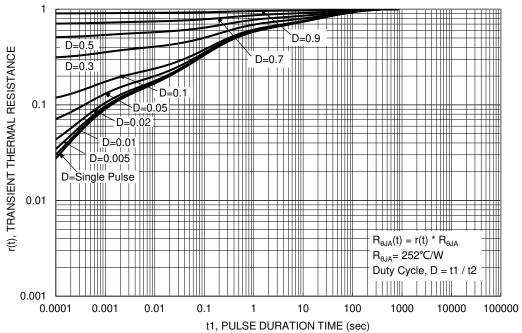


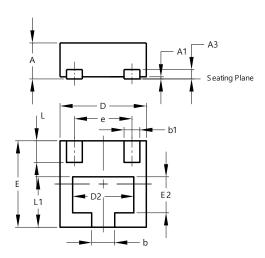
Figure 13. Transient Thermal Resistance



Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

U-DFN1212-3 (Type C)

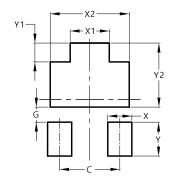


U-DFN1212-3 Type C							
Dim	Min	Max	Тур				
Α	0.47	0.53	0.50				
A1	0	0.05	0.02				
A3	-	-	0.13				
b	0.27	0.37	0.32				
b1	b1 0.17		0.22				
D	1.15	1.25	1.20				
D2	D2 0.75		0.85				
е	-	-	0.80				
E	1.15	1.25	1.20				
E2	0.40	0.60	0.50				
L	0.25	0.35	0.30				
L1	0.65	0.75	0.70				
All	Dimens	sions in	mm				

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

U-DFN1212-3 (Type C)



Dimensions	value				
Dillielisions	(in mm)				
С	0.800				
G	0.200				
X	0.320				
X1	0.520				
X2	1.050				
Υ	0.450				
Y1	0.250				
Y2	0.850				

Value



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