

SN54LS682, SN54LS684, SN54LS685, SN54LS687, SN54LS688, SN74LS682, SN74LS684 THRU SN74LS688 8-BIT MAGNITUDE/IDENTITY COMPARATORS

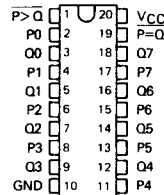
D2617, JANUARY 1981 - REVISED MARCH 1988

- Compares Two-8-Bit Words
- Choice of Totem-Pole or Open-Collector Outputs
- Hysteresis at P and Q Inputs
- 'LS682 has 20-k Ω Pullup Resistors on the Q Inputs
- SN74LS686 and 'LS687 . . . JT and NT 24-Pin, 300-Mil Packages

TYPE	P = Q	P > Q	OUTPUT ENABLE	OUTPUT CONFIGURATION	20-k Ω PULLUP
'LS682	yes	yes	no	totem-pole	yes
'LS684	yes	yes	no	totem-pole	no
'LS685	yes	yes	no	open-collector	no
SN74LS686	yes	yes	yes	totem-pole	no
'LS687	yes	yes	yes	open-collector	no
'LS688	yes	no	yes	totem-pole	no

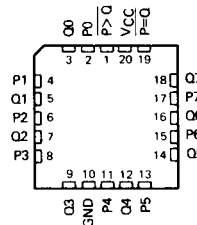
SN54LS682, SN54LS684, SN54LS685 . . . J PACKAGE
SN74LS682, SN74LS684, SN74LS685 . . . DW OR N PACKAGE

(TOP VIEW)



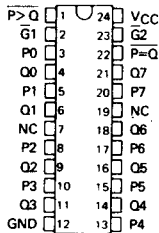
SN54LS682, SN54LS684, SN54LS685 . . . FK PACKAGE

(TOP VIEW)



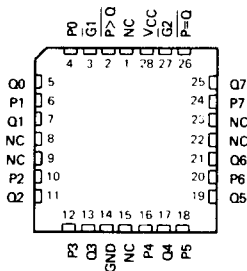
SN54LS687 . . . JT PACKAGE
SN74LS686, SN74LS687 . . . DW OR NT PACKAGE

(TOP VIEW)



SN54LS687 . . . FK PACKAGE

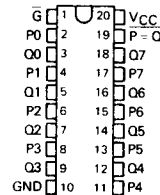
(TOP VIEW)



NC—No internal connection

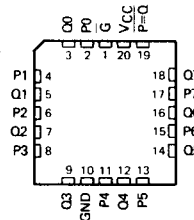
SN54LS688 . . . J PACKAGE
SN74LS688 . . . DW OR N PACKAGE

(TOP VIEW)



SN54LS688 . . . FK PACKAGE

(TOP VIEW)



2

TTL Devices

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

TEXAS INSTRUMENTS

POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

2-1129

SN54LS682, SN54LS684, SN54LS685, SN54LS687, SN54LS688 SN74LS682, SN74LS684 THRU SN74LS688 8-BIT MAGNITUDE/IDENTITY COMPARATORS

description

These magnitude comparators perform comparisons of two eight-bit binary or BCD words. All types provide $\overline{P=Q}$ outputs and all except 'LS688 provide $\overline{P>Q}$ outputs as well. The 'LS682, 'LS684, 'LS686, and 'LS688 have totem-pole outputs, while the 'LS685 and 'LS687 have open-collector outputs. The 'LS682 features 20-k Ω pullup termination resistors on the Q inputs for analog or switch data.

FUNCTION TABLE

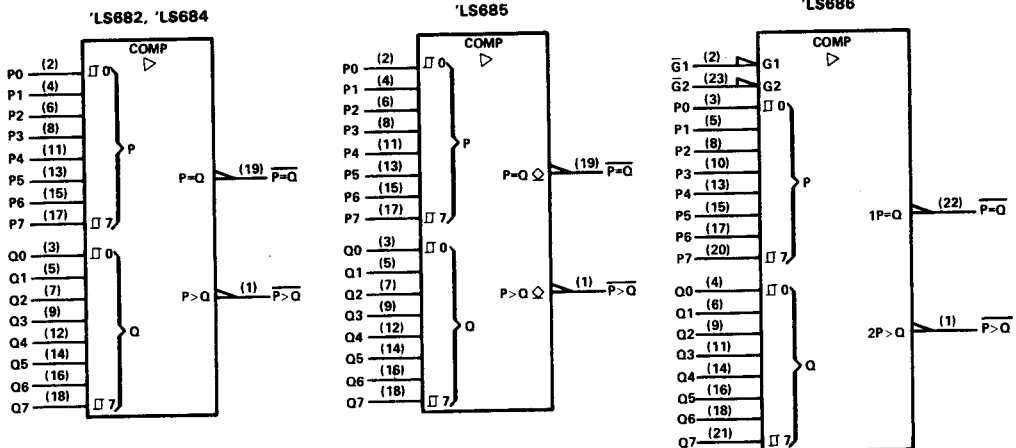
INPUTS			OUTPUTS	
DATA P, Q	ENABLES		$\overline{P=Q}$	$\overline{P>Q}$
	$\overline{G_1}$, $\overline{G_2}$	$\overline{G_2}$		
$P=Q$	L	X	L	H
$P>Q$	X	L	H	L
$P<Q$	X	X	H	H
$P=Q$	H	X	H	H
$P>Q$	X	H	H	H
X	H	H	H	H

- NOTES: 1. The last three lines of the function table applies only to the devices having enable inputs, i.e., 'LS686 thru 'LS688.
2. The $\overline{P<Q}$ function can be generated by applying the $\overline{P=Q}$ and $\overline{P>Q}$ outputs to a 2-input NAND gate.
3. For 'LS686 and 'LS687, $\overline{G_1}$ enables $\overline{P=Q}$ and $\overline{G_2}$ enables $\overline{P>Q}$.

2

logic symbols†

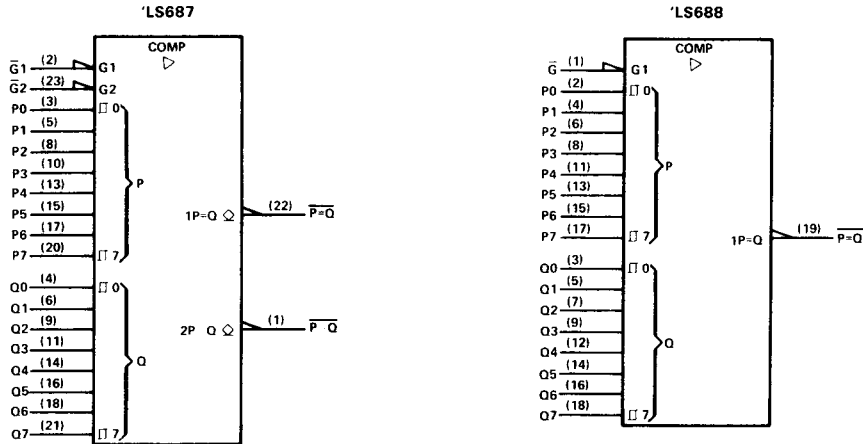
TTL Devices



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for DW, J, JT, N, and NT packages.

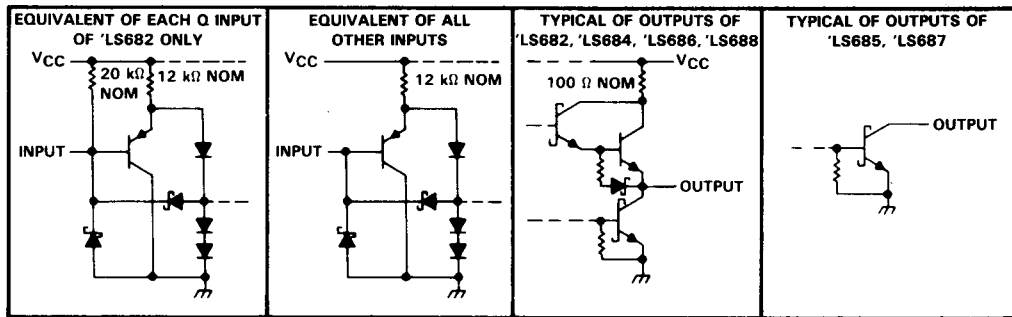
**SN54LS682, SN54LS684, SN54LS685, SN54LS687, SN54LS688,
SN74LS682, SN74LS684 THRU SN74LS688
8-BIT MAGNITUDE/IDENTITY COMPARATORS**

logic symbols† (continued)



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for DW, J, JT, N, and NT packages.

schematics of inputs and outputs



2

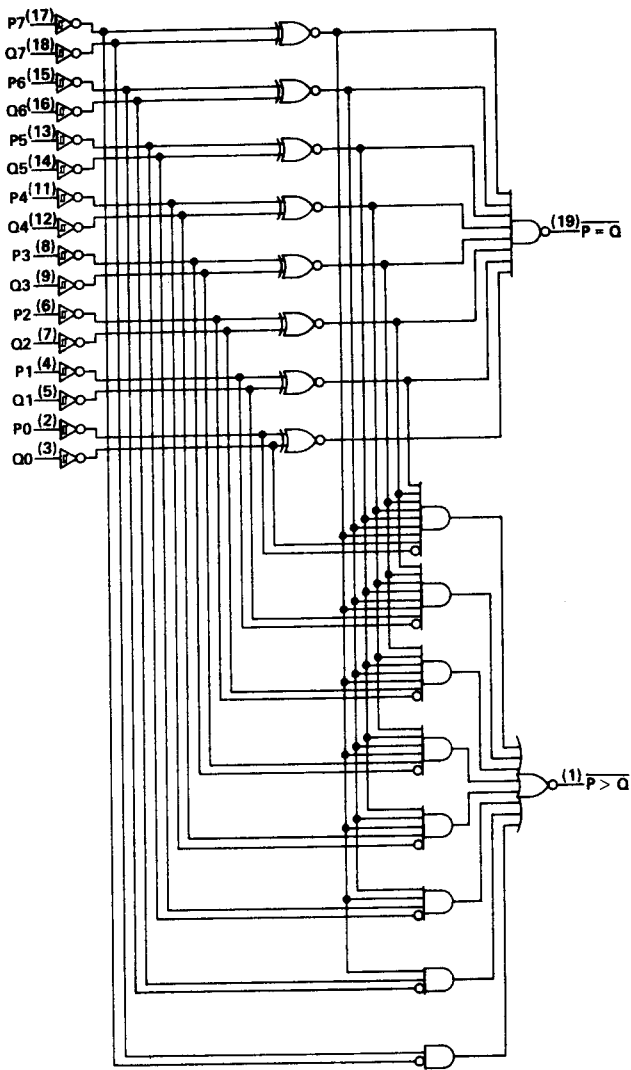
TTL Devices

**SN54LS682, SN54LS684, SN54LS685
SN74LS682, SN74LS684, SN74LS685
8-BIT MAGNITUDE/IDENTITY COMPARATORS**

1S682, 1S684, 1S685 logic diagram (positive logic)

2

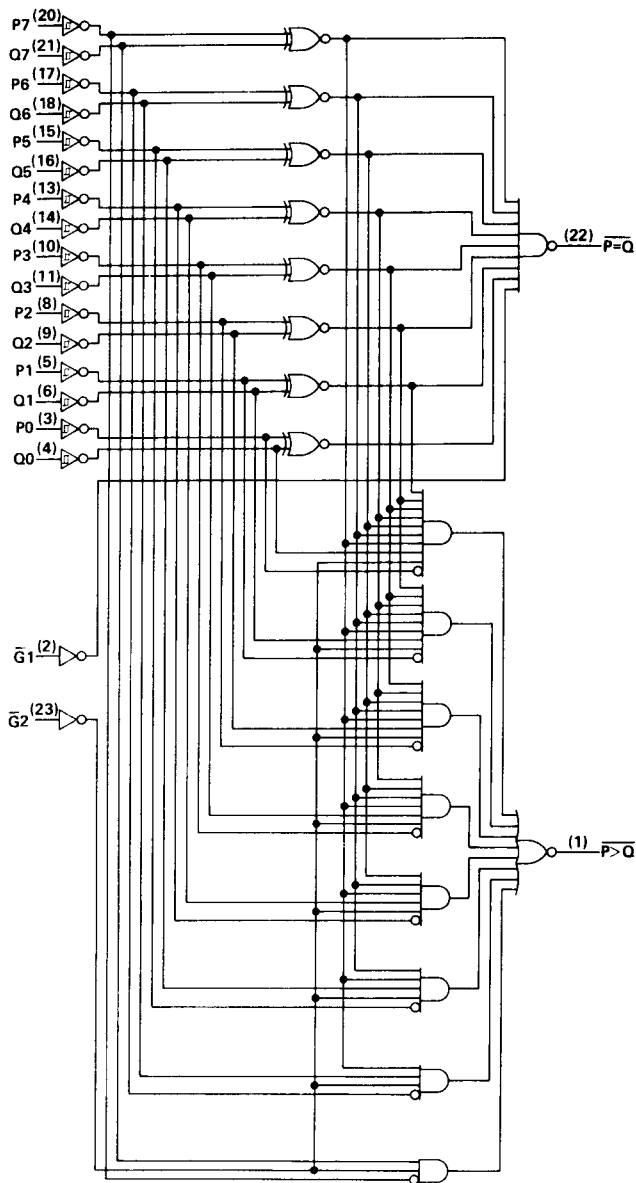
TTL Devices



Pin numbers shown are for DW, J, and N packages.

**SN54LS687
SN74LS686, SN74LS687
8-BIT MAGNITUDE/IDENTITY COMPARATORS**

'LS686, 'LS687 logic diagram (positive logic)



Pin numbers shown are for DW, JT, and NT packages.

2
TTL Devices

Application Information (continued)

T-51-09-08

If sub-pixel synchronization of multiple Bt460s is not

When using multiple Bt460s, each Bt460 should have

SN54LS682, SN54LS684, SN54LS688
SN74LS682, SN74LS684, SN74LS686, SN74LS688
8-BIT MAGNITUDE/IDENTITY COMPARATORS WITH TOTEM-POLE OUTPUTS

recommended operating conditions

	SN54LS*			SN74LS*			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.85	5	5.25	V
High-level output current, I_{OH}			-400			-400	μ A
Low-level output current, I_{OL}			12			24	mA
Operating free-air temperature, T_A	-55		125	0		70	$^{\circ}$ C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54LS*		SN74LS*		UNIT
			MIN	TYP‡	MAX	MIN	
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage		0.7		0.8		V
$V_{T+} - V_{T-}$	Hysteresis	P or Q inputs	0.4		0.4		V
V_{IK}	Input clamp voltage	$V_{CC} = \text{MIN}$	-1.5		-1.5		V
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = V_{IL\text{max}}$, $I_{OH} = -400 \mu\text{A}$	2.5		2.7		V
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = V_{IL\text{max}}$	$I_{OL} = 12 \text{ mA}$ 0.25 0.4		$I_{OL} = 12 \text{ mA}$ 0.25 0.4		V
I_I	Input current at maximum input voltage	Q inputs, 'LS682	$V_{CC} = \text{MAX}$, $V_I = 5.5 \text{ V}$				mA
		All other inputs	$V_{CC} = \text{MAX}$, $V_I = 7 \text{ V}$		0.1		
I_{IH}	High-level input current	$V_{CC} = \text{MAX}$, $V_I = 2.7 \text{ V}$	20		20		μ A
I_{IL}	Low-level input current	Q inputs, 'LS682	$V_{CC} = \text{MAX}$, $V_I = 0.4 \text{ V}$		-0.4		mA
		All other inputs			-0.2		
I_{OS}^{\S}	Short-circuit output current	$V_{CC} = \text{MAX}$, $V_O = 0$	-20 -100		-20 -100		mA
I_{CC}	Supply current	$V_{CC} = \text{MAX}$, See Note 1	'LS682		42 70		mA
			'LS684		40 65		
			'LS686		44 75		
			'LS688		40 65		

† For conditions shown as MIN or MAX, use the appropriate values specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

NOTE 1: I_{CC} is measured with any \bar{G} inputs grounded, all other inputs at 4.5 V, and all outputs open.

2

TTL Devices

SN54LS682, SN54LS684, SN54LS688
SN74LS682, SN74LS684, SN74LS686, SN74LS688
8-BIT MAGNITUDE/IDENTITY COMPARATORS WITH TOTEM-POLE OUTPUTS

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER†	FROM (INPUTS)	TO (OUTPUT)	TEST CONDITIONS	'LS682			'LS684			'LS686			'LS688			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t _{PLH}	P	$\overline{P} = \overline{Q}$	R _L = 667 Ω, C _L = 45 pF, All other inputs low, See Note 2	13	25		15	25		13	25		12	18	ns	
t _{PHL}				15	25		17	25		20	30		17	23		
t _{PLH}	Q	$\overline{P} = \overline{Q}$		14	25		16	25		13	25		12	18	ns	
t _{PHL}				15	25		15	25		21	30		17	23		
t _{PLH}	\overline{Q} , $\overline{Q}1$	$\overline{P} = \overline{Q}$								11	20		12	18	ns	
t _{PHL}										19	30		13	20		
t _{PLH}	P	$\overline{P} > \overline{Q}$			20	30		22	30		19	30			ns	
t _{PHL}							15	30		17	30		15	30		
t _{PLH}	Q	$\overline{P} > \overline{Q}$			21	30		24	30		18	30			ns	
t _{PHL}							19	30		20	30		19	30		
t _{PLH}	$\overline{Q}2$	$\overline{P} > \overline{Q}$								21	30			ns		
t _{PHL}											16	25				

† t_{PLH} = propagation delay time, low-to-high-level outputs; t_{PHL} = propagation delay time, high-to-low-level output.
 NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

2

TTL Devices

**SN54LS685, SN54LS687
SN74LS685, SN74LS687, SN74LS688
8-BIT MAGNITUDE/IDENTITY COMPARATORS WITH TOTEM-POLE OUTPUTS**

recommended operating conditions

	SN54LS'			SN74LS'			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.85	5	5.25	V
High-level output current, V_{OH}	5.5			5.5			V
Low-level output current, I_{OL}	12			24			mA
Operating free-air temperature, T_A	-55			125			0 70 °C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54LS'			SN74LS'			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage		0.7			0.8			V
$V_{T+} - V_{T-}$	Hysteresis	P or Q inputs	0.4			0.4			V
V_{IK}	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$	-1.5			-1.5			V
I_{OH}	High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{ILmax}, V_{OH} = 5.5 \text{ V}$	250			100			μA
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{ILmax}, I_{OL} = 12 \text{ mA}$	0.25		0.4		0.25 0.4		V
		$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{ILmax}, I_{OL} = 24 \text{ mA}$					0.35 0.5		
I_I		$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$	0.1			0.1			mA
I_{IH}	High-level input current	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$	20			20			μA
I_{IL}	Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$	-0.2			-0.2			mA
I_{CC}	Supply current	'LS685	40 65		40 65		mA		
		'LS687	44 75		44 75				

†For conditions shown as MIN or MAX, use the appropriate values specified under recommended operating conditions.

‡All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

NOTE 1: I_{CC} is measure with any \bar{G} inputs grounded, all other inputs at 4.5 V, and all outputs open.

2

TTL Devices

SN54LS685, SN54LS687
SN74LS685, SN74LS687
8-BIT MAGNITUDE/IDENTITY COMPARATORS WITH OPEN-COLLECTOR OUTPUTS

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS685			'LS687			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	P	$\overline{P} = \overline{Q}$	$R_L = 667\ \Omega$, $C_L = 45\ \text{pF}$, All other inputs low, See Note 2	30	45		24	35	ns	
t_{PHL}				19	35		20	30		
t_{PLH}	Q	$\overline{P} = \overline{Q}$		24	45		24	35	ns	
t_{PHL}				23	35		20	30		
t_{PLH}	$\overline{Q}, \overline{Q}_1$	$\overline{P} = \overline{Q}$					21	35	ns	
t_{PHL}							18	30		
t_{PLH}	P	$\overline{P} > \overline{Q}$		32	45		24	35	ns	
t_{PHL}				16	35		16	30		
t_{PLH}	Q	$\overline{P} > \overline{Q}$		30	45		24	35	ns	
t_{PHL}				20	35		16	30		
t_{PLH}	\overline{Q}_2	$\overline{P} > \overline{Q}$					24	35	ns	
t_{PHL}							15	30		

t_{pLH} = propagation delay time, low-to-high-level outputs; t_{pHL} = propagation delay time, high-to-low-level output.
 NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

2

TTL Devices