12-Channel Gamma Buffers with VCOM Buffer

ADD8701

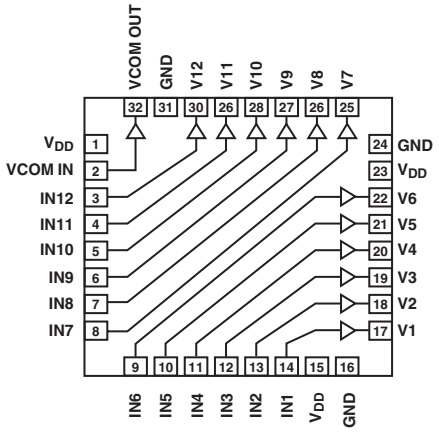
FEATURES

Single-Supply Operation: 7 V to 16 V
Dual-Supply Operation: ±3.5 V to ±8 V
Supply Current: 13 mA Max
Upper/Lower Buffers Swing to V_{DD}/GND
Continuous Output Current: 10 mA
VCOM Peak Output Current: 250 mA
Offset Voltage: 15 mV Max
Slew Rate: 6 V/μs
Fast Settling Time with Large C-Load

APPLICATIONS

TFT LCD Panels

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The ADD8701 is a low cost, 12-channel buffer amplifier and VCOM driver that operates from a single supply. The part is designed for high resolution TFT LCD panels, and is built on an advanced, high voltage, CBCMOS process.

The buffers have high slew rate, 10 mA continuous output current, and high capacitive load drive capability. The VCOM buffer has increased drive of 35 mA and can drive large capacitive loads. The ADD8701 offers wide supply range and offset voltages below 15 mV.

The ADD8701 is specified over the –40°C to +85°C temperature range and is available in a 32-lead lead frame chip scale package (LFCSP).

All inputs and outputs incorporate internal ESD protection circuits.

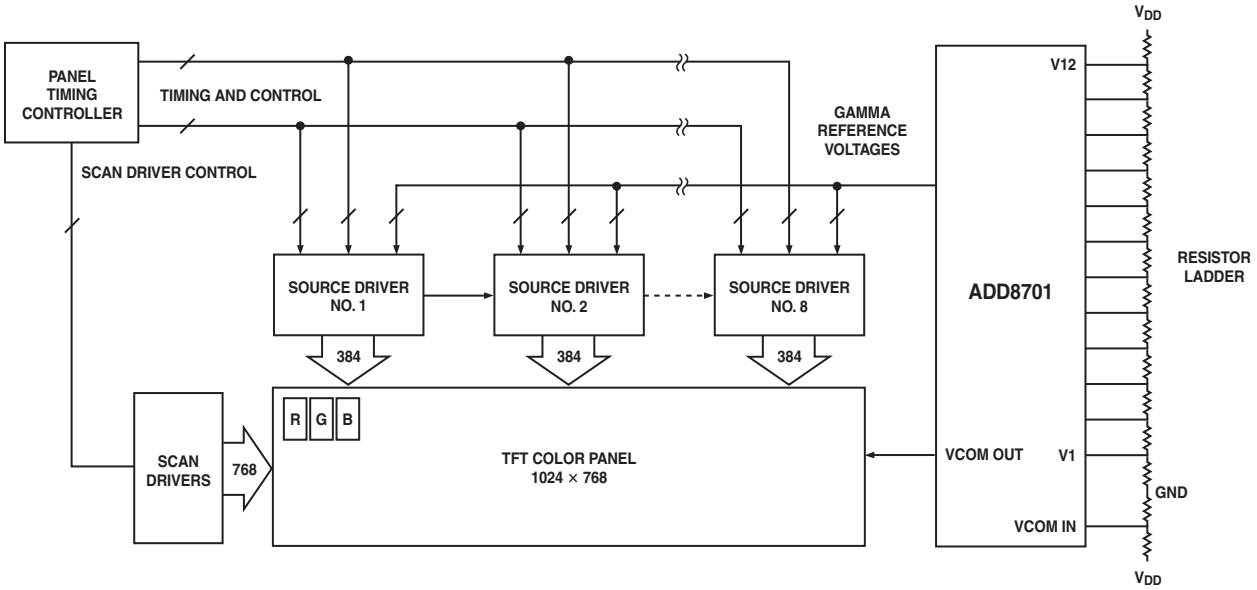


Figure 1. Typical SVGA TFT-LCD Application

REV. 0

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ADD8701–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS ($7\ V \le V_{DD} \le 16\ V$, $T_A = 25°C$, unless otherwise specified.)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			4	15	mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	$-40°C \le T_A \le +85°C$		5		µV/°C
Input Bias Current	I_B			0.5	1.1	µA
		$-40°C \le T_A \le +85°C$			1.5	µA
Input Voltage Range			–0.5		V_{DD} + 0.5	V
Input Impedance	Z_{IN}			400		kΩ
Input Capacitance	C_{IN}			1		pF
OUTPUT CHARACTERISTICS						
Output Voltage High (V11, V12)	V_{OUT}	$I_L = 100\ \mu A$		15.995		V
		$V_{DD} = 16\ V$, $I_L = 5\ mA$	15.85	15.9		V
		$-40°C \le T_A \le +85°C$	15.75			V
		$V_{DD} = 7\ V$, $I_L = 5\ mA$	6.75	6.85		V
		$-40°C \le T_A \le +85°C$	6.65			V
Output Swing (V3 to V10)	V_{OUT}	$I_L = 5\ mA$, $V_{DD} = 16\ V$		14.6		V
Output Swing (V3 to V10)	V_{OUT}	$I_L = 5\ mA$, $V_{DD} = 7\ V$		5.6		V
Output Voltage Low (V1, V2)	V_{OUT}	$I_L = 100\ \mu A$		5		mV
		$V_{DD} = 16\ V$, $I_L = 5\ mA$		85	150	mV
		$-40°C \le T_A \le +85°C$			250	mV
		$V_{DD} = 7\ V$, $I_L = 5\ mA$		140	300	mV
		$-40°C \le T_A \le +85°C$			400	mV
Continuous Output Current	I_{OUT}			10		mA
Peak Output Current	I_{PK}	$V_{DD} = 16\ V$		150		mA
VCOM CHARACTERISTICS						
Continuous Output Current	I_{OUT}			35		mA
Peak Output Current	I_{PK}	$V_{DD} = 16\ V$		250		mA
TRANSFER CHARACTERISTICS						
Gain	A_{VCL}	$R_L = 2\ k\Omega$	0.995	0.9985	1.005	V/V
		$-40°C \le T_A \le +85°C$	0.995	0.9980	1.005	V/V
Gain Linearity	NL	$R_L = 10\ k\Omega$				
		$V_O = 0.5$ to $(V_{DD} - 0.5\ V)$		0.01		%
SUPPLY CHARACTERISTICS						
Supply Voltage	V_{DD}		7		16	V
Power Supply Rejection Ratio	PSRR	$V_{DD} = 6\ V$ to $17\ V$				
		$-40°C \le T_A \le +85°C$	70	90		dB
Supply Current	I_{SYS}	No Load		10	13	mA
		$-40°C \le T_A \le +85°C$			15	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	$R_L = 10\ k\Omega$, $C_L = 200\ pF$	4	6		V/µs
Bandwidth	BW	–3 dB, $R_L = 10\ k\Omega$, $C_L = 200\ pF$		4.5		MHz
Settling Time to 0.1% (Buffers)	t_S	$1\ V$, $R_L = 10\ k\Omega$, $C_L = 200\ pF$		1.1		µs
Settling Time to 0.1% (VCOM)	t_S	$1\ V$, $R_L = 10\ k\Omega$, $C_L = 200\ pF$		0.7		µs
Phase Margin	fo	$R_L = 10\ k\Omega$, $C_L = 200\ pF$		55		Degrees
Channel Separation				75		dB
NOISE PERFORMANCE						
Voltage Noise Density	e_n	f = 1 kHz		26		$nV/\sqrt{Hz}$
	e_n	f = 10 kHz		25		$nV/\sqrt{Hz}$
Current Noise Density	i_n	f = 10 kHz		0.8		$pA/\sqrt{Hz}$

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage (V_{DD}) . . . . . 18 V
Input Voltage . . . . . –0.5 V to V_{DD} + 0.5 V
Storage Temperature Range . . . . . –65°C to +150°C
Operating Temperature Range . . . . . –40°C to +85°C
Junction Temperature Range . . . . . –65°C to +150°C
Lead Temperature Range (Soldering, 60 sec) . . . . . 300°C
ESD Tolerance (HBM) . . . . . ±1,000 V

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

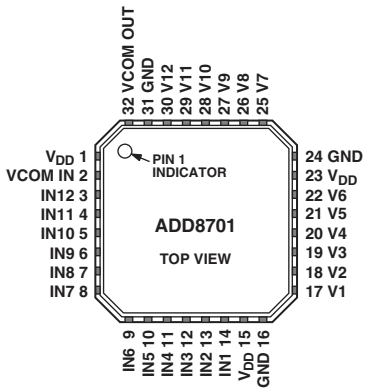
Package Type	θ_{JA}[1]	Ψ_{JB}[2]	Unit
32-Lead LFCSP (CP)	35	13	°C/W

NOTES
[1]θ_{JA} is specified for worst-case conditions, i.e., θ_{JA} is specified for device soldered in circuit board for surface-mount packages.
[2]ψ_{JB} is applied for calculating the junction temperature by reference to the board temperature.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADD8701ACP	–40°C to +85°C	32-Lead LFCSP	CP-32

PIN CONFIGURATION



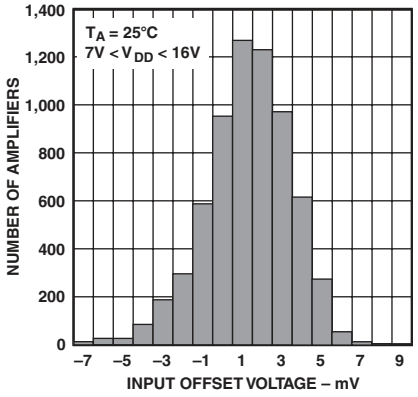
PIN FUNCTION DESCRIPTION

Pin No.	Mnemonic	Description
1, 15, 23	V_{DD}	Power (+)
2	VCOM IN	VCOM Buffer Input
3–14	IN12–IN1	Gamma Buffer Inputs
16, 24, 31	GND	Power (–)
17–22, 25–30	V1–V12	Gamma Buffer Outputs
32	VCOM OUT	VCOM Buffer Output

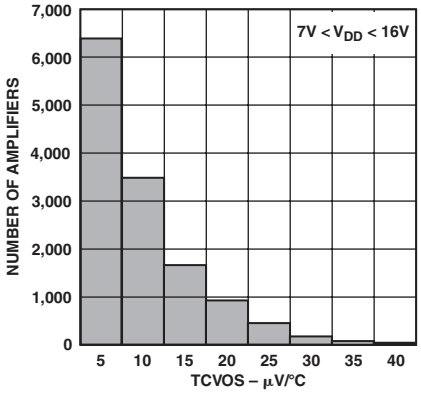
CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADD8701 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

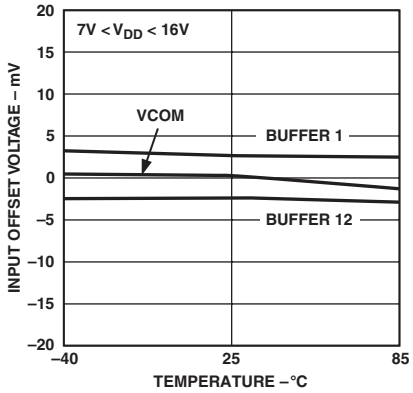
ADD8701–Typical Performance Characteristics



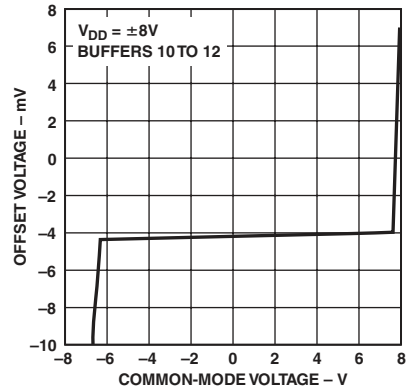
TPC 1. Input Offset Voltage Distribution



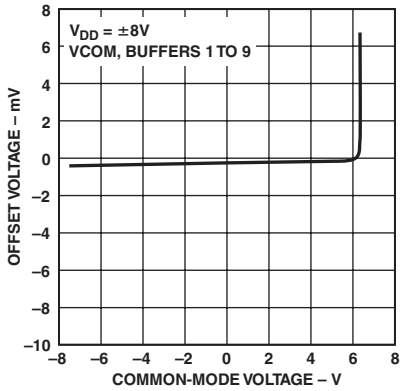
TPC 2. TCVOS Distribution



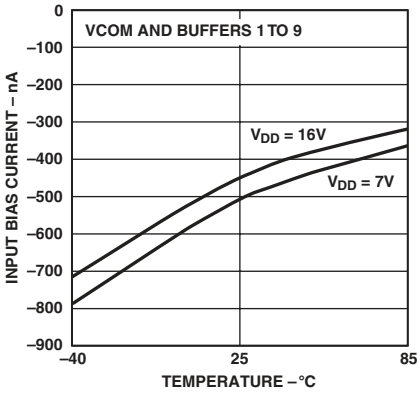
TPC 3. Input Offset Voltage vs. Temperature



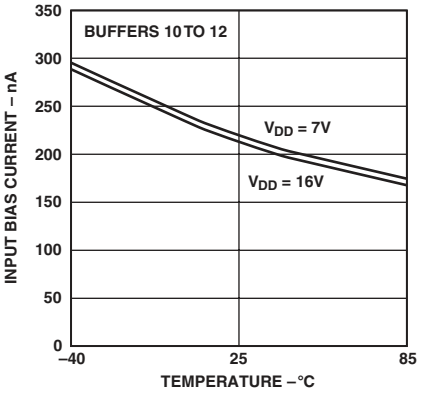
TPC 4. Offset Voltage vs. Common-Mode Voltage



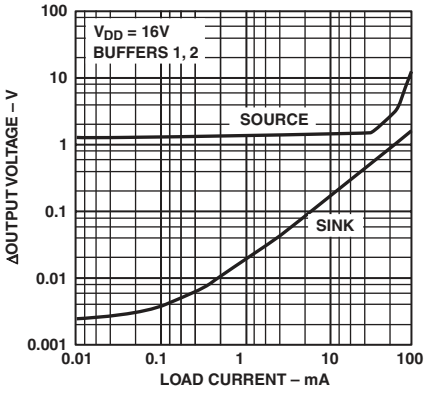
TPC 5. Offset Voltage vs. Common-Mode Voltage



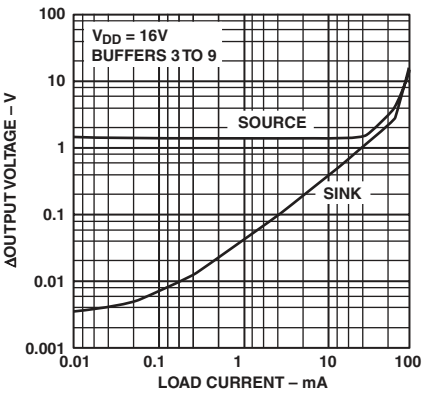
TPC 6. Input Bias Current vs. Temperature



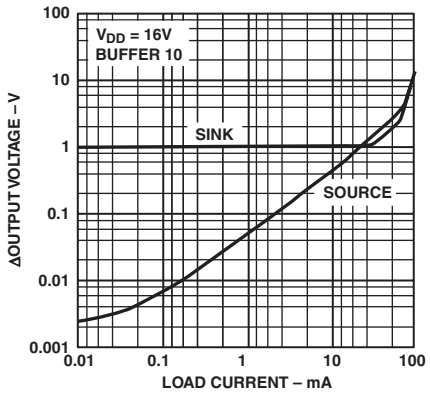
TPC 7. Input Bias Current vs. Temperature



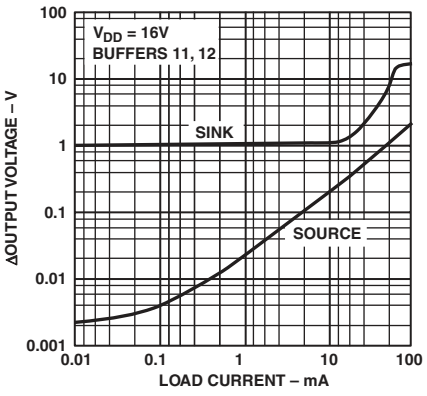
TPC 8. Output Voltage to Supply Rail vs. Load Current



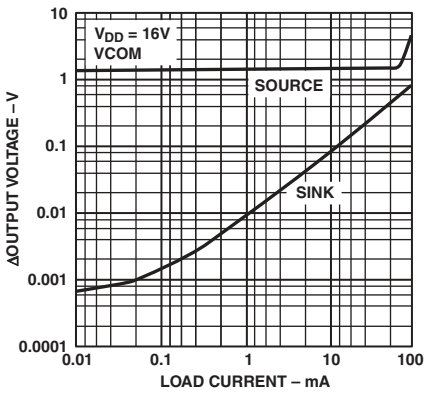
TPC 9. Output Voltage to Supply Rail vs. Load Current



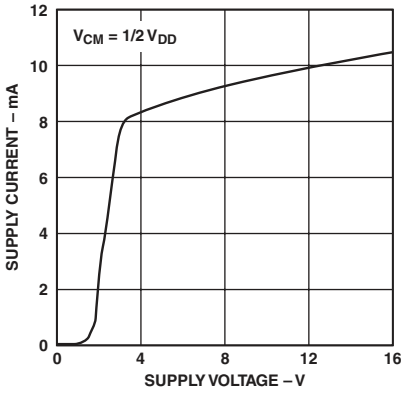
TPC 10. Output Voltage to Supply Rail vs. Load Current



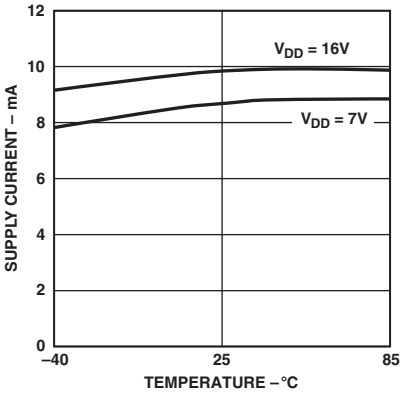
TPC 11. Output Voltage to Supply Rail vs. Load Current



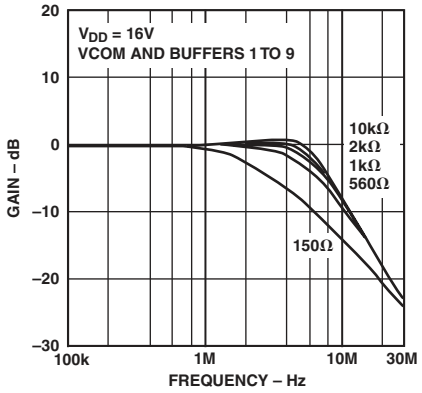
TPC 12. Output Voltage to Supply Rail vs. Load Current



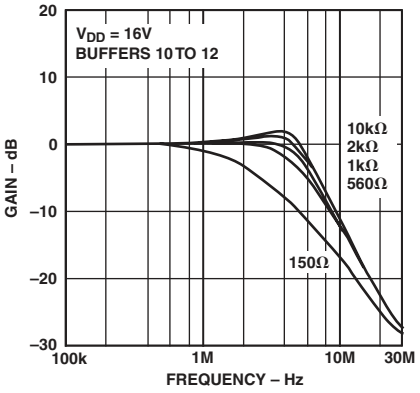
TPC 13. Supply Current vs. Supply Voltage



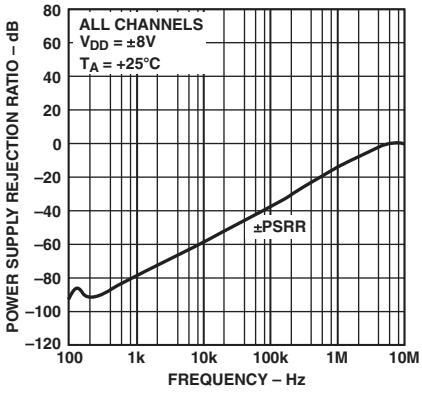
TPC 14. Supply Current vs. Temperature



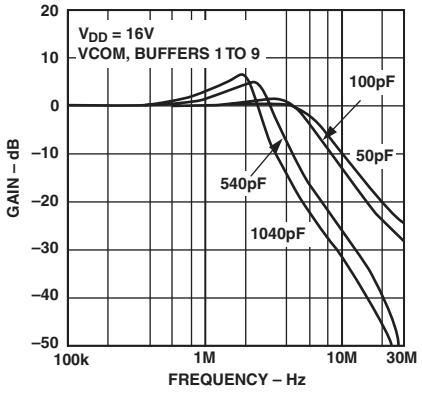
TPC 15. Frequency Response vs. Resistive Loading



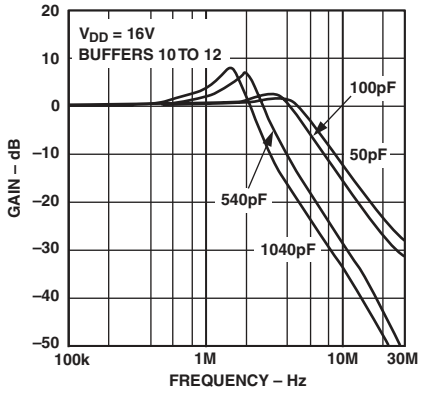
TPC 16. Frequency Response vs. Resistive Loading



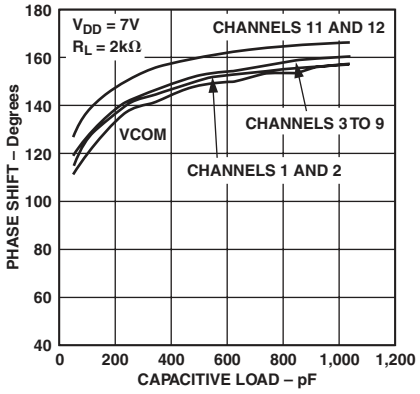
TPC 17. Power Supply Rejection Ratio vs. Frequency



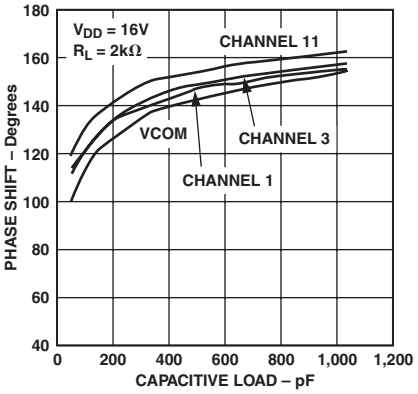
TPC 18. Frequency Response vs. Capacitive Loading



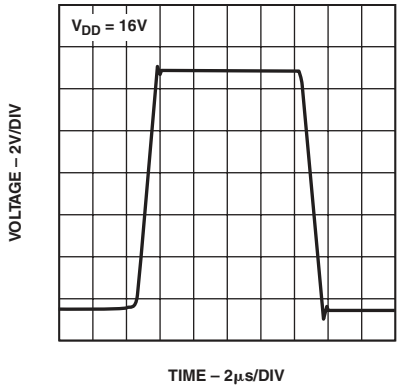
TPC 19. Frequency Response vs. Capacitive Loading



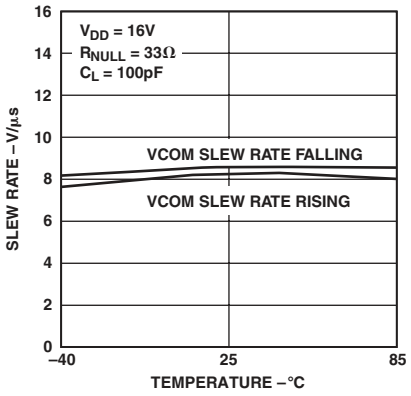
TPC 20. Input-Output Phase Shift vs. Capacitive Load



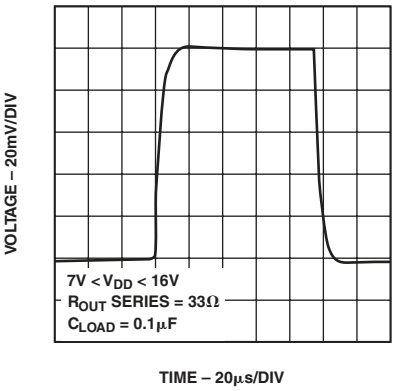
TPC 21. Input-Output Phase Shift vs. Capacitive Load



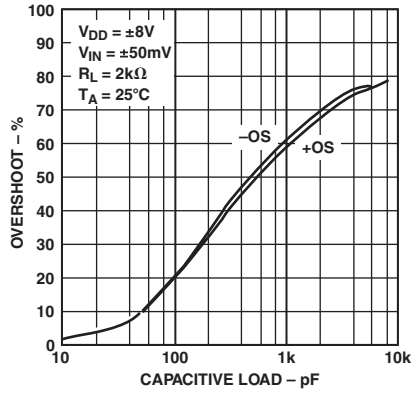
TPC 22. Large-Signal Transient Response



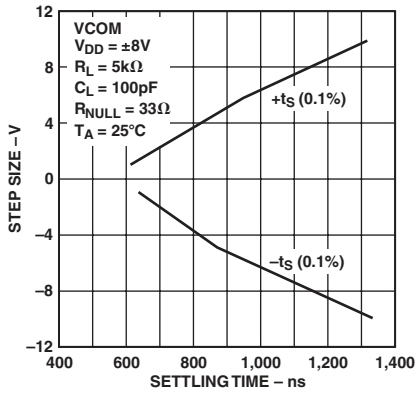
TPC 23. Slew Rate vs. Temperature



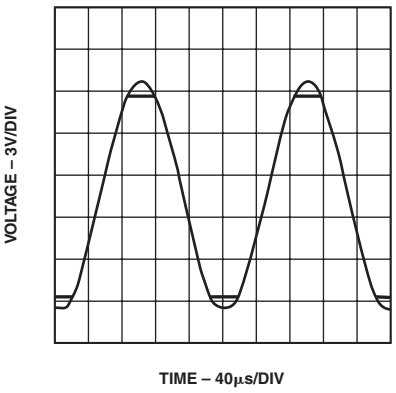
TPC 24. Small Signal Transient Response



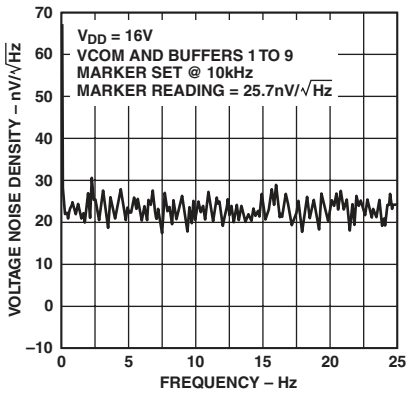
TPC 25. Small-Signal Overshoot vs. Capacitive Load



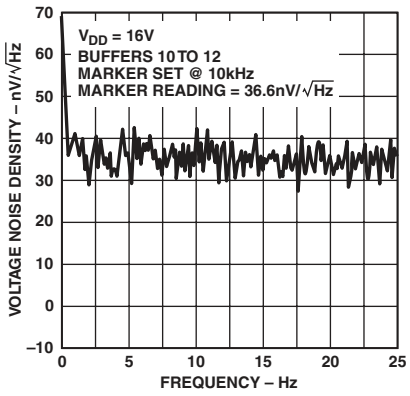
TPC 26. Settling Time vs. Step Size



TPC 27. No Phase Reversal



TPC 28. Voltage Noise Density vs. Frequency



TPC 29. Voltage Noise Density vs. Frequency

APPLICATIONS

LCD Gamma Reference Buffers

In high resolution TFT-LCD displays, gamma correction must be performed to correct the nonlinearity in the LCD panel's transmission characteristics. A typical TFT-LCD panel consisting of 256 grayscale levels takes an 8-bit digital word to select an appropriate gamma reference voltage. An 8-bit source driver may use 12 analog voltages that match the characteristic gamma curve for optimum panel picture quality. The ADD8701 is specifically designed to generate analog reference voltages to meet the gamma characteristics of an LCD panel used by the source driver. The gamma reference buffers offer 10 mA drive capability.

The ADD8701 is designed to meet the rail-to-rail capability needed by the application and yet offers a low cost-per-channel solution. The design maximizes the die area by offering channels to swing to the positive and negative rails. It is imperative that the channels swinging close to the supply rail be used for the positive gamma references and that the channels swinging close to GND be used for the negative gamma references. See Figure 2 for an example of the application circuit.

LCD VCOM Buffer

The output of the VCOM buffer is designed to control the voltage on the back plate of the LCD display. The buffer must be capable of sinking and sourcing capacitive pulse current. The amplifier stability is designed for high load capacitance. A high quality ceramic capacitor is recommended to supply short duration current pulses at the output. The VCOM buffer of the ADD8701 can handle up to 35 mA of continuous output current and can drive up to 1,000 nF of pure capacitive load.

Unused Buffers

Inputs of any unused buffer should be tied to the ground plane.

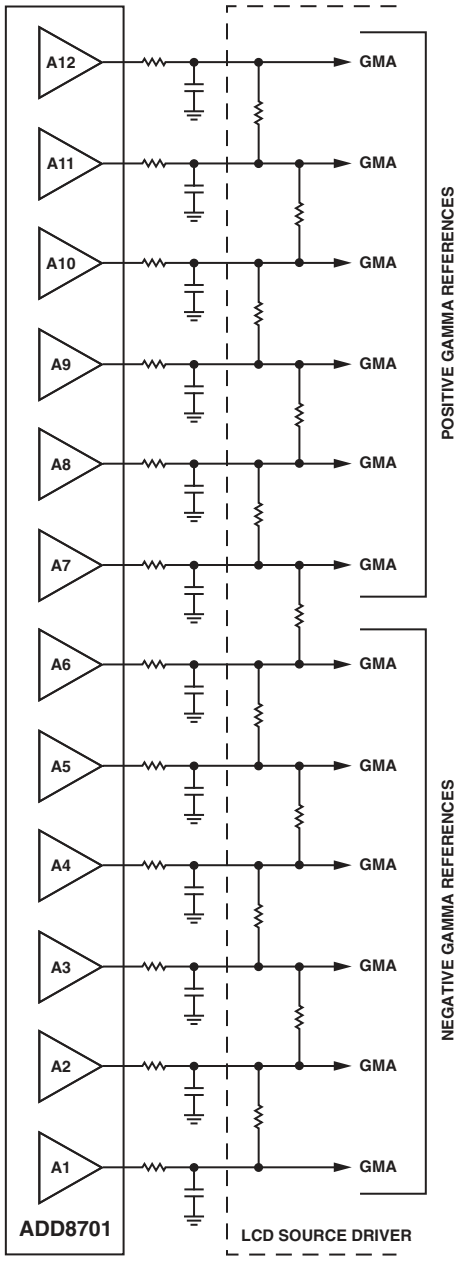
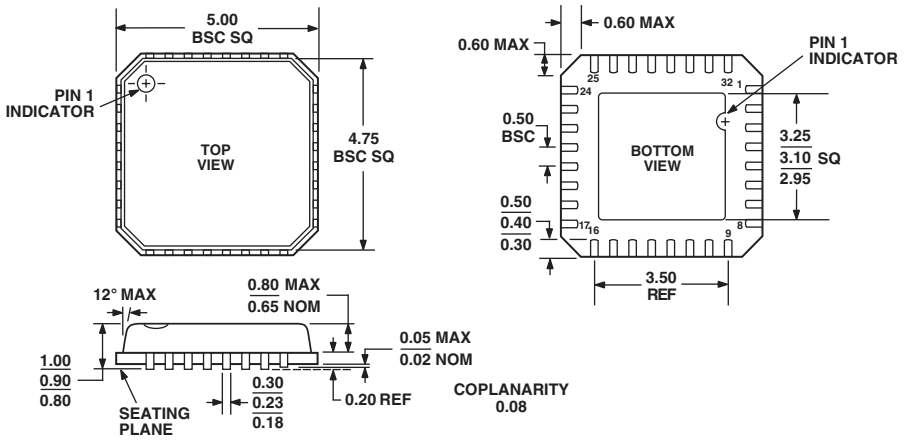


Figure 2. Application Circuit

OUTLINE DIMENSIONS

32-Lead Lead Frame Chip Scale Package [LFCSP]
(CP-32)

Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-220-VHHD-2

C03599–0–4/03(0)