



The Future of Analog IC Technology®

# MP4013B

## High-Brightness, High-Current Accuracy WLED Controller

### DESCRIPTION

The MP4013B is a current mode controller designed for driving the high brightness Light Emitting Diodes (LEDs) with wide supply voltage 8V-26V. It can be used in both Boost and SEPIC topologies.

The MP4013B drives external MOSFET with fixed frequency architecture to regulate the LED current, which is measured through an external current feedback resistor. The switching frequency can be programmed to meet kinds of applications. The cycle-by-cycle current limit can be programmed by the sense resistor on CS pin.

The MP4013B integrates a 600mV reference voltage for LED current feedback with  $\pm 1.2\%$  accuracy; a 5V reference voltage with  $\pm 1\%$  accuracy for the reference voltage for external circuit.

The MP4013B implements both DC input analog dimming and pulse signal input analog dimming function. The amplitude of the LED current could be controlled either by the level of a DC input signal or by the duty cycle of a pulse signal. The MP4013B also employs fast and deep PWM dimming to the LED current with high dimming ratio.

MP4013B integrates Under-Voltage Lockout, Over Voltage Protection, Over Current Protection, Short LED Protection, Short Output Protection, Short Inductor/diode Protection and OTP. The fault indicator is pulled low in fault condition.

The MP4013B is available in SOIC-16 package.

### FEATURES

- Constant-current WLED Driver
- 600mV Feedback Voltage with  $\pm 1.2\%$  Accuracy
- 8V-26V Input Voltage
- Programmable Switching Frequency
- Leading Edge Blanking for Current Sense
- High Dimming Ratio Fast PWM Dimming
- DC Input or Pulse Signal Input Analog Dimming
- 5V Reference Voltage with  $\pm 1\%$  Accuracy
- External PWM Dimming MOS Driver
- Programmable Input Bus Voltage UVLO
- Soft Start @ Any Startup Condition
- Over Voltage Protection
- Short LED Protection
- Short Output Protection
- Over Current Protection
- Short Inductor/Diode Protection
- Fault Indicator
- VIN UVLO
- Thermal Shutdown
- Available in SOIC-16 package

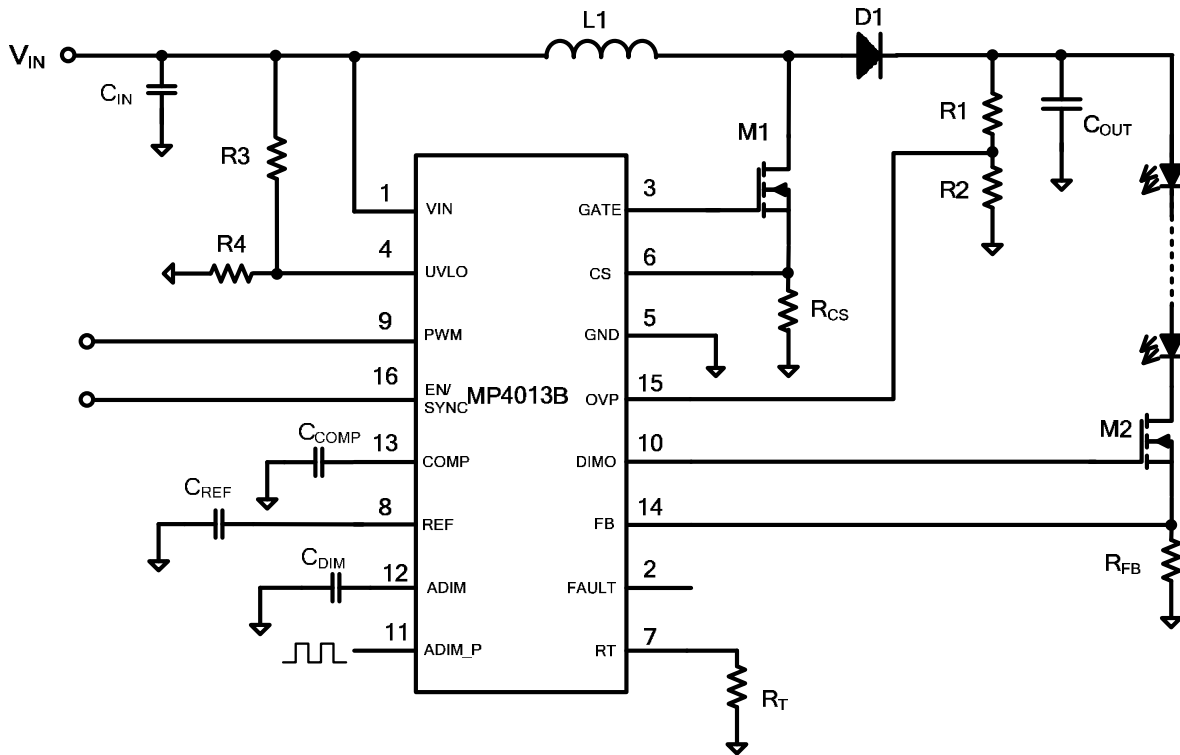
### APPLICATIONS

- LCD Backlighting applications
- DC/DC LED Driver applications
- General Illumination
- Industrial Lighting
- Automotive/ Decorative LED Lighting

All MPS parts are lead-free, halogen free, and adhere to the RoHS directive. For MPS green status, please visit MPS website under Quality Assurance.

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### TYPICAL APPLICATION



### ORDERING INFORMATION

Part Number*	Package	Top Marking
MP4013BGS	SOIC-16	See Below

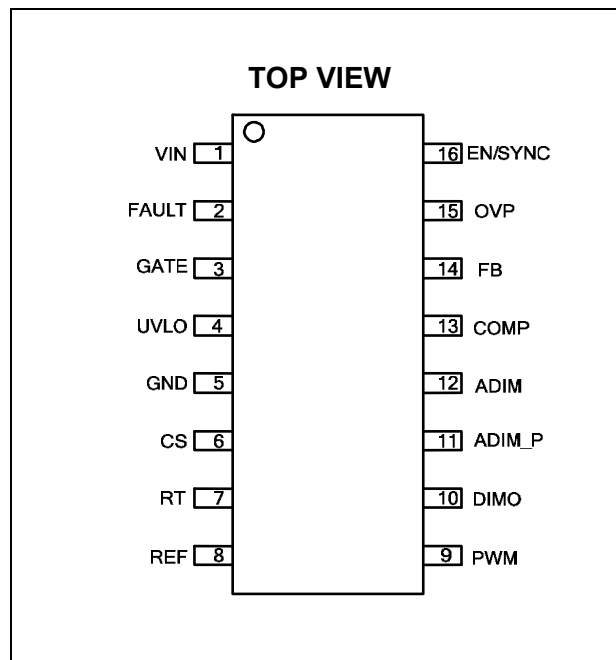
\* For Tape & Reel, add suffix -Z (e.g. MP4013BGS-Z);

### TOP MARKING

**MPSYYWW**  
**MP4013B**  
**LLLLLLLLL**

MPS: MPS prefix;  
 YY: year code;  
 WW: week code;  
 MP4013B: product code of MP4013BGS;  
 LLLLLLLLL: lot number;

### PACKAGE REFERENCE



**ABSOLUTE MAXIMUM RATINGS** <sup>(1)</sup>

V <sub>IN</sub> , V <sub>EN</sub> , V <sub>ADIM_P</sub> .....	-0.3V to 28V
V <sub>FAULT</sub> .....	-0.3V to 26V
V <sub>GATE</sub> , V <sub>DIMO</sub> .....	-0.3V to 19V
All Other Pins.....	-0.3V to 6.5V
Junction Temperature.....	150°C
Lead Temperature.....	260°C
Continuous Power Dissipation (T <sub>A</sub> = +25°C) <sup>(2)</sup>	
SOIC16.....	1.56 W

**Recommended Operating Conditions** <sup>(3)</sup>

IN Supply Voltage V <sub>IN</sub> .....	8V to 26V
Operating Junction Temp. T <sub>J</sub> .....	-40°C to +125°C

<b>Thermal Resistance</b> <sup>(4)</sup>	<b>θ<sub>JA</sub></b>	<b>θ<sub>JC</sub></b>	
SOIC-16.....	80....	35...	°C/W

**Notes:**

- 1) Exceeding these ratings may damage the device.
- 2) The maximum allowable power dissipation is a function of the maximum junction temperature T<sub>J</sub> (MAX), the junction-to-ambient thermal resistance θ<sub>JA</sub>, and the ambient temperature T<sub>A</sub>. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P<sub>D</sub> (MAX) = (T<sub>J</sub> (MAX)-T<sub>A</sub>)/θ<sub>JA</sub>. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
- 3) The device is not guaranteed to function outside of its operating conditions.
- 4) Measured on JESD51-7, 4-layer PCB.

## ELECTRICAL CHARACTERISTICS

$V_{IN} = 24V$ ,  $T_A = +25^{\circ}C$ , unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Operating Input Voltage	$V_{IN}$		7.6		26	V
Supply Current (Quiescent)	$I_Q$	$V_{FB}=1V$		1.1	1.3	mA
VIN Under Voltage Lockout	$V_{IN-UVLO}$	$V_{IN}$ Rising	6.7	7.1	7.5	V
VIN Under Voltage Lockout Hysteresis	$V_{IN-HYS}$		320	395	470	mV
<b>Feedback</b>						
FB Feedback Voltage	$V_{FB}$		593	600	607	mV
FB Input Current	$I_{FB}$	$V_{FB}=600mV$	-0.1		0.1	$\mu A$
<b>Reference</b>						
Reference Voltage	$V_{REF}$		4.95	5	5.05	V
Reference Line Regulation	$V_{REFLINE}$	0.1 $\mu F$ bypass capacitor, $I_{REF}=0$ $V_{IN}=8-24V$	0		25	mV
Reference Load Regulation	$V_{REFLOAD}$	0.1 $\mu F$ bypass capacitor, $I_{REF}=0-500\mu A$	0		50	mV
<b>UVLO</b>						
UVLO Threshold	$V_{UVLO}$	UVLO Rising	2.25	2.37	2.49	V
UVLO Hysteresis	$V_{UVLO-HYS}$		110	160	210	mV
UVLO pin Leakage Current	$I_{UVLO}$		-1		1	$\mu A$
<b>Oscillator</b>						
Oscillator Frequency	$f_{OSC1}$	$R_T=100k\Omega$	510	590	670	kHz
Oscillator Frequency	$f_{OSC2}$	$R_T=499k\Omega$	112	130	148	kHz
Maximum Duty Cycle	$D_{MAX}$	$R_T=499k\Omega$	95	97.5		%
<b>GATE</b>						
GATE High Threshold	$V_{GATE}$		12	13	13.8	V
GATE Output Rise Time	$T_{RISE}$	$C_{GATE}=1nF$		40		ns
GATE Output Fall Time	$T_{FALL}$	$C_{GATE}=1nF$		40		ns
GATE Source Current <sup>(5)</sup>	$I_{GATE-SO}$	$V_{GATE}=0V$		1.5		A
GATE Sink Current <sup>(5)</sup>	$I_{GATE-SI}$	$V_{GATE}=13V$		0.7		A
<b>Enable</b>						
EN High Threshold	$V_{EN-HI}$	$V_{EN}$ Rising	1.5			V
EN Low Threshold	$V_{EN-LO}$	$V_{EN}$ Falling			0.8	V
EN Input Current	$I_{EN}$	$V_{EN}=3.3V$		3	4	$\mu A$
<b>PWM Dimming</b>						
PWM High Threshold	$V_{PWMI-HI}$	$V_{PMW}$ Rising	1.5			V
PWM Low Threshold	$V_{PWMI-LO}$	$V_{PMW}$ Falling			0.8	V
PWM Pull-down Resistance	$R_{PWM}$			1		M $\Omega$

**ELECTRICAL CHARACTERISTICS (continued)**
 $V_{IN} = 24V$ ,  $T_A = +25^{\circ}C$ , unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
<b>DIMO</b>						
DIMO High Threshold	$V_{DIMO}$	$V_{IN}=24V$	12.8	13.3	13.8	V
DIMO Source Current <sup>(5)</sup>	$I_{DIMO-SO}$	$V_{DIMO}=0V$		0.1		A
DIMO Sink Current <sup>(5)</sup>	$I_{DIMO-SI}$	$V_{DIMO}=13V$		0.2		A
<b>Analog Dimming</b>						
Maximum Analog Dimming Threshold	$V_{ADMAX}$		2.25	2.34	2.43	V
Dimming Linearity	$V_{FB\_ADIM}$	$V_{ADIM}=24mV$		9.8		mV
		$V_{ADIM}=100mV$		28.4		mV
		$V_{ADIM}=240mV$		63.3		mV
		$V_{ADIM}=480mV$		123.3		mV
		$V_{ADIM}=720mV$		183.3		mV
ADIM_P High Threshold	$V_{ADIM\_PHI}$		1.5			V
ADIM_P Low Threshold	$V_{ADIM\_PLO}$				0.8	V
ADIM_P Pull Down Resistor	$R_{ADIM\_P}$			1		MΩ
ADIM_P Floating (when the voltage high than this level, IC take it as no pulse signal applied)	$V_{ADIM\_PF}$		6	6.45	6.9	V
<b>Current Sense</b>						
Current Limit Value	$V_{CL}$	Duty=0	435	485	535	mV
OCP Detect Voltage	$V_{OCP}$	Over Current Protection		490		mV
Leading Edge Blanking Time	$T_{BLANK}$		100	180	250	ns
<b>Compensation</b>						
Transconductance of Error Amplifier	$G_{EA}$		280	370	460	μA/V
Maximum Sourcing/Sinking Current	$I_{EA}$			80		μA
Soft Start Current	$I_{SS}$	$V_{FB}<0.8 \cdot I_{REF}$	15	22	30	μA
Time for COMP Saturated Protection Detection	$T_{COMP}$			2048		cycle
<b>Over Voltage Protection</b>						
OVP Threshold	$V_{OVP-TH}$		4.9	5	5.1	V
OVP Threshold Hysteresis	$V_{OVP-HYS}$			440		mV
SCP Protection Threshold	$V_{OVP-SCP}$		250	300	350	mV
<b>Output Short Protection</b>						
FB Short Protection Threshold			1.15	1.22	1.29	V
Propagation time for short circuit detection	$T_{OFF}$	FB=1.3V, FAULT goes form high to low		1.4	2	μs
Thermal Shutdown <sup>(5)</sup>				160		°C

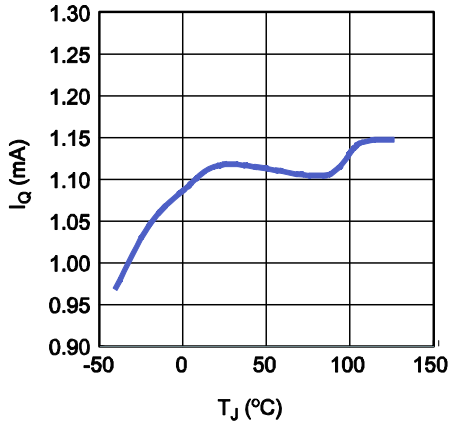
**Notes:**

5) Guaranteed by design

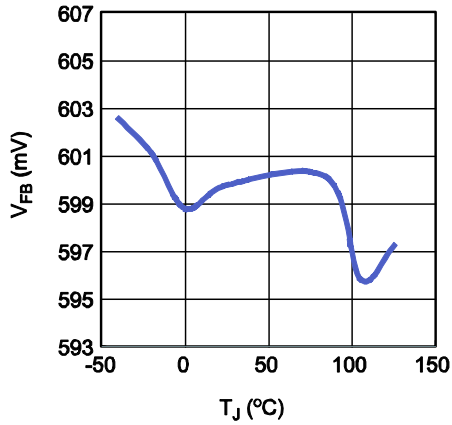
## TYPICAL PERFORMANCE CHARACTERISTICS

VIN=24V, Otherwise noticed.

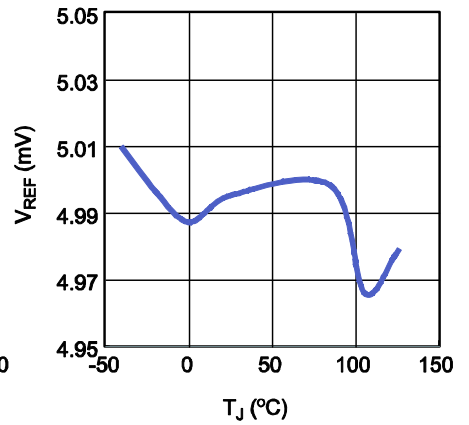
**Quiescent Current vs. T<sub>J</sub>**



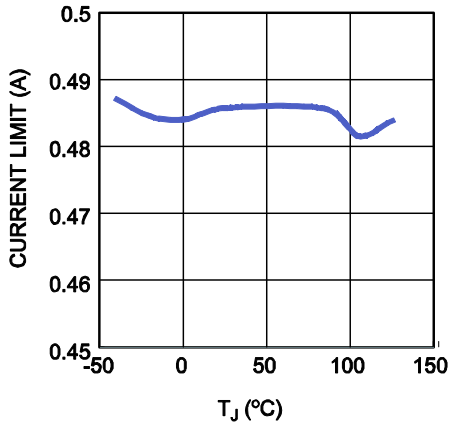
**FB Voltage vs. T<sub>J</sub>**



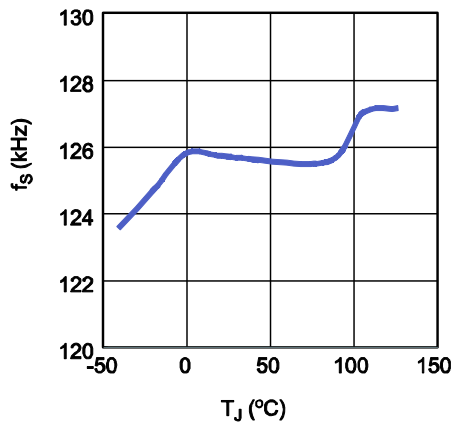
**Reference Voltage vs. T<sub>J</sub>**



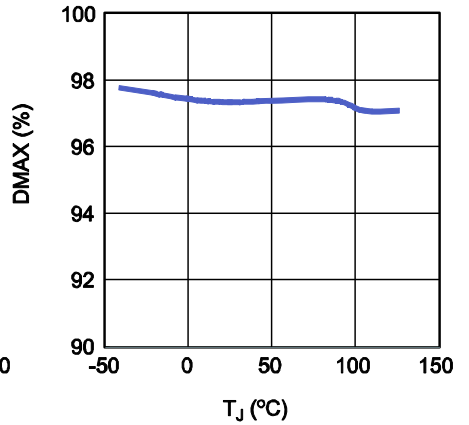
**Current Limit Threshold vs. T<sub>J</sub>**



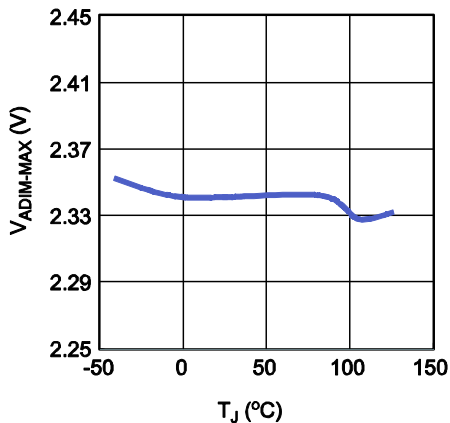
**Switch Frequency vs. T<sub>J</sub>**  
R<sub>T</sub>=499kΩ



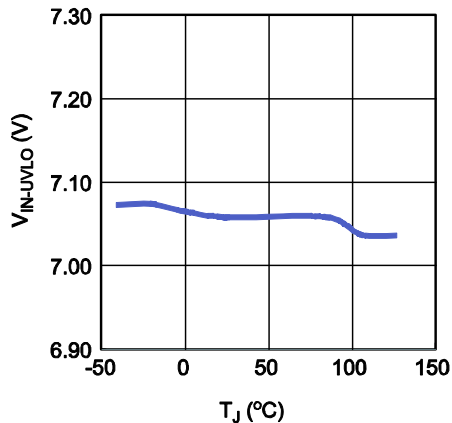
**Maximum Duty vs. T<sub>J</sub>**  
R<sub>T</sub>=499kΩ



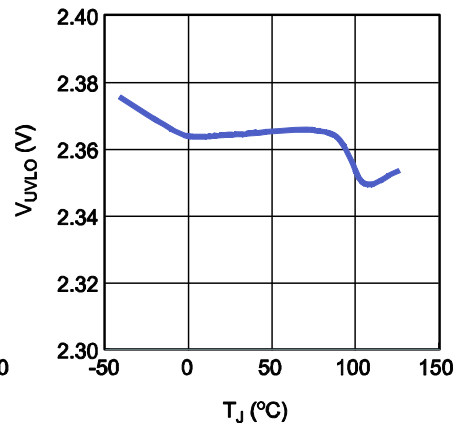
**Analog Dimming High Threshold vs. T<sub>J</sub>**



**VIN UVLO Rising Threshold vs. T<sub>J</sub>**



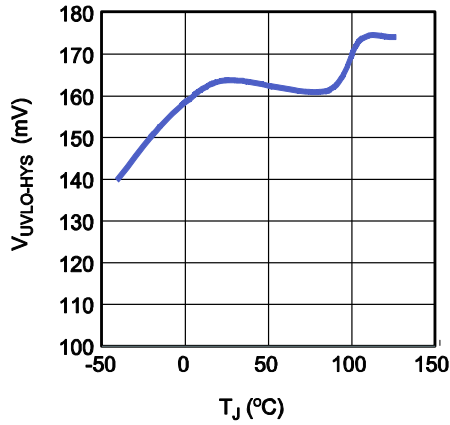
**UVLO Rising Threshold vs. T<sub>J</sub>**



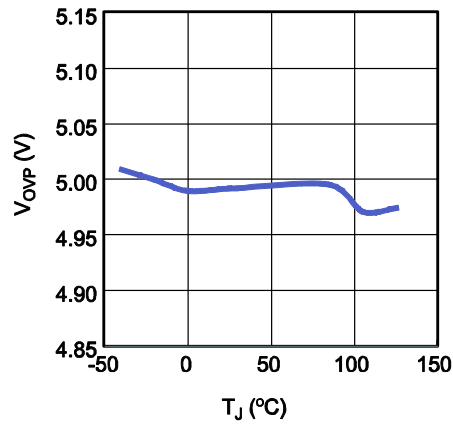
## TYPICAL PERFORMANCE CHARACTERISTICS

VIN=24V, Otherwise noticed.

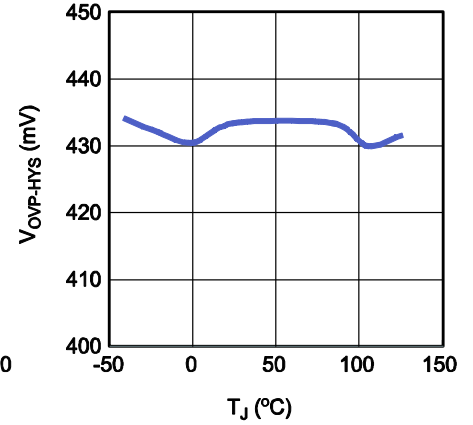
**UVLO Hysteresis vs. T<sub>J</sub>**



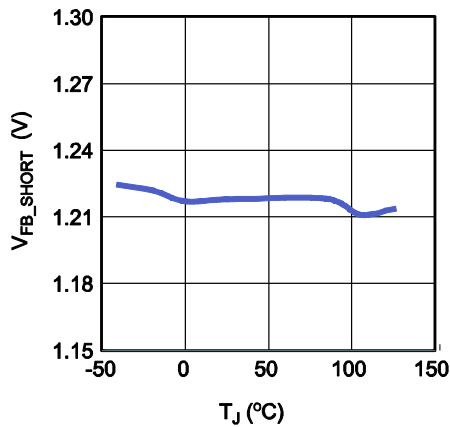
**OVP Rising Threshold vs. T<sub>J</sub>**



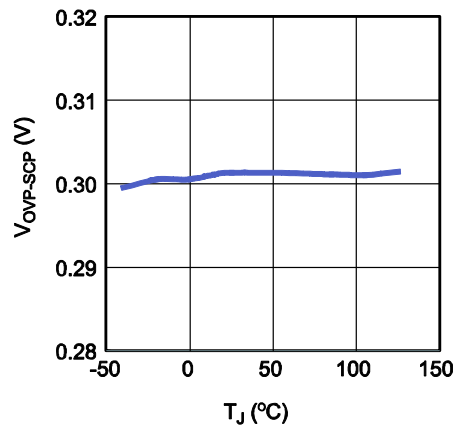
**OVP Hysteresis vs. T<sub>J</sub>**



**FB Short Protection Threshold vs. T<sub>J</sub>**



**SCP Threshold vs. T<sub>J</sub>**

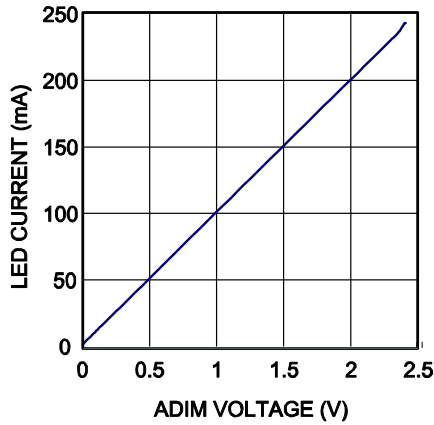




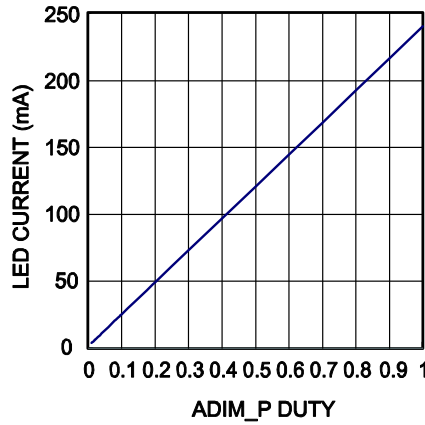
## TYPICAL PERFORMANCE CHARACTERISTICS

$P_{VIN}$ (bus voltage)=36V,  $V_{IN}$ (IC supply)=12V,  $V_{LED}$ =150V,  $I_{LED}$ =240mA,  $f_s$ =100kHz,  $L$ =330 $\mu$ H. Otherwise noticed.

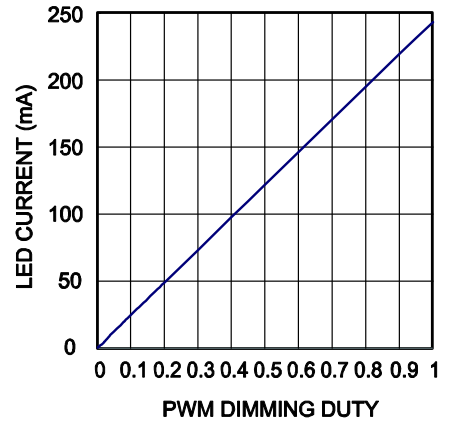
**DC-input Analog Dimming Curve**



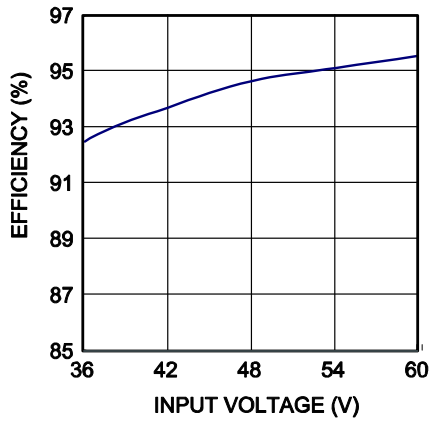
**Pulse-Input Analog Dimming**



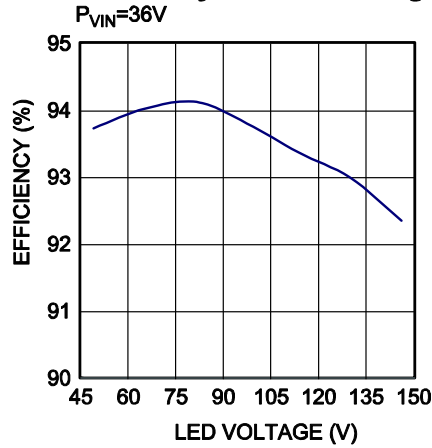
**PWM Dimming Curve**



**Efficiency vs. Input Voltage**

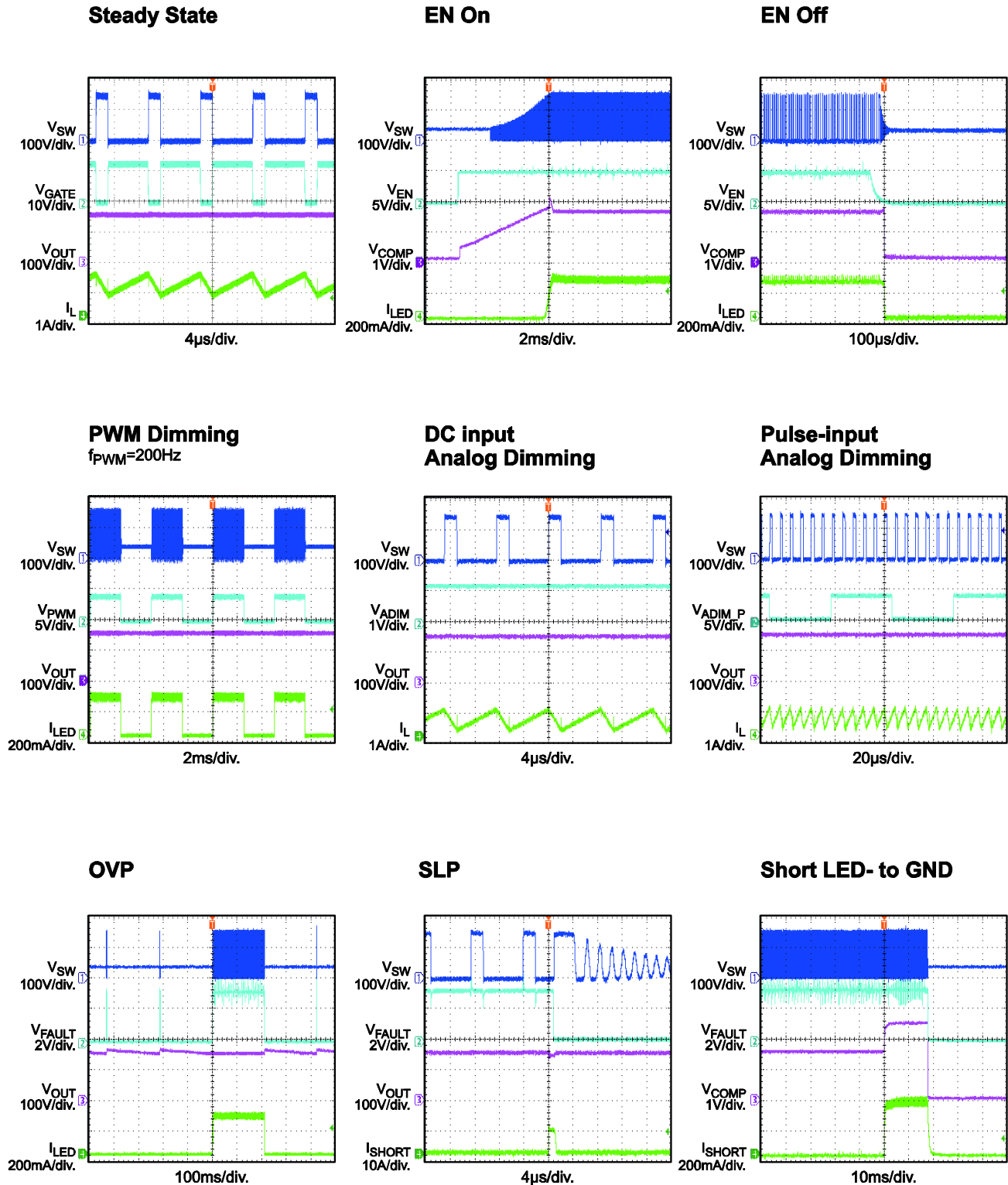


**Efficiency vs. LED Voltage**



## TYPICAL PERFORMANCE CHARACTERISTICS

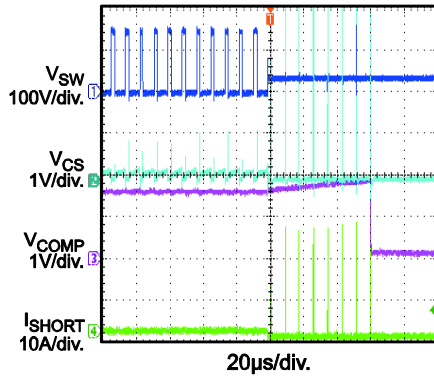
$V_{IN(bus\ voltage)}=36V$ ,  $V_{IN(IC\ supply)}=12V$ ,  $V_{LED}=150V$ ,  $I_{LED}=240mA$ ,  $f_s=118kHz$ ,  $L=330\mu H$ . Otherwise noticed.



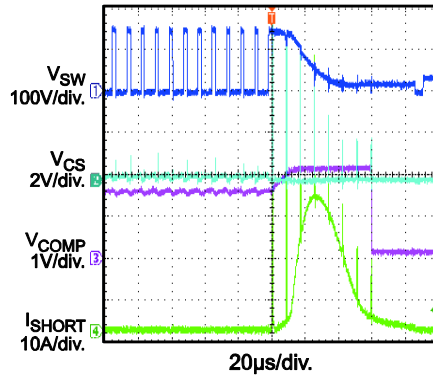
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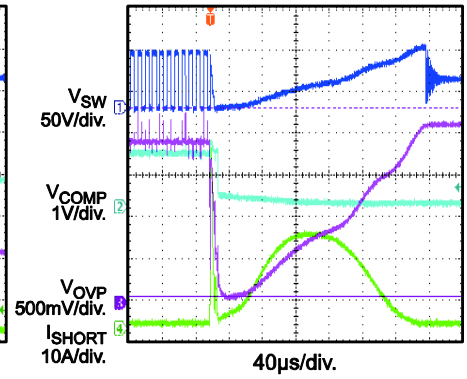
**Short Inductor**



**Short Diode**



**Short to GND**



## PIN FUNCTIONS

Pin #	Name	Pin Function
1	VIN	Input Supply Pin, 8-26V. It is the input of internal linear regulator. Must be locally bypassed.
2	FAULT	Fault Indication Output Pin, open drain. FAULT is high-Z during normal operation, and pulled to GND when fault is triggered.
3	GATE	External MOSFET Gate Driver Pin.
4	UVLO	Input Voltage Bus UVLO Pin. A voltage higher than UVLO threshold (2.37V) to enable IC.
5	GND	Ground.
6	CS	Switch Current Sense Input Pin. It is used to sense the current of the external power FET. It integrates a built-in blanking time to avoid switching noise interruption.
7	RT	Switching frequency set Pin. A resistor connected between this pin and GND sets the frequency.
8	REF	Reference Output Pin. 5V reference voltage with $\pm 1\%$ accuracy. Must be locally bypassed.
9	PWM	PWM Dimming Input Pin. Apply a PWM signal on this pin for brightness control. The GATE and DIMO are disabled when PWM signal is low. The GATE and DIMO are enabled when PWM signal is high.
10	DIMO	External Dimming MOS Driving Signal Pin. This pin is pulled down to GND when the PWM signal is Low, or the protection is triggered.
11	ADIM_P	Pulse signal Input Analog Dimming Input Pin. Apply a high-frequency pulse signal on this pin while doing pulse signal input analog dimming. Pull this pin high (>6.9V) to disable the pulse-signal-input analog dimming function.
12	ADIM	Analog Dimming Input Pin. Apply a DC voltage from 0 to 2.34V to adjust the amplitude of LED current from minimum to full scale to implement the DC analog dimming function. Place a capacitor on this pin while doing pulse signal input analog dimming. Keep the voltage of this pin higher than 2.43V when analog dimming is not required.
13	COMP	Compensation Pin. This pin is used to compensate the regulation control loop. Connect a capacitor or a series RC network from COMP to GND. COMP pin is also used for soft start. At IC start up, the internal error sourcing/sinking current is limited until the output current reaches 80% of setting current.
14	FB	Feedback Input Pin. 600mV internal feedback voltage. Connect a current sense resistor from FB to GND. The FB voltage is higher than 1.22V for 1us, the short load protection is triggered, and IC latch off.
15	OVP	Over Voltage Protection Input Pin. Connect a resistor divider from output to this pin to program the OVP threshold. When the voltage of this pin reaches 5V, the MP4013B triggers over voltage protection.
16	EN/SYNC	Enable/Switching frequency Synchronization Pin. A high level to enable the IC. Apply a high frequency (>40kHz) pulse signal on this pin, the switching frequency can be synchronized.

## OPERATION

MP4013B drives external MOSFET with current mode architecture to regulate the LED current, which is measured through an external current sense resistor.

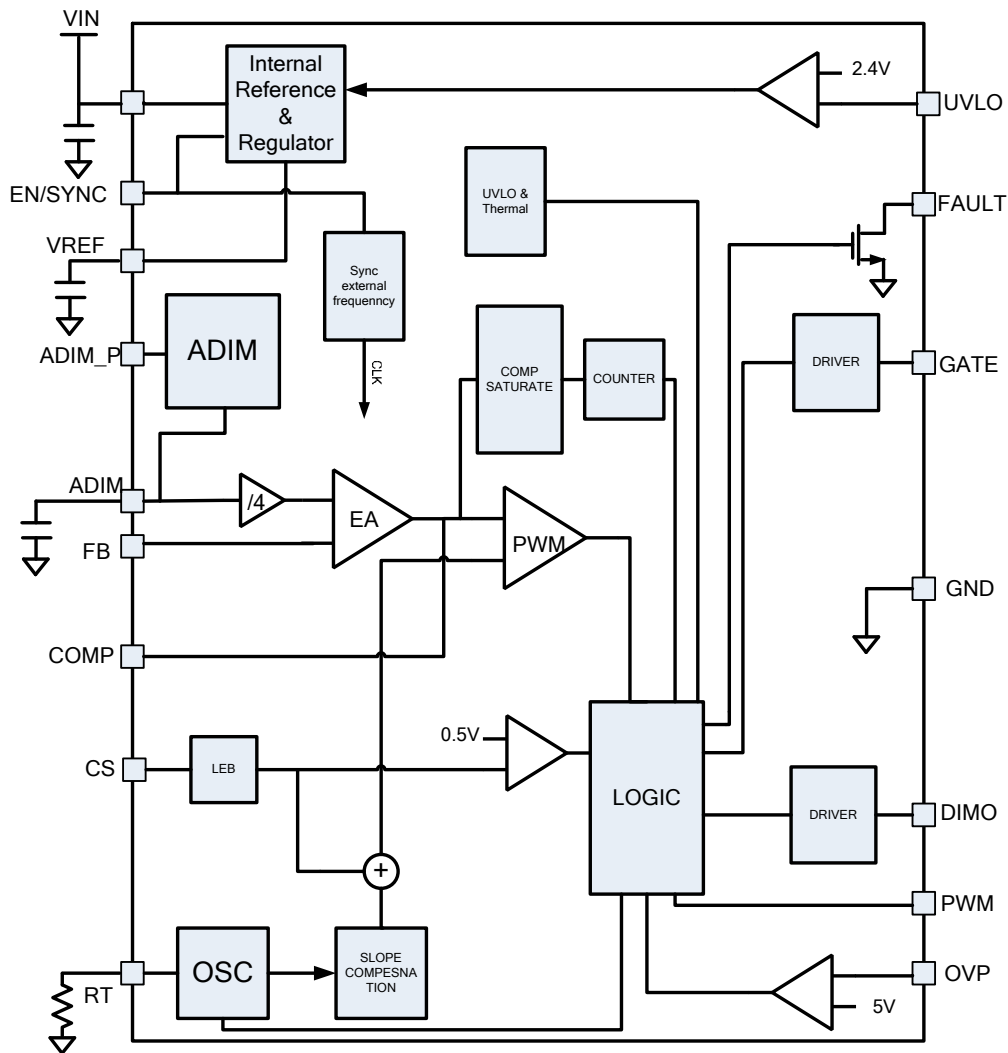
MP4013B employs a special circuit for regulating the internal power supply, which covers a wide input voltage from 8V to 26V. MP4013B has a 5V reference with  $\pm 1\%$  accuracy, which is used as the reference of external circuit.

The switching frequency of MP4013B can be programmed through the resistor between RT pin and GND to meet variable specifications.

The slope compensation is integrated to avoid sub harmonic resonant when duty cycle is greater than 0.5. The cycle-by-cycle current limit can be programmed by the sense resistor on CS pin.

MP4013B implements both DC input analog dimming and pulse signal input analog dimming.

MP4013B integrates Under-Voltage Lockout, Over Voltage Protection, Over Current Protection, Short LED protection, Short Circuit Protection, Short Inductor/diode Protection and OTP.

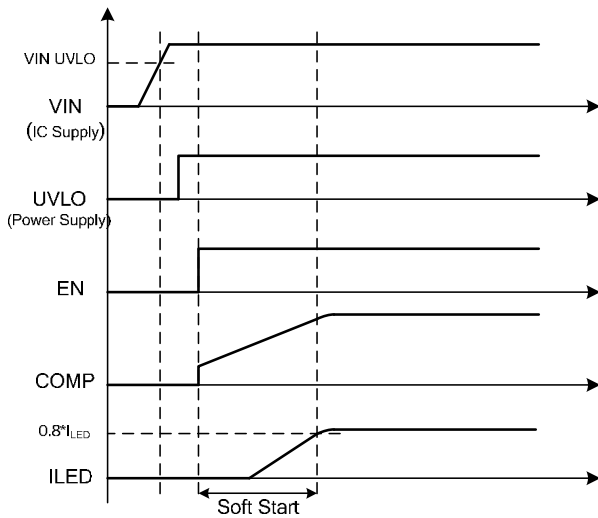


**Figure 1: Functional Block of MP4013B**

**Soft Start**

MP4013B implements soft start by limiting the current of the internal error amplifier when startup. The COMP is firstly jump to its clamp voltage (~0.3V), and then the sourcing/ sinking current of the internal error amplifier is limited to charge up external COMP capacitor. IC is always in soft start mode until the output current reaches 0.8 of the setting value to achieve the soft start.

The soft start process is showing the figure 2, note that the VIN UVLO, UVLO and EN get the same priority to ensure the soft start at any startup condition.



**Figure 2: Soft Start Process**

**Analog Dimming**

MP4013B implements DC input analog dimming and pulse signal input analog dimming.

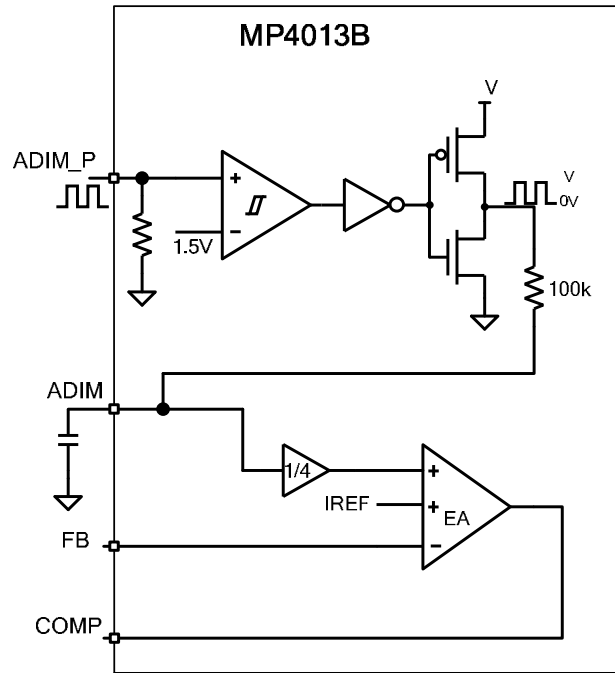
For DC input analog dimming, apply a DC voltage from 0-2.34V on ADIM pin to linearly adjust internal LED current reference voltage from minimum to the maximum value.

For pulse-signal-input analog dimming, place a capacitor on the ADIM pin and apply a pulse signal (>10 kHz recommended) on ADIM\_P pin. This external pulse signal is adjusted internally and forms an internal pulse signal with the same duty and internal reference amplitude. Through an R-C filter, the average voltage of this internal pulse signal is gotten on ADIM pin. Adjust the duty cycle of the pulse signal on ADIM\_P to

adjust the voltage on ADIM pin and realize the pulse signal input analog dimming.

Pull ADIM\_P high (>6.9V) to disable the pulse-signal-input analog dimming.

Connect ADIM pin to 2.43V or higher, if neither analog dimming or pulse-signal-input analog dimming is not used.



**Figure 3: Analog Dimming Functional Block**

**PWM Dimming**

PWM dimming can be achieved by applying a PWM signal on PWM pin. When the PWM signal is high, the GATE and DIMO outputs are enabled, and the output of the internal error amplifier is connected to the external compensation network. So the LED current is regulated accurately. When the PWM signal goes low, the GATE signal is disabled, and the DIMO pin is pulled down to GND to turn off the external dimming MOSFET. Meanwhile, the output of the internal EA is disconnected from the compensation network. Thus, the COMP voltage will be held by the external capacitor. And the dimming MOSFET can prevent the output voltage from being discharged, which helps to achieve the high-speed and deep-ratio PWM dimming with better linear dimming performance.

To avoid the LED flicker in small ratio PWM dimming such as 0.1% PWM dimming duty, the

oscillator is synchronized by the PWM dimming signal.

**Protection**

MP4013B includes Under-Voltage Lockout, Over Voltage Protection, Short Load Protection, Short Circuit Protection, Over Current Protection and Short Inductor/diode Protection. If the fault conditions are detected, the Gate, DIMO, COMP and Fault pins are pulled down.

**A Under Voltage Lockout**

MP4013B integrates VIN UVLO. The internal circuit does not work until the VIN voltage reaches 7.1V. The hysteresis of VIN UVLO is 395mV.

**B. Over Voltage Protection**

The Over Voltage Protection is detected by the voltage of OVP pin. When the OVP voltage rise to its high threshold, the over voltage protection is triggered. The GATE, DIMO, COMP and Fault pin are pulled down. After the OVP voltage decreases to its low threshold, the IC tries to recover.

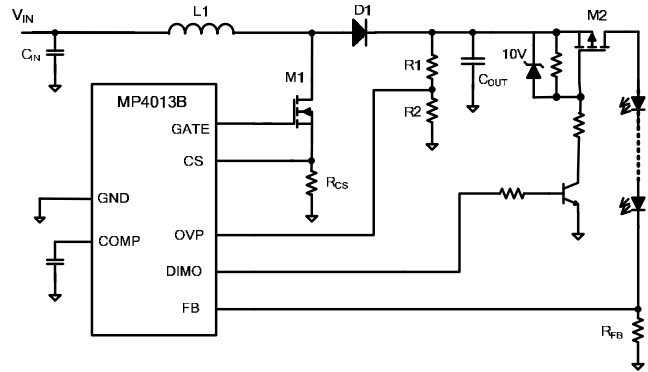
**C. Short Load Protection**

In short load condition, a large short current will be detected by FB sense resistor. If the FB sensed voltage is higher than 1.22V for 1.4us, the Short Load Protection is triggered, IC latch off, and FAULT pin pulls to low.

**D. Short Circuit Protection**

When short circuit at normal operation, the output voltage is pulled low and no current is sensed on FB pin. If the conditions  $OVP < 300mV$ ,  $FB < 0.3 \times IREF$ ,  $COMP > 1V$  are satisfied, the protection is triggered and IC latch off.

Fig 5 shows another circuit for the short circuit protection. It uses a PMOS for PWM dimming and also for short circuit protection. When LED+ is shorted to GND, the MP4013B disables the output of DIMO, and the PMOS is disconnected.



**Figure 4: Short Circuit Protection Scheme**

**E. Over Current Protection (Short Inductor/ Diode Protection)**

MP4013B implements cycle-by-cycle current limit function for protection. In normal operation caused by over load and lower input voltage, the over current protection can be recoverable.

In some unexpected cases, like inductor or diode short cases, when the voltage of CS pin which is detected by external CS sense resistor hits latch off current limit value within mini-on time (around 300ns) for 7 consecutive cycles, the Over Current Protection is triggered, IC latch off.

**F. LED- to GND Short Protection**

In LED- to GND short condition, FB pin sense no current that makes the COMP charge to its saturated value. When COMP keeps saturated for 2048 switching cycles and FB is below 30% of internal IREF, protection is triggered, IC latches off.

## APPLICATION INFORMATION

### LED Current Setting

The LED current is set by LED current sense resistor ( $R_{FB}$ ).

$$R_{FB} = \frac{600\text{mV}}{I_{LED}}$$

### Switching Frequency Setting

The switching frequency is set by an external frequency resistor on RT pin.

$$R_T(\text{k}\Omega) = \frac{6.8 \times 10^4}{f_s(\text{kHz})} - 15.6$$

Set switching frequency to 100 kHz, a 664kOhm resistor is needed.

### Selecting Inductor

Select the inductor to make the circuit work in CCM (Continuous Conduction Mode).

$$L = \frac{V_{IN} \times (V_O - V_{IN})}{V_O \times \Delta I_L \times f_s}$$

Where,  $\Delta I_L$  is the peak-to-peak current of inductor current. Design the  $\Delta I_L$  30% to 60% of inductor average current.

$$I_{L\_AVG} = \frac{V_O \times I_{LED}}{V_{IN}}$$

Make sure the inductor saturated current is greater than the inductor peak current.

$$I_{L\_PK} = I_{L\_AVG} + \frac{1}{2} \Delta I_L$$

### Current Sense Resistor Setting

The cycle-by cycle current limit and slope compensation are both integrated. The current limit value can be programmed by the external CS resistor which connects from CS pin to GND. The maximum value of CS sense resistor can be set as follow:

$$R_{CS1}(\Omega) = \frac{0.435 - 0.27 \times D}{I_{L\_pk}}$$

The D is duty cycle of GATE signal, in CCM,

$$D = 1 - \frac{V_{IN}}{V_O}$$

The  $I_{L\_PK}$  is the peak current of inductor. The slope compensation is integrated to avoid sub-

harmonic resonant when duty is larger than 0.5 in CCM. The following must be satisfied.

$$R_{CS2}(\Omega) = 5.4 \times \frac{L(\mu\text{H}) \times f_s(\text{kHz})}{V_L(\text{V})} \times 10^{-4}$$

Where,  $V_L$  is the voltage across the inductor at GATE off.

$$V_L(\text{V}) = V_{O\max} - V_{IN\min}$$

The CS resistance must be smaller than  $R_{CS1}$  and  $R_{CS2}$

### Over Voltage Protection Setting

Choose a voltage divider ( $R1$ ,  $R2$  in typical application) to set the over voltage protection threshold:

$$V_{OVP} = 5V \times \frac{R1 + R2}{R2}$$

Normally set the OVP point 10%-20% higher than normal operation output voltage.

### Bus Voltage UVLO Setting

Choose a voltage divider ( $R3$ ,  $R4$  in typical application) to set the Input Bus Voltage UVLO point

$$V_{UVLO} = 2.37V \times \frac{R3 + R4}{R3}$$

Normally, set the Bus voltage UVLO point about 10%-20% lower than minimum input bus voltage.

### Selecting MOSFET and Diode

There are 2 MOSFET for MP4013B applications. One is for boost converter, the power MOSFET; and the other is for PWM dimming, the dimming MOSFET.

Choose the power MOS with voltage rating at least 20% higher than OVP voltage to ensure the safety in all condition. The RMS current of the MOSFET can be calculated as follow.

$$I_{RMS} = \sqrt{D \times (I_{L\_AVG}^2 + \frac{1}{12} \Delta I_L^2)}$$

Choose the dimming MOS with the voltage rating 20% higher than OVP voltage, and the current rating is about 3-5 of LED current.



Choose the diode with voltage rating greater than OVP point, at least 20% higher than OVP point, and the current rating greater than LED current.

**Selecting Input Capacitor**

The input capacitor reduces the surge current drawn from the input supply and switching noise from the device. Use ceramic capacitor with X7R dielectrics with low ESR and small temperature coefficients.

Select a capacitor to limit the input voltage ripple  $\Delta V_{IN}$  to less than 5% to 10% of its DC value.

$$C_{IN} \geq \frac{\Delta I_L}{8 \times \Delta V_{IN} \times f_s}$$

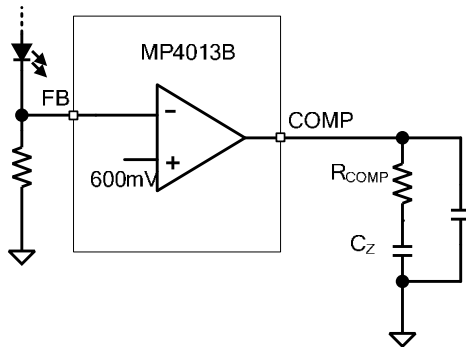
**Selecting Output Capacitor**

The output capacitor limits the output voltage ripple  $\Delta V_O$  (normally less than 1% to 5% of its DC value), and ensure feedback loop stability.

$$C_{OUT} \geq \frac{I_{LED} \times (V_O - V_{IN})}{\Delta V_O \times f_s \times V_O}$$

**Compensation Network Setting**

The MP4013B implements peak-current-mode control to regulate the LED current through a compensation network on COMP pin. Usually a RCC network is adopted for most applications, as showing in Figure 5.



**Figure 5: Compensation Network**

The transfer function of the compensation network is (assume  $C_Z \gg C_P$ ):

$$EA(s) \approx \frac{G_{EA} \times R_{FB}}{R_{FB} + R_{LED\_AC}} \times \frac{1}{s \times C_Z} \times \frac{1 + s \times C_Z \times R_{COMP}}{1 + s \times C_P \times R_{COMP}}$$

Where,  $G_{EA}$  is the transconductance of internal error amplifier.  $G_{EA}=370\mu A/V$ .  $R_{LED\_AC}$  is the

dynamic resistor of LED load, which can be gotten from

$$R_{LED\_AC} = \frac{\Delta V_{LED}}{\Delta I_{LED}}$$

The zero of compensation network is

$$f_{Z\_EA} = \frac{1}{2\pi \times C_Z \times R_{COMP}}$$

The pole of this compensation network is

$$f_{P\_EA} = \frac{1}{2\pi \times C_P \times R_{COMP}}$$

The power stage of boost converter is

$$f_{P\_PS} = \frac{1}{2\pi \times \left(\frac{V_O}{I_{LED}} \parallel (R_{LED\_AC} + R_{FB})\right) \times C_{OUT}}$$

Where,  $V_O$  is output voltage,  $I_{LED}$  is LED current,  $C_{OUT}$  is output capacitance. The right-half-plane (RHP) zero of boost converter stage is:

$$f_{RHP\_Z} = \frac{(1-D)^2 \times \frac{V_O}{I_{LED}}}{2\pi \times L}$$

Choose the cross frequency  $f_c$  below 1/3 of  $f_{RHP\_Z}$  to get the  $R_{COMP}$  value as follow.

$$R_{COMP} = \frac{R_{LED\_AC} + R_{FB}}{R_{FB}} \times \frac{f_c \times C_{OUT} \times 2\pi}{G_{EA} \times (1-D) \times G_{CS}}$$

Where,  $G_{CS}$  is conductance of CS circuit.

The zero of the compensation network is to compensate the power-stage pole.

$$C_Z = \frac{1}{2\pi \times f_{PS\_P} \times R_{COMP}}$$

The pole of the compensation network is to compensate the RHP zero.

$$C_P = \frac{1}{2\pi \times f_{RHP\_Z} \times R_{COMP}}$$

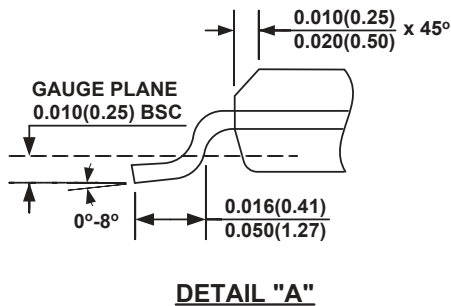
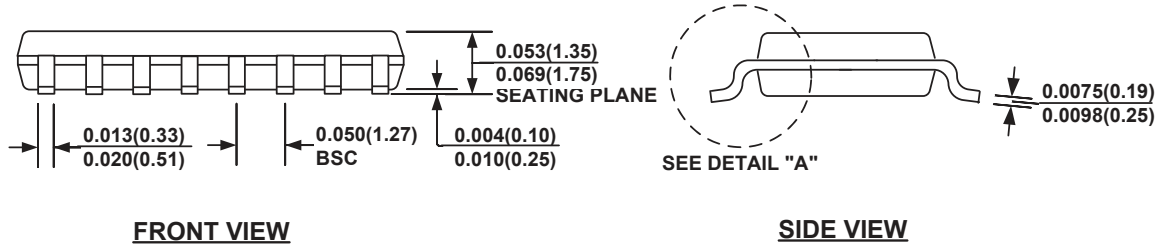
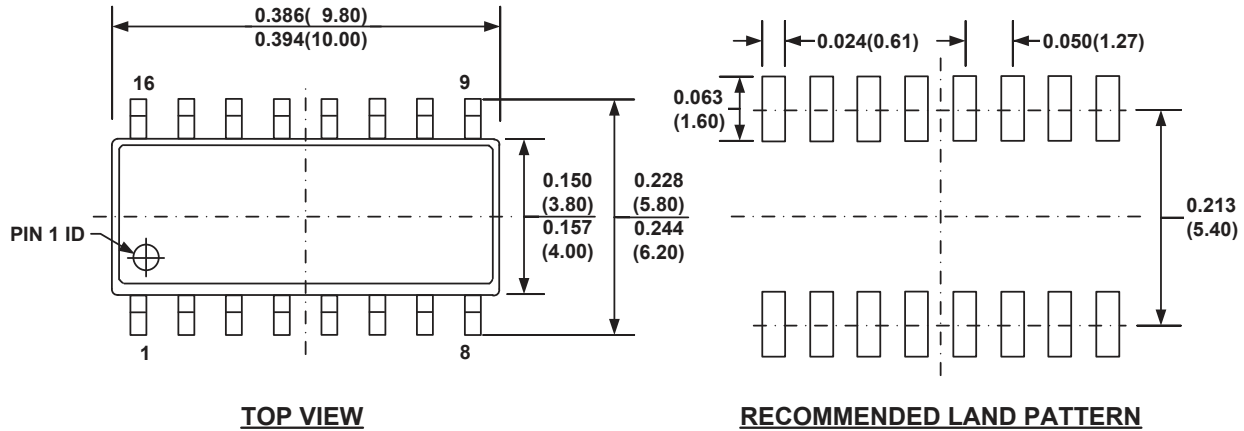
**Gate Drive Design**

A 10-20  $\Omega$  gate resistor is recommended as following figure.



**PACKAGE INFORMATION**

**SOIC-16**



**NOTE:**

- 1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
- 2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
- 3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
- 4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
- 5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION AC.
- 6) DRAWING IS NOT TO SCALE.

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