UM11183 KITFS85SKTEVM evaluation board Rev. 2.0 – 20 February 2019

User guide



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1 Introduction

This document is the user guide for the KITFS85SKTEVM evaluation board. This document is intended for the engineers involved in the evaluation, design, implementation, and validation of FS8500 Fail-safe system basis chip with multiple SMPS and LDO.

The scope of this document is to provide the user with information to evaluate the FS8500 Fail-safe system basis chip with multiple SMPS and LDO. This document covers connecting the hardware, installing the software and tools, configuring the environment and using the kit.

The KITFS85SKTEVM enables development on FS84/FS85 family of devices. The kit can be connected to the FlexGUI software which allows you to play with registers, try OTP configurations, and burn the part.

The devices can be placed and removed easily from the board by using the socket. The device OTP can be burned three times, which provides a good flexibility. This board supports FS84/FS85 family of devices.

2 Finding kit resources and information on the NXP web site

NXP Semiconductors provides online resources for this evaluation board and its supported device(s) on <u>http://www.nxp.com</u>.

The information page for KITFS85SKTEVM evaluation board is at <u>http://www.nxp.com/</u> <u>KITFS85SKTEVM</u>. The information page provides overview information, documentation, software and tools, parametrics, ordering information and a **Getting Started** tab. The **Getting Started** tab provides quick-reference information applicable to using the KITFS85SKTEVM evaluation board, including the downloadable assets referenced in this document.

2.1 Collaborate in the NXP community

The NXP community is for sharing ideas and tips, ask and answer technical questions, and receive input on just about any embedded design topic.

The NXP community is at <u>http://community.nxp.com</u>.

3 Getting ready

Working with the KITFS85SKTEVM requires the kit contents, additional hardware and a Windows PC workstation with installed software.

3.1 Kit contents

- Assembled and tested evaluation board in an anti-static bag
- 3.0 ft USB-STD A to USB-B-mini cable
- Two connectors, terminal block plug, 2 pos., str. 3.81 mm
- Three connectors, terminal block plug, 3 pos., str. 3.81 mm
- · Jumpers mounted on board

3.2 Additional hardware

In addition to the kit contents, the following hardware is necessary or beneficial when working with this kit.

• Power supply with a range of 8.0 V to 60 V and a current limit set initially to 1.0 A

3.3 Windows PC workstation

This evaluation board requires a Windows PC workstation. Meeting these minimum specifications should produce great results when working with this evaluation board.

• USB-enabled computer with Windows 7 or Windows 10

3.4 Software

Installing software is necessary to work with this evaluation board. All listed software is available on the evaluation board's information page at <u>http://www.nxp.com/</u><u>KITFS85SKTEVM</u> or from the provided link.

- FlexGUI latest version
- FS85_FS84_OTP_Config.xlsm
- Java installation <u>https://www.oracle.com/technetwork/java/javase/downloads/jre8-downloads-2133155.html</u>

4 Getting to know the hardware

The KITFS85SKTEVM provides flexibility to play with all the features of the device and make measurements on the main part of the application. The KL25Z MCU installed on the board, combined with the FlexGUI software allows access to the registers in read and write mode. All regulators are accessible through connectors. Nonuser signals, like DC/DC switcher node are mapped on test points. Digital signals (SPI, I2C, RSTb, etc.) are accessible through connectors. Wake1 pin has a switch to control (Ignition) them. A V_{BAT} switch is available to power On or Off the device.

The main purpose of this kit is to burn the OTP configuration. This kit can be operated in Emulation mode or in OTP mode. In Emulation mode, as long as the power is supplied, the board configuration stays valid. The OTP mode uses the fused configuration. The device can be fused three times. In OTP mode, the device always starts with the fused configuration, except if the user wants to overwrite OTP configuration using Emulation mode. This board is able to fuse the OTP without any extra tools or board.

Note: Due to the socket, this kit is not optimized for performance measurement or current higher than 1.0 A.

4.1 Kit overview

The KITFS85SKTEVM is a hardware evaluation tool that allows OTP burning. Due to the socket, the FS84/FS85 part can be configured without the need to solder it. Devices can be programmed three times (see <u>Section 7.3 "Programming the device with an OTP configuration"</u>).

An Emulation mode is possible to test as many configurations as needed.

An external LDO provides VDDI2C voltage with a choice of 1.8 V or 3.3 V (default). VDDIO is assigned by default to VDDI2C. From USB voltage, an external DC/DC

generates the OTP programming voltage (8.0 V) without any need for an external power supply.

4.1.1 KITFS85SKTEVM features

- VBAT power supply connectors (Jack and Phoenix)
- VPRE output capability up to 1.0 A (socket limit)
- VBUCK1/2 in Standalone (default) or Multiphase mode
- VBUCK3
- VBOOST 5.0 V or 5.74 V
- LDO1 and LDO2, from 1.1 V to 5.0 V
- · Ignition key switch
- FS0B external safety pin
- Embedded USB connection for easy connection to software GUI (access to SPI/I2C bus, IOs, RSTB, FS0B, INTB, Debug, MUX_OUT, regulators)
- · LEDs that indicate signal or regulator status
- · Support OTP fuse capabilities
- USB connection for register access, OTP emulation and programming
- Voltage monitoring jumper setting

Note: Due to the socket, all current capabilities are limited to 1.0 A.

4.1.2 VMON board configuration

The VMONx configuration is highly dependent on the use case. This kit is delivered with a default configuration shown in <u>Figure 2</u>.

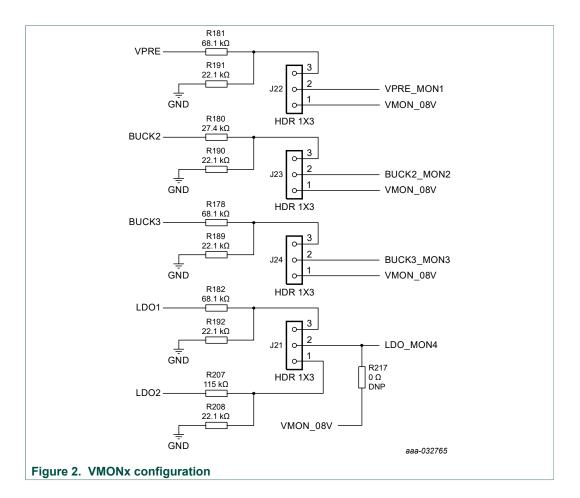
This configuration supports the following mapping:

- VPRE, assigned to VMON1; Bridge resistor set for 3.3 V
- BUCK2, assigned to VMON2; Bridge resistor set for 1.8 V
- BUCK3, assigned to VMON3; Bridge resistor set for 3.3 V
- LDO1, assigned to VMON4; Bridge resistor set for 3.3 V
- LDO2, assigned to VMON4; Bridge resistor set for 5.0 V

LDO1 and LDO2 use the same VMON, a reassignement is necessary to monitor both.

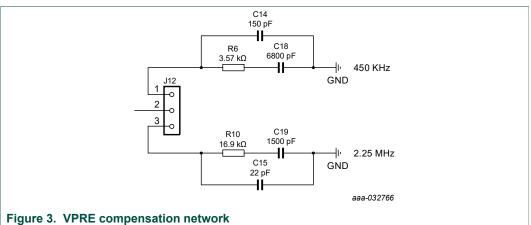
Due to the jumpers, VMONx can be tied to a 0.8 V to force a good voltage at pin level. This behaves like hardware disabling and makes debug easy in some cases.

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4.1.3 VPRE compensation network

This board is delivered with a VPRE compensation network defined for VPRE 4.1 V at 450 kHz. All other VPRE configurations require a new calculation for these components.

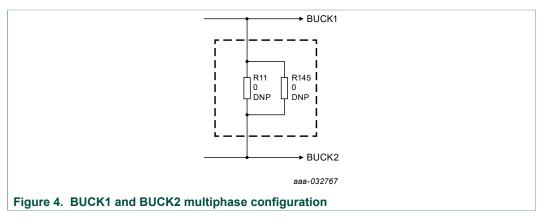


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Table 1. Compensation network			
Components	VPRE 450 kHz	VPRE 2.2 MHz	
C18/C19	6.8 nF	1.5 nF	
C14/C15	150 pF	22 pF	
R6/R10	3.57 kΩ	16.9 kΩ	
LPRE	4.7 μH or 6.8 μH	1.5 μH , 2.2 μH or 4.7 μH	

4.1.4 BUCK1 and BUCK2 multiphase configuration

The board is designed to work independently with BUCK1 and BUCK2. Due to R11 and R145, it is possible to connect both connectors together and work in multiphase.



4.1.5 SPI/I2C

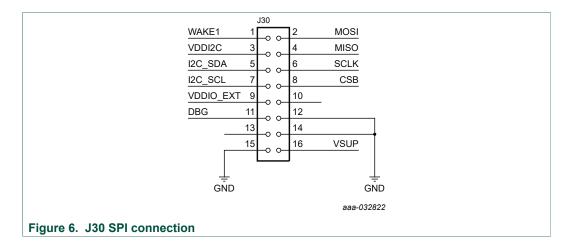
The SPI and I2C buses are connected to KL25Z MCU. The user can use either one or the other. The choice can be done at start of the FlexGUI or at any time after launch (see <u>Section 8 "Using FlexGUI"</u>).

This kit uses a KL25Z MCU to communicate with FlexGUI. However, if the user wants to connect the SPI to another MCU, this is possible. In this case, remove J28 and appropriate jumpers to disconnect the KL25Z MCU (see Figure 5) and connect the external MCU on J30 connector as shown in Figure 6. In addition to this change, make sure that the VDDIO voltage domain is the same on MCU side and SBC side.

		J28	
[3] R	зть 1	2	RSTb_SH
[3] FS	2	4	FS0b_SH
[3] M	5	6	MISO_SH
[3] M	7	8	MOSI_SH
[3] SC	0	10	SCLK_SH
[3] CS	11	12	CSB_SH
[0] 0.		ĽĽ	aaa-032768
Figure 5. SPI connection to KI	L25Z		

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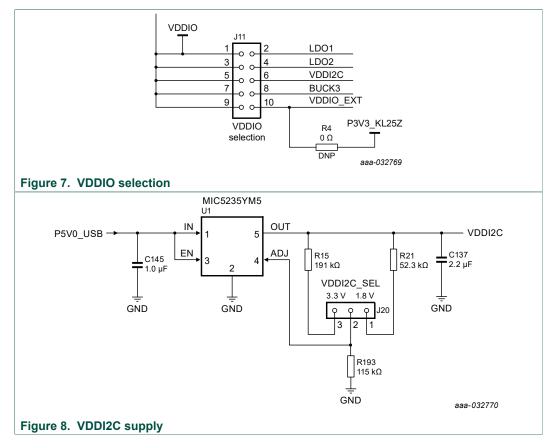
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4.1.6 VDDI2C

As an option, an external LDO is provided to feed VDDI2C. This LDO can also be used to feed VDDIO, which is the default implementation.

The I2C is compatible with 1.8 V or 3.3 V, while VDDIO is compatible with 3.3 V and 5.0 V. For this reason, the LDO default configuration is 3.3 V. The LDO is supplied by 5.0 V coming from the USB.



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4.2 Device OTP user configuration

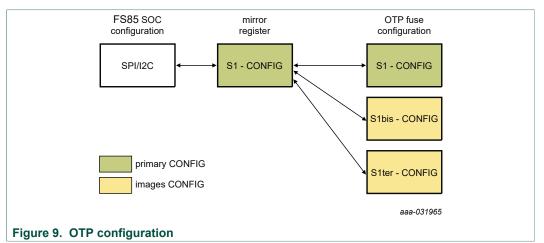
It is recommended to learn about OTP before operating with the device. The device has a high level of flexibility due to parameter configuration available in the OTP. This impacts the functionality of the device. It is key to understand how OTP parameters can be programmed, the interaction with mirror registers and the FS85 SoC.

The OTP related operations can be performed either in Emulation mode, where the product uses a given configuration as long as power supply is not switched Off or from OTP fuse content that is valid even after a power down/power up sequence.

4.2.1 OTP and mirrors registers

There are two OTP blocks in the device. One is for the main section, and the other for the fail-safe. During configuration, each of them are using dedicated sectors. The OTP configuration scheme is shown in Figure 9 (same implementation for main and fail-safe).

The device can be fused three times using mirror registers. The user can first load the mirror register content with the desired contents, then decide either to use the device in Emulation mode or to burn the next sector. The first sector to be burned is S1, the second S1bis and the third S1ter. FlexGUI automatically manages the next sector to be burned. It is not possible to revert back to the previous sector. When the user reaches the sector S1ter, there no other possibility for burn, however emulation mode is still available.



At boot, the content of the valid sector is loaded into the Mirror Register Sector 1. The mirror register content is accessible from FlexGUI by using specific SPI/I2C commands. The mirror configuration is managed by the FlexGUI, which eases the access.

4.2.2 OTP hardware implementation

To work in OTP emulation or OTP programming, it is required to start the device in Debug mode.

<u>Figure 10</u> shows the sequence to be followed to enter in Debug mode. The voltage sequence on the kit is done using switches installed on the board, while the OTP registers configuration is managed by the FlexGUI GUI. This is described in detail in the following sections.

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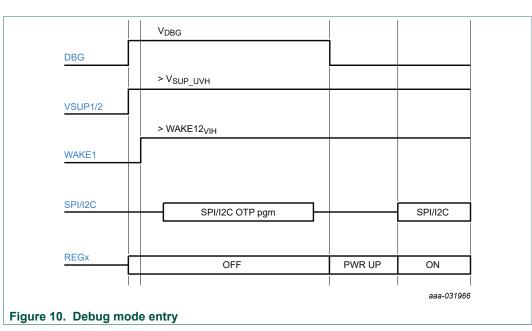
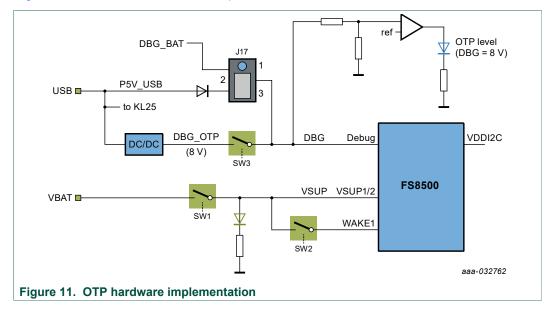


Figure 11 shows the hardware kit implementation.



4.3 Kit featured components

Figure 12 identifies important components on the board and <u>Table 2</u> provides additional details on these components.

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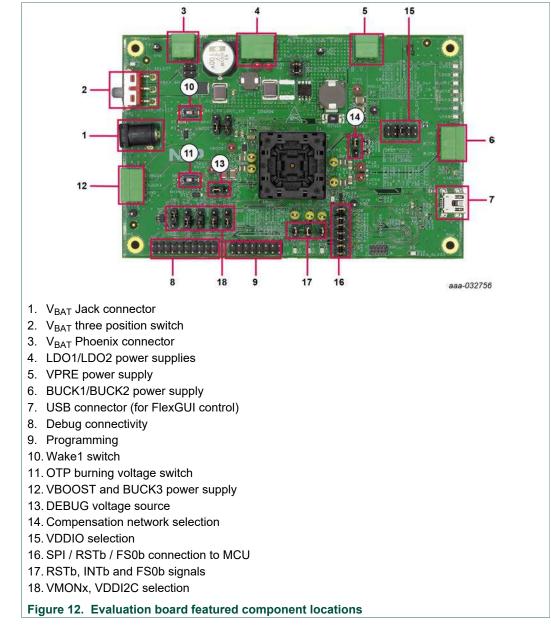


Table 2. Evaluation board board component descriptions

Number	Description
1	V _{BAT} Jack connector
2	 V_{BAT} three position switch Left position: board supplied by Jack connector Middle position: board not supplied Right position: board supplied by Phoenix connector
3	V _{BAT} Phoenix connector
4	LDO1/LDO2 power supply
5	VPRE power supply
6	BUCK1/BUCK2 power supply
7	USB connector (for FlexGUI control)

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Number	Description
8	Debug connectivity. Access to: • VSUP, GND • FOUT/FIN • PGOOD/RST/FS0b • FCCUx • Wake2 • PSYNC, ERRMON, AMUX • VMONx
9	Programming SPI bus I2C bus Debug pin VPRE, VSUP, GND
10	Wake1 switch
11	OTP burning voltage switch
12	VBOOST and BUCK3 power supply
13	DEBUG voltage source either from USB (recommended) or from VSUP
14	VPRE compensation network selection, either 2.2 MHz or 450 kHz
15	VDDIO source from device regulators or external sources
16	SPI, RSTb or FS0b can be disconnected between device and MCU
17	RSTb, INTb and FS0b signals available here (device pin level)
18	Allows to select VMON from regulators or a fix 0.8 V VDDI2C can be selected either 1.8 V or 3.3 V

4.3.1 FS8500/FS8400: Fail-safe system basis chip with multiple SMPS and LDO

4.3.1.1 General description

This device family is part of a global platform FS84 (fit for ASIL B) and FS85 (fit for ASIL D), pin to pin and software compatible. The FS85/FS84 is an automotive functionally safe multi-output power supply integrated circuit, with focus on Radar, Vision, ADAS domain controller, Radio and Infotainment applications. It includes multiple switch mode and linear voltage regulators. It offers external frequency synchronization input and output, for optimized system EMC performance.

The FS85/FS84 includes enhanced safety features, with fail-safe output, becoming a full part of a safety-oriented system partitioning, covering both ASIL B and ASIL D safety integrity level. It is developed in compliance with ISO 26262 standard. Several device versions are available, offering choice in number of output rails, output voltage setting, operating frequency and power up sequencing, to address multiple applications.

4.3.1.2 Features

- 60 V DC maximum input voltage for 12 V and 24 V applications
- VPRE synchronous buck controller with external MOSFETs. Configurable output voltage, switching frequency, and current capability up to 10 A peak.
- Low voltage integrated synchronous BUCK1 converter, dedicated to MCU core supply with SVS capability. Configurable output voltage and current capability up to 3.6 A peak.

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- **Based on part number:** low voltage integrated synchronous BUCK2 converter. Configurable output voltage and current capability up to 3.6 A peak. Multi-phase capability with BUCK1 to extend the current capability up to 7.2 A peak on a single rail. Static voltage scaling capability.
- **Based on part number**: low voltage integrated synchronous BUCK3 converter. Configurable output voltage and current capability up to 2.5 A typical peak.
- BOOST converter with integrated low-side switch. Configurable output voltage and max input current up to 1.5 A peak.
- EMC optimization techniques including SMPS frequency synchronization, spread spectrum, slew rate control, manual frequency tuning
- 2x linear voltage regulators for MCU IOs and ADC supply, external physical layer. Configurable output voltage and current capability up to 400 mA DC.
- Standby OFF mode with very low sleep current (10 µA typ)
- · 2x input pins for wake-up detection and battery voltage sensing
- Device control via 32 bits SPI or I2C interface with CRC
- Power synchronization pin to operate 2x FS85 devices or FS85 plus an external PMIC
- Scalable portfolio from ASIL B to ASIL D with independent monitoring circuitry, dedicated interface for MCU monitoring, simple and challenger watchdog function, power good, reset and interrupt, built-in self-test, fail-safe output
- Configuration by OTP programming. Prototype enablement to support custom setting during project development in engineering mode.

4.3.2 Indicators

The following LEDs are provided as visual output devices for the evaluation board:

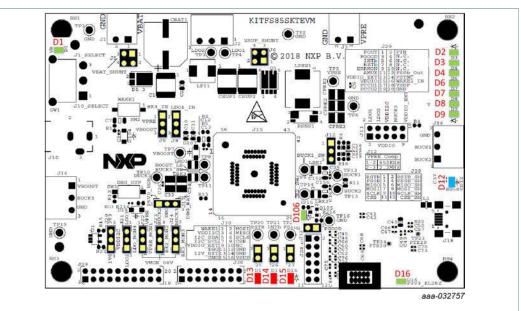


Figure 13. Evaluation board indicator locations

	heard indicator	

Table J.	Table 5. Evaluation board mulcator descriptions			
Label	Name	Color	Description	
D1	V _{BAT}	Green	V _{BAT} On	
D2	LDO1	Green	LDO1 On	
D3	LDO2	Green	LDO2 On	

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Label	Name	Color	Description
D4	BUCK1	Green	BUCK1 On
D6	BUCK2	Green	BUCK2 On
D7	BUCK3	Green	BUCK3 On
D8	VBOOST	Green	VBOOST On
D9	V _{PRE}	Green	V _{PRE} On
D12	DBG > 8.0 V	Blue	DBG pin voltage > 8.0 V (OTP programming)
D13	RSTb	Red	RSTb asserted (logic level = 0)
D14	INTb	Red	INTb asserted (logic level = 0)
D15	FS0b	Red	FS0b asserted (logic level = 0)
D16	P3V3_KL25	Green	P3V3_KL25 On
D106	PGOOD	Green	PGOOD released

4.3.3 Connectors

Figure 14 shows the location of connectors on the board.

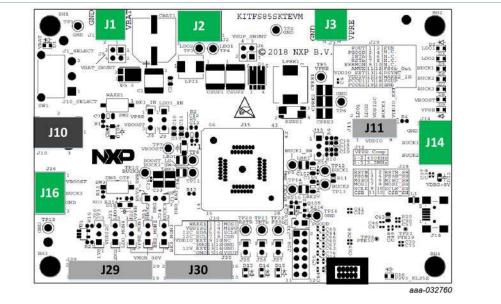


Figure 14. Evaluation board connector locations

4.3.3.1 V_{BAT} connector (J1)

VBAT connects to the board through Phoenix connector (J1).

Table 4. V_{BAT} Phoenix connector (J1)

Schematic label	Signal name	Description
J1-1	V _{BAT}	Battery voltage supply input
J1-2	GND	Ground

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4.3.3.2 Output power supply connectors

Table 5. BUCK1/BUCK2 connector (J14)

Schematic label	Signal name	Description
J14-1	BUCK2	BUCK2 power supply output
J14-2	BUCK1	BUCK1 power supply output
J14-3	GND	Ground

Table 6. VBOOST/BUCK3 connector (J16)

Schematic label	Signal name	Description
J16-1	VBOOST	VBOOST output
J16-2	BUCK3	BUCK3 power supply output
J16-3	GND	Ground

Table 7. LDO1/LDO2 connector (J2)

Schematic label	Signal name	Description
J2-1	LDO1	LDO1 power supply output
J2-2	LDO2	LDO2 power supply output
J2-3	GND	Ground

Table 8. VPRE connector (J3)

Schematic label	Signal name	Description
J3-1	VPRE	VPRE power supply output
J3-2	GND	Ground

4.3.3.3 Debug connector (J29)

Table 9. Debug connector (J29)

Schematic label	Signal name	Description
J29-1	FOUT	Frequency synchronization output
J29-2	FIN	Frequency synchronization input
J29-3	PGOOD	Power GOOD
J29-4	n.c.	not connected
J29-5	INTB	Interrupt, active low
J29-6	n.c.	not connected
J29-7	RSTb	Reset, active low
J29-8	n.c.	not connected
J29-9	ERRMON	Error monitoring
J29-10	n.c.	not connected
J29-11	AMUX	Analog multiplexer
J29-12	FS0b_Out	Fail-safe, active low
J29-13	VDDIO_EXT	VDDIO external reference

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Schematic label	Signal name	Description
J29-14	PSYNC	Power synchronization
J29-15	VDDIO	VDDIO used by FS85
J29-16	WAKE2_IN	Wake2 input
J29-17	FCCU1	Fault collector control unit 1
J29-18	VSUP	VSUP power supply
J29-19	FCCU2	Fault collector control unit 2
J29-20	GND	Ground

4.3.3.4 Program connector (J30)

Schematic label	Signal name	Description
J30-1	WAKE1	WAKE1 input
J30-2	MOSI	SPI master output slave input
J30-3	VDDI2C	VDDI2C voltage
J30-4	MISO	SPI master input slave output
J30-5	I2C_SDA	I2C serial data
J30-6	SCLK	SPI clock
J30-7	I2C_SCL	I2C serial clock
J30-8	CSB	SPI chip select
J30-9	n.c.	not connected
J30-10	VPRE	VPRE output
J30-11	DBG	Connected to Debug pin
J30-12	GND	Ground
J30-13	n.c.	not connected
J30-14	VSUP	Connected to VSUP pin
J30-15	GND	Ground
J30-16	GND	Ground

4.3.4 Test points

The following test points provide access to various signals to and from the board.

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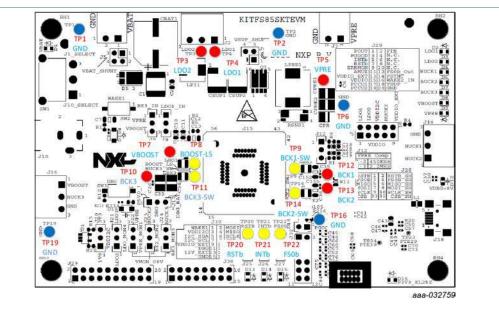


Figure 15. Evaluation board test points

Table 11. Evaluation board test point descriptions

Test point name	Signal name	Description
TP1	GND	Ground
TP2	GND	Ground
TP3	LDO2	LDO2 regulator output
TP4	LDO1	LDO1 regulator output
TP5	VPRE	VPRE DC/DC regulator output
TP6	GND	Ground
TP7	VBOOST	VBOOST DC/DC output
TP8	BOOST_LS	VBOOST low-side switcher
TP9	BUCK1_SW	BUCK1 switcher
TP10	BUCK3	BUCK3 DC/DC regulator output
TP11	BUCK3_SW	BUCK3 switcher
TP12	BUCK1	BUCK1 DC/DC regulator output
TP13	BUCK2	BUCK2 DC/DC regulator output
TP14	BUCK2_SW	BUCK2 switcher
TP16	GND	Ground
TP19	GND	Ground
TP20	RSTb	Reset
TP21	INTb	Interruption
TP22	FS0b	Fail-safe output

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4.3.5 Jumpers

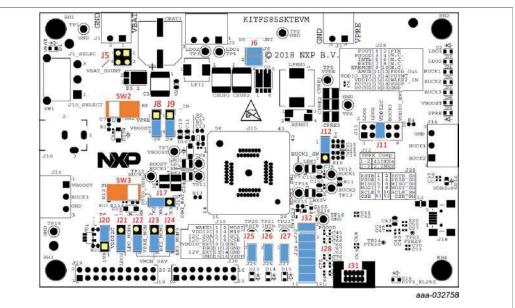


Figure 16. Evaluation board jumper locations

Table 12.	Evaluation	board	jumper	descri	ptions

Name	Function	Pin number	Jumper/pin function
J5	V _{BAT} shunt	1-2	Shunt switch SW1 for current > 5.0 A
12	V _{BAT} shuft	3-4	Shunt switch SW1 for current > 5.0 A
J6	V object	1-2	For current measurement (insert amperemeter)
30	V _{SUP} shunt	3-4	For current measurement (insert amperemeter)
J8	DLICK2 input	1-2	BUCK_INQ tied to VPRE
JO	BUCK3 input	2-3	BUCK_INQ tied to VBOOST
10	L DO1 input	1-2	LDO1_IN connected to V _{PRE}
J 9	LDO1 input	2-3	LDO1_IN connected to VBOOST
J10	V _{BAT} jack	Jack	Used for V _{BAT} supply using jack connector
		1-2	VDDIO tied to LDO1
		3-4	VDDIO tied to LDO2
J11	VDDIO selection	5-6	VDDIO tied to VDDI2C (provided by external regulators)
		7-8	VDDIO tied to BUCK3
		9-10	VDDIO tied to VDDIO external
147	Dahara	1-2	Debug pin tied to P5V0_USB (5.0 V provided by USB connector)
J17	Debug	2-3	Debug pin tied to V _{BAT} (through external protection) Do not use for OTP burning
120		1-2	VMON4 tied to LDO2
J20	VMON4	2-3	VMON4 tied to LDO1
100	V/040014	1-2	VMON1 tied to 0.8 V
J22	VMON1	2-3	VMON1 tied to VPRE

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Name	Function	Pin number	Jumper/pin function
J23	VMON2	1-2	VMON2 tied to 0.8 V
JZJ		2-3	VMON2 tied to BUCK2
J24	VMON3	1-2	VMON3 tied to 0.8 V
JZ4	VIVIOINS	2-3	VMON3 tied to BUCK3
J25	RSTb	1–2	Reset LED Enabled when jumper is plugged
J26	INTb	1–2	Interrupt LED Enabled when jumper is plugged
J27	FS0b	1–2	FS0b LED Enabled when jumper is plugged
J29	—	—	_
J30	-	—	
J31	-	_	Use only during board manufacturing
J32	PGOOD	1–2	PGOOD LED Enabled when jumper is plugged

4.3.6 Switches

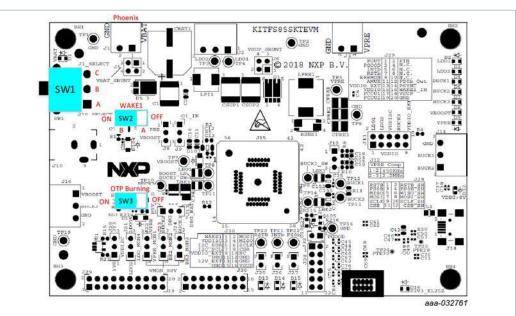


Figure 17. Switch locations

Table 13. SW3

Position	Function	Description
RIGHT	OTP programming Off	OTP burning not possible
LEFT	OTP programming On	8.0 V on DBG pin allows OTP burning (blue LED turns On to indicate this state)

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Table 14. SW2		
Position	Function	Description
OFF	WAKE1 open	Wake1 pin not connected to V_{SUP}
ON	WAKE1 closed	Wake1 pin connected to V_{SUP}

Table 15. SW1

Position	Function	Description
ТОР	VBAT On	VBAT from J1
MIDDLE	VBAT Off	Board not supplied
BOTTOM	VBAT On	VBAT from J10

4.4 Schematic, board layout and bill of materials

The schematic, board layout and bill of materials for the KITFS85SKTEVM evaluation board are available at http://www.nxp.com/KITFS85SKTEVM.

5 Installing and configuring software and tools

This development kit uses FlexGUI software. FlexGUI software is based on Java JRE.

Preparing the Windows PC workstation consists of three steps.

- 1. Install the appropriate Java SE Runtime Environment (JRE).
- 2. Install Windows 7 FlexGUI driver.
- 3. Install FlexGUI software package.

5.1 Installing the Java JRE

- Download Java JRE (Java SE Runtime Environment), available at <u>http://www.oracle.com/technetwork/java/javase/downloads/jre8-downloads-2133155.html</u> (8u162 or newer).
- 2. Open the installer and follow the installation instructions.
- 3. Following the successful installation, restart the computer.

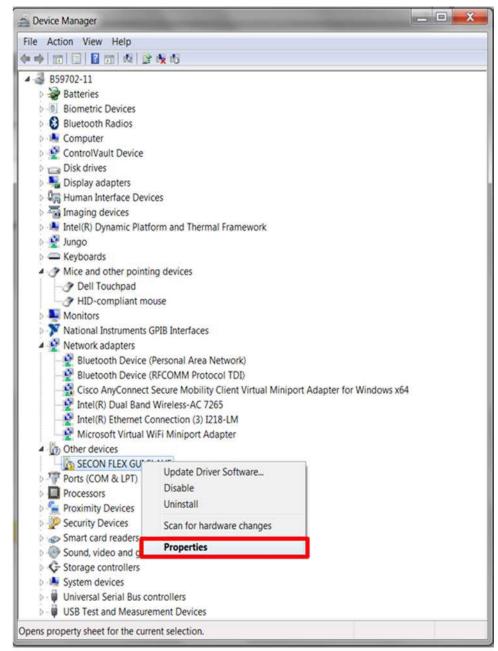
5.2 Installing Windows 7 FlexGUI driver

On Windows 7 PCs, a virtual COM port installation is required. Install the Windows 7 FlexGUI driver using the following procedure.

Note: On Windows 10, it is not necessary to install virtual com port as Windows 10 uses a generic COM port driver.

- 1. Connect the kit to the computer as described in <u>Section 6 "Configuring the hardware</u> <u>for startup"</u>
- 2. On the Windows PC, open the Device Manager.
- 3. In the **Device Manager** window, right-click on **SECON FLEX GUI SLAVE**, and then select **Properties**.

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4. In the SECON FLEX GUI SLAVE Properties window, click Update Driver.

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eneral	Driver Details	
1	SECON FLEX GU	JI SLAVE
	Device type:	Other devices
	Manufacturer.	Unknown
	Location:	Port_#0002.Hub_#0002
		e are not installed. (Code 28)
Ther	e is no driver select	
Ther	e is no driver select	ed for the device information set or element.
Ther	e is no driver select	ed for the device information set or element. evice, click Update Driver.

5. in the Update Software Driver window, select Browse my computer for driver software.

•	Search automatically for updated driver software Windows will search your computer and the Internet for the latest driver software for your device, unless you've disabled this feature in your device installation settings.	
+	Browse my computer for driver software Locate and install driver software manually.	

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- 6. Select Let me pick from a list of device drivers on my computer, and then click Next.

7. Select Ports (COM & LPT) from the list, and then click Next.

Select your device's type from the list below	Ν.
Common hardware types:	
Network Client	*
- Network Protocol	
Service	
Non-Plug and Play Drivers	
PCMCIA adapters	
Portable Devices	
Ports (COM & LPT)	
Reprinters	
Processors	=
Proximity Devices	(L
SBP2 IEEE 1394 Devices	
SD host adapters	
Security Devices	*

8. Click Have Disk.

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Select the manufacture	ou want to install for this hardware. rand model of your hardware device and then click Next. If you have river you want to install, click Have Disk.
Manufacturer	Model
(Standard port types) Brother Compaq GSM Radio Card	Gommunications Port ECP Printer Port Multiport Communications Port Printer Port
This driver is digitally signed	

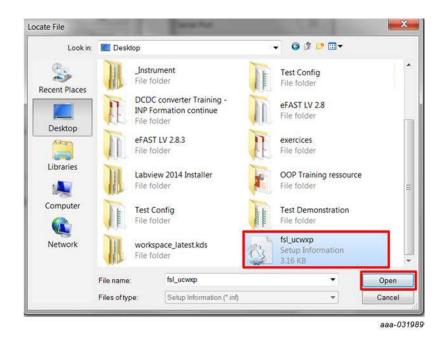
aaa-031987

9. Click Browse.

Install From	t the manufacturer and model of your hardware device a n Disk	nd then click Next. If
	Insert the manufacturer's installation disk, and then make sure that the correct drive is selected below.	OK Cancel
	Copy manufacturer's files from:	Browse
		Browse

10.In the Locate File window, locate and select fsl_ucwxp, and then click Open.

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11.In the Install from Disk window, click OK.

Insert the manufacturer's installation disk, and then make sure that the correct drive is selected below.	ОК
	Cancel
Copy manufacturer's files from:	
C:\Users\B59702\Desktop	Browse

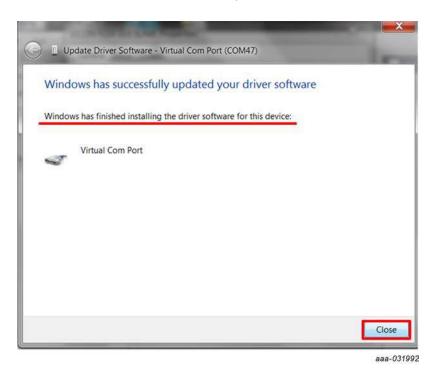
12.If prompted, in the **Windows Security** window, click **Select this driver software anyway**.

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13.Close the window when the installation is complete.



14.In the **Virtual Com Port Properties** window, verify that the device is working properly, and then click **Close**.

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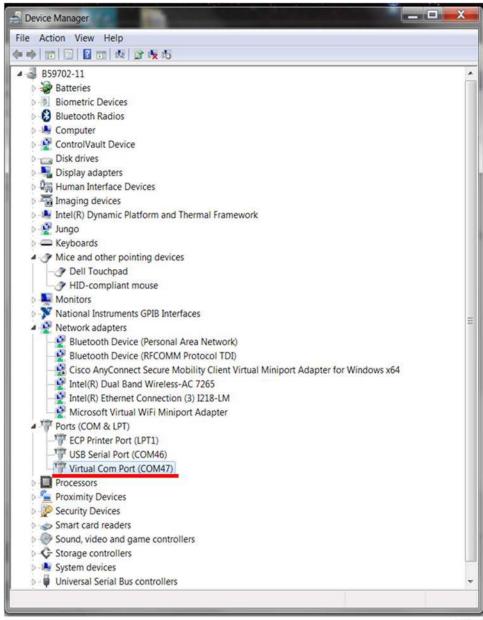
General	Driver Details		
1	Virtual Com Port ((COM47)	
	Device type:	Other devices	
	Manufacturer:	NXP	
	Location:	Port_#0002.Hub_#0002	
	e status device is working p	roperly.	*
		roperly.	*
		roperly.	*
		roperly.	•

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The Virtual Com Port appears in the Device Manager window.

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5.3 Installing FlexGUI software package

The FlexGUI software installation requires only extracting the zip file in a desired location.

- 1. If necessary, install the Java JRE and Windows 7 FlexGUI driver.
- 2. Download the latest FlexGUI (32-bit or 64-bit) version, available at http://www.nxp.com/KITFS85SKTEVM.
- Extract all the files to a desired location on your PC. FlexGUI is started by running the batch file, \bin\flexgui-app-fs85.bat.

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Figure 18. Typical initial configuration

6 Configuring the hardware for startup

Figure 18 presents a typical hardware configuration incorporating the development board, power supply and Windows PC workstation.

To configure the hardware and workstation as illustrated in <u>Figure 18</u>, complete the following procedure:

1. Install jumpers for the configuration.

Table 16. Jumper configuration						
Jumper	Configuration					
J17	connect 1-2 (connect 5.0 V on DBG pin from the USB)					

2. Configure switches for the configuration

Table 17. Switch configuration					
Switch	Configuration				
SW1	middle position (VBAT off)				
SW2	open (WAKE1)				
SW3	open (OTP programming off)				

 Connect the Windows PC USB port to the KITFS85SKTEVM development board using the provided USB 2.0 cable.
 Set the DC power supply to 12 V and current limit to 1.0 A. With power turned off,

attach the DC power supply to 12 v and current limit to 1.0 A. with power turned on, attach the DC power supply positive and negative output to KITFS85SKTEVM V_{BAT} Phoenix connector (J1).

- 4. Turn on the power supply.
- 5. Close SW2.

Note: At this step, the product is in debug mode and all regulators are turned off. The user can then power up with OTP configuration or configure the mirror registers before power up. Power up is effective as soon as J17 jumper is removed.

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7 Using the KITFS85SKTEVM evaluation board

This section summarizes the overall setup. Detailed description is provided in the following sections.

Before starting the process, choose the mode you want to run the device .

- In Normal mode, the configuration comes from OTP fuses.
- In Debug mode, you can either use the current configuration from OTP fuse, if any, or use the OTP emulation mode to write in the mirror register.

The Normal mode or Debug mode is defined at startup depending on the DBG pin level.

- Normal mode is set by tying DBG to ground
- Debug mode is set by setting DBG voltage to 5.0 V

In OTP emulation, you can overwrite the mirror registers from a given OTP fuse configuration. See <u>Section 4.2.1 "OTP and mirrors registers"</u> and <u>Section 8.3 "Working with the Script editor"</u> to define your configuration.

In OTP fuse configuration, use the configuration fused in the OTP. So, if a valid OTP fuse configuration exists, then it will be copied to the mirror registers at startup.

7.1 Generating the OTP configuration file

Define and generate your OTP configuration using the excel file *FS85_FS84_OTP_Config.xlsm*. This file allows configuring the device for parameters controlled by the the main state machine and the fail-safe state machine.

To generate the script:

1. Fill the OTP_conf_main_reg sheet

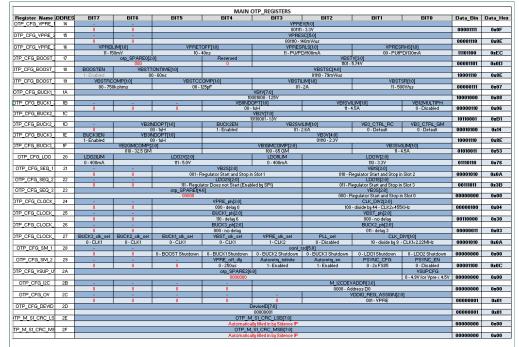


Figure 19. OTP_conf_main_reg spreadsheet example

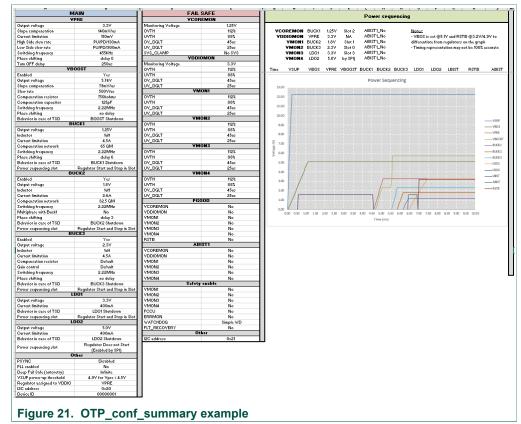
2. Fill the OTP_conf_failsafe_reg sheet

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				F	AIL-SAFE OTF	P_REGISTERS			10		
Register Name	ADDRESS	BIT7	BITO	BITS	BIT4	BIT3	8/12	8171	BITO	Data_Bin	Data_He
OTP_CFG_UVOV_1	0A				VCORE	V[7:0]					
	10000		10001000 - 1.25v							10001000	0.488
OTP_CEG_UVOV_2	OB		VDDIODVTH[3:0] VCOREOVTH[3:0]								
			1111	-112%				- 11256		11111111	OxFF
OTP OFG UVOV 3	0C			VDDI0_V			CORE SVS CLAMP[4:	0[Summer and	
- New Route Construction	1.1.1.1.1.1	0.	.0.	0-3.3V	3		00000 - No SVS	and an at		00000000	0000
OIP_CHG_UVUV_4	OD			OVTH[3:0]				2VTH[3:0]		Concernances -	
			1111-1128					112%		111111111	OxFF
OTP_CFG_UVOV_5	0E			OVTH[3:0]				DVTH[3:0]		Service events	10.00
	1977			State of the		5	1111			11111111	0xFF
OTP_CFS_UVOV_6	OF 2		VDDIOUVTH(310)				VCORFUVTH[3:0]				
			1111-88%				1111-88%			11111111	UndFF
OTP_CFG_UVOV_7	10			UVTH[3:0]		6		JVTH[3:0]		Second and the second	10000
0.0010200200000000000000000000000000000		1111-88%				2		-88%		111111111	OXFF
OIP CHG UVOV 8	11		VMON4UVTH[3:0]				VMON2UV1H[3:0]			11111111	
				1996			1111-489				ONEF
OTP_CFG_PGODD	12		PGOCO_RSTB	POODD_VMON4	PGOOD_VMCN3	PGOOD_VMON2	PGOOD_VMON1	PCCOD_VDDIQ	PGOOD_VCORE	in and the	1.22
		0	0 - Not assigned	0+Not exercised.	0 - Not excepted	0 - Not assigned	0 - Not assigned	0 - Not assigned	0 - Not assigned	00000000	0.000
OTP_CEG_ABIST1	13		pare[1:0]	ABIST1_VMON4	ABIST1_VMON3	ABIST1_VMON2	ABIS 1 VMON1	ABIST1_VDDIC	ABIST1_VCORE		
			00	0 Nut calgitos	0 fict assigned	0 Not assigned	0 Not assigned	0 - Not assigned	O Not assigned	00000000	0x00
OTP CFG ASIL	14	WD_DIS	WD_Selection	ERRMON_EN	FCCU_EN	VMDN4_EN	VMDN3_EN	VMON2_EN	VMCNI EN	Same marries to	61.03
		0 - Enabled	n timple WD	if Dicatiled	0 Ditableri	0 - Disound	0 Ditablet	0 - Disabled (ADDRI3:01	0-Disabled	00000000	0000
OTH CFG 12C	15		otp_spare1[2:0]		FLT RECOVERY EN						
	1	000 0 Disables 0000 Address D0				Procession and the second	00000000	0:00			
DTP_CFG_DGLT_DUR_1	16		ipane(1:0)		V_DGLT[1:0]	VCORE_OV_DGLT VDDID_UV_DGLT[1:0] VDDI0_OV_DGLT					2.22
		00 10 - 25ut				1 - 45at		75.s	1 - 45us	00101101	0x2D
DTP_CFG_DGLT_DUR_2	17			otp_spare[4:0]			VMCNx_U		VMONK OV DOLT		
				00000			10-	2505	1-45us	00000101	0x05
OTP TS S1 CRC LSB	18					CRC_USB[7:0]					
	-					ed in by Sidence IP				00000000	0:00
OTP PS SI CRC MSB	19					ORC_MSB(7:0)					0x00
					Automatically hik	ed in by Sidence III				00000000	0.600

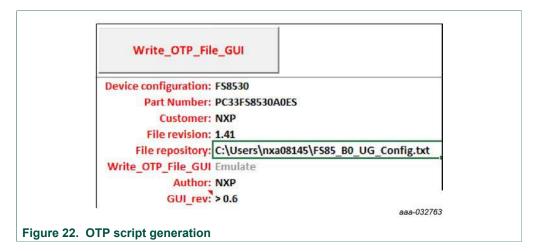
Figure 20. OTP_conf_failsafe_reg spreadsheet example

3. See the **OTP_conf_summary** sheet to review the complete configuration (main and fail-safe)



 Generate the script in OTP_conf_file_generation sheet Once the configuration is ready, the user can generate the script file. Go to OTP_conf_file_generation, enter the path in the File repository and then click Write_OTP_File_GUI.

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7.2 Working in OTP emulation mode

At startup, the device always uses the content from the mirror register. This content can come from OTP fuse or from configuration written directly in the mirror register. OTP emulation means that the user can emulate the OTP writing in the mirror register. This allows trials before burning the OTP.

- 1. Configure the hardware. See Section 6 "Configuring the hardware for startup".
- 2. Launch the FlexGUI software.
- 3. Switch to Debug mode:
 - a. Place SW1 in TOP direction (VBAT switched On).
 - b. Close SW2 (WAKE1).

While in Debug mode, all regulators are turned Off.

- 4. Load the mirror registers to work in OTP emulation mode. See <u>Section 8.3 "Working</u> with the <u>Script editor"</u>.
- 5. Unplug jumper J17 1-2 to start the device with the mirror configuration setting.
 - a. If the mirror registers are filled (with a configuration using the Script editor), that configuration will be used in the emulation session.
 - b. If the mirror registers are not filled (with a configuration using the Script editor), the currently-programmed OTP fuse configuration will be used, if it exists.
 - c. Otherwise, the mirror registers are not filled and the OTP fuse is not burned, and the device will not start up.

As long as initialization phase is not closed by a first good WD_Answer, the WD will not start and regulators will stay alive. Also, as long as Debug mode is not exited by writing FS_STATES:[DBG_EXIT] bit to 1, the FS0b pin cannot be released.

6. Use the FlexGUI software to evaluate the device configured. See <u>Section 8 "Using</u> <u>FlexGUI"</u>.

7.2.1 Example script: Closing initialization phase, disabling FCCU monitoring and releasing FS0b

The following script can be used to:

- Disable the WD (simple WD configuration is used here).
- Disable the FCCU monitoring.
 - On the hardware kit, the FCCU1 is pulled to GND and FCCU2 is pulled to VDDIO, which is detected as error phase by default. Disabling the FCCU by SPI/I2C avoids safety issue at startup.
- Close the initialization phase.
- Exit the Debug mode.
- Release FS0b pin. This is valid only if WD is activated in OTP. Seven good consecutive WD answers are required to have the FLT_ERR_CNTR back to 0. This is one of the conditions to allow FS0b release.

Table 18. FS85 starting sequence example

Step	Register name	Value	Description
1	FS_WD_WINDOW	0x0200	WDW_WINDOWS[3:0] = 0x0 => Watchdog disabled
2	FS_NOT_WD_WINDOW	0xF50F	NOT of FS_WD_WINDOW
3	FS_I_SAFE_INPUTS	0x51C6	FCCU_CFG[1:0] = 0x0 => 0x1 => Monitoring by pair FCCU12_FLT_POL[0] = 1 => FCCU1 or 2 = 0 is a fault
4	FS_I_NOT_SAFE_INPUTS	0xAC18	NOT of FS_I_SAFE_INPUTS
5	FS_WD_ANSWER	0x5AB2	1st good WD answer (for simple WD selection in OTP) Close the initialization phase
6	FS_STATES	0x4000	DBG_EXIT[0]=1 => Exit Debug mode
7	FS_WD_ANSWER	0x5AB2	2nd good WD answer
8	FS_WD_ANSWER	0x5AB2	3rd good WD answer
9	FS_WD_ANSWER	0x5AB2	4th good WD answer
10	FS_WD_ANSWER	0x5AB2	5th good WD answer
11	FS_WD_ANSWER	0x5AB2	6th good WD answer
12	FS_WD_ANSWER	0x5AB2	7th good WD answer
13	FS_RELEASE_FS0B	0xB2A5	FS0b pin released (pulled to high level)
14	MFLAG2	0x40F1	Clear flags VSUPUV7; VPREUVL, VSUPUVL, WAKE1FLG
15	FS_OVUVREG_STATUS	0x4550	Clear UV status flags

This sequence can be sent using a script built with FlexGUI. See <u>Section 8.3.2 "Script</u> <u>sequence files"</u>.

7.3 Programming the device with an OTP configuration

The device configuration can be changed three times (see <u>Section 4.2.1 "OTP and</u> <u>mirrors registers"</u>). The programming steps are exactly the same as the OTP emulation mode up to step 6.

Then, the user has to burn the part with FlexGUI. See <u>Section 8.4.8 "OTP programming</u>". Follow the instructions on the screen to proceed.

8 Using FlexGUI

To follow the steps in this section, make sure that the board is connected using the appropriate hardware configuration (see <u>Section 7.2 "Working in OTP emulation mode"</u>).

Note: It is recommended to use the latest version of FlexGUI.

8.1 Starting the FlexGUI application

After FlexGUI is launched with the *flexgui-app.bat* file, the FlexGUI launcher displays available kits.

Communication bus, SPI or I2C can be selected at this level. It is also possible to switch from one to the other using the communication tab from the main panel (see <u>Section 8.2</u> "Establishing the connection between FlexGUI and the hardware").

		×
Select a kit, device(s) and its fe	atures	
Kit and device(s)		
▼ FS85_KITs		
▼ FS85		
V BO		
FS85_with_KL25Z_board_inte	rface	
A kit for FS85 and FS84 evaluation	n.	
✓ Advanced settings		
Features		
debug-spi 👻	SPI or I2C bus selection	
Use this configuration and do	not ask again	
	OK	Cancel

When the configuration is selected, click **OK**.

8.2 Establishing the connection between FlexGUI and the hardware

The board must be connected to the USB before establishing a connection.

- Click Search to detect the COM port of the board.
- Click Start to enable the connection.

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COME - Seath State													
> 110	FSIS Sogradius												
		Measurements Internat/Dage Hill Earlie Dag Entry (OTE prog. Techtodologuenen Techtodologuenen Techtodologuenen Earlier) P(_MC_ANDERE_Entry exceedence exceedence exceedence exceedence exceedence exceedence exceedence exceedence exceedence											
Search Start	Report rap Functional Bask 0 -0x00,0x00+												15 Speed
COM Port Communication			WD,AVERDQ'AR	NO, AND HEADING	HC, AND HEARING	NO. MONIMPOSI	90,41949(110)	WE AND MERCER	INC, AND HERE S IS	ec.Arbentini	640: W	[1-1 PS_WD_AVENTK (0-10] [1-1 PS_OVUVRIG_STATUS (0-11)	
	Barel 1 =0x04,0x07+ Barel 2 =0x08,0x08+	PE, OVENIES, STATUS (SHE)	vorentradov.	VERMONAN	V000,0V	v(000,i/v	VIDILOV	WORLN	WORLDY	WENLW .		(-CPS_RELEASE_PSON (IN12)	
	Bark 3 +0x23.0x23+		VMDHE,DV	VARONALLY	WHENT,ON	WONDA	NUMAD	ILDIUM/JY	HLON, SHIT	REININAD	0.4000 (2)	D-175, SAVEJOS (D-13)	
	▼ Safety											1.1.1.1.1.1.1.1.1.1.1.1.1.1.1.1.1.1.1.1.	
	Baria D v0x00 0x0F+ Baria T +3x10, 0x13+	FS, RELEASE, FEDR (DV/C)	NUMPER	10.002/02/10	artypicantural	NUTRICIAL PROPERTY	server contact	WEAKS / SINCAR	49,2435,7509(19.0)	NUTROFAL	9		
	Bank 2 -0x14, 0x16-		REACTOR	45,0456,7508:1521	NULLASSI, PERSONAL	NUMBER PORTING	NELBASE, POINT 1943	RULASL/SMC103	REDAR FOR THE	NULAKE PURCH	1940 - ¥	T+) PS_WO_ANSWER (0x10)	
	 Write init safety 	PS SAFE IOL DATE	100000 0.40	Apoco Julivi	P4000.046	67,875	4012.042	4173,015	Alfa Jugot	ALTR. SIAS		(-EPS_DVDVR80_STATUS (5/11)	
	Bank 0 +5x01, 0x04> Bank 1 +5x05, 0x08>		- MARINA CONTRACT	FIGN.ORV	FORING	1506,0165	HUNC	ALLAND	PECULIFT		0.6402	(+) FEBERERE (100 (0+13)	
	Bark 2 +0x00,0x0C>			10110		113120255			100.00000		Parate No.	1-145,5440,05 (bit)	
User mode or Test mode selection		Select at Read											
48		PL/ND ANSWER SHITE	La company a	Tel, average and			Concernance of	Concernance of	()	-			
Nucle		PLAC ACCREADED	The part of the second s	NO.AMINOR/SID	A Contraction of the local		And the second second	Status of some first status		And in case of the second seco	Sector and		
eitch Node terr mode + Apply				and the second second				Contraction	And a second second	Concernation	ALL DO NO.		
erant Mode and-mode Auf		PS_DNU/REG_STATUS (Sv11)	VORMON, DV	VOORMONLAN	1000,07	Y000,W	Webia,bv	MONOV	WORLDY	VIENUV			
Carlo Status	Communication		webulay.	vvicitizi,vv	WENT, IN	UNDRUGY	10000	1555.80,0V	R.02.347	REARING	2-005 2		
they should v	Status	120200200200	-		(Internet in the second								
(P1	SPI or I2C Switch	PE, RELEASE, PERMISSION	and some starting in	NUMBER OF STREET									
a 94	Contraction and Statistics		arriver's stat. ro	arriver, special	and a second second	and and and and	derserf.stational	and an and a state of the	STOCK STOCK	Margin Condition	antes		
aud rates \$200000		PS_SAFE_KIS (DVTI)	P0000,0H8	10002_0VEVT	Approxim	07,979	84384/90	8039400	RENAME	APROVA			
			1016,002	1001010	NUMBER	100,016	FILE, REQ.	40,10,1116	*8549-40	REIR-SD	56 (1)		
FlexGUI to MCU Communication status		Select at	Clear										
		Shine status											
MOU Sume CONNECTED		The second		-			_		_				

<u>Figure 24</u> shows the mode selection. At first launch, the FlexGUI starts in User mode. The user can then decide to switch to Test mode using the Switch mode drop-down list followed by clicking **Apply**.

The **GUI-Device Status** field checks the connection from MCU to the device. The **ONLINE** status indicates a good connection, while **ERROR** status indicates an issue (e.g. V_{SUP} is not provided to the device).

The SPI/I2C communication bus can be changed at any time using the drop-down list. This change is managed by the onboard MCU to communicate with the desired bus.

It is also possible to change the clock frequency using this panel.

Note that in the case of I2C, most of the time, the default address used by the device are 0x20 for main and 0x21 for the fail-safe.

The I2C address is managed differently in Debug and Normal mode

- Debug mode :
 - I2C address when debug mode pin is set to 5.0 V are 0x20 for main and 0x21 for failsafe.
 - The user can change this address in the mirror register. The new address is taken into account only after debug pin is released to 0 V.
- · Normal mode:
- The address is burned in the OTP.

The user can read in which mode the device is operating. It is also possible to switch from user mode to test mode (and vice-versa).

The current mode is displayed only when Poll button is activated. If required, this has to be done at start up (Poll button is disabled by default). See <u>Figure 25</u>.

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FS85			
Mode Switch Mode: Current Mode:	user-mode user-mode	•	Apply
Figure 25. Disabling device mode po			eaa-032771

To move from one mode to the other, select the mode with switch mode drop-down button and click **Apply** to validate. At this time, the current mode will be updated at the condition that Poll button is enabled.

8.3 Working with the Script editor

The register and OTP emulation can be configured with the script editor. This is particularly useful to try various OTP configurations in Emulation mode.

The main subareas of this panel are:

- Send and receive command: displays a summary of commands sent and received from the device
- Command script editor: builds commands to be sent to the device
- Script text editor: sends a sequence of register configurations from a text file or from command edited directly in this area
- Script results: displays result status of each command sent to the device

8.3.1 Script text editor

Using Script editor, you can execute any command either directly or from a file. It is also possible to save and modify a script. Using the brush symbol, it is possible to clean windows if needed.

All commands have to follow a specific syntax. The Help menu describes commands available in the script editor and their syntax.

This help page describes commands available in the script editor and their format.

List of commands

- SET_REG: sets value of a selected register.
- READ_REG: reads value of a selected register.
- SET_DPIN: sets value of a selected digital pin.
- · GET_DPIN: gets value of a selected digital pin.
- · GET_APIN: gets value of a selected analog pin. Returned value is in mV.
- PAUSE: shows a dialog with user defined message. The script is paused until the user cofirms the dialog.
- EXIT: stops execution of the script.
- SET_MODE: sets device mode. List of modes depends on a device.

Command format

The following table describes command parameters. All paramaters are mandatory.

	lst parameter	2nd parameter	3rd parameter	4th parameter	5th parameter
SET_REG	Device	Reg. set	Reg. name / Reg. address	Reg. value	
GET_REG	Device	Reg. set	Reg. name / Reg. address		+
SET_DPIN	Device	Pin name	Dig. pin value	*	-
GET_DPIN	Device	Pin name	-	8	2
GET_APIN	Device	Pin name			-
PAUSE	Message	0.40			
EXIT	-		-		-

Description of command parameters mentioned in the table above:

- Device: device name (alias used in application).
- Reg. set: register set name. Register sets allows to associate registers which have similar function.
- Reg. name: register name as defined in datasheet.
- Reg. address: register address in decimal or hexadecimal (with 0x prefix) format.
- Reg. value: register value in decimal or hexadecimal (with 0x prefix) format.
- Pin name: name of digital or analog pin as defined in device datasheet.
- Dig. pin value: value of digital pin. Allowed strings are 'low' and 'high'.
- · Message: a message to be displayed in a dialog. It cannot contain '?' character, which is used as delimiter of
- parameters.Mode: name of a device mode.

Figure 27 shows an example to build a command from the panel.

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Device:	FS85	*	Commands:	
Digital pins			SET_REG:FS85:functional:M_REG	CTRL1:0x0800
Analog pins			Command Built	
▼ Registers				
Operation:	Write reg.	*		
Reg. set:	functional	*		
Reg. name/address:	M_REG_CTRL1	*		
Reg. value:	0×080d			
	d Command			aaa-032336

The value 0x0800 is sent to the register M_REG_CTRL1 (BUCK2DIS). The user can then send it to the device by clicking the arrow (see Figure 28).

	Send Script aaa-032337	
Figure 28. Send script	t	
	Commands:	
Einen 20. Onen et fan	// This command will disable // Regulator BUCK2 SET_REG:FS85:functional:M_REG_CTRL1:0x0800	
Figure 29. Correct for		
	Commands:	
	// This command will disable Regulator BUCK2 SET_REG:FS85:functional:M_REG_CTRL1:0x0800	
Figure 30. Wrong form	nat ("//" missing in second line)	

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8.3.2 Script sequence files

The Script editor allows the user to save script sequence files. A script sequence file is text file that contains a set of commands sent to the device in the order they are written, as shown in the following example.

```
// FS85_Release_FS0b
SET_REG:FS85:safety:FS_WD_WINDOW:0x0200
SET_REG:FS85:safety:FS_NOT_WD_WINDOW:0xF50F
SET_REG:FS85:Write_INIT_Safety:FS_I_SAFE_INPUTS:0x51C6
SET_REG:FS85:Write_INIT_Safety:FS_I_NOT_SAFE_INPUTS:AC18
SET_REG:FS85:safety:FS_WD_ANSWER:0x5AB2
```

Note: Comments can be added with a // prefix.

8.4 Understanding the FS85 workspace

The FS85 workspace consists of several tabs, each dedicated to a specific aspect of device functionality or configuration.

- · Register map
- Clocks
- · Regulators
- Measurements
- Interrupt flags
- · INIT safety
- Diag safety
- OTP programming
- TestMode:Sequencer
- TestMode:Mirrors_Main and TestMode:Mirrors_Failsafe

8.4.1 Register map

All SPI/I2C registers can be accessed in write and read mode using this tab.

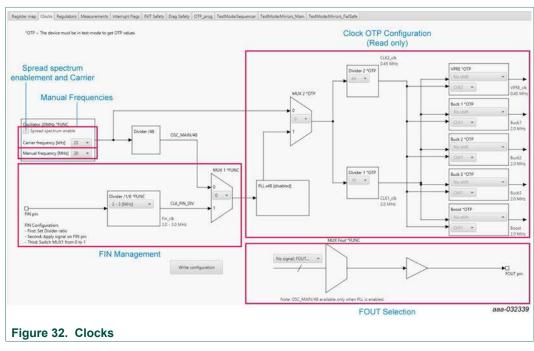
KITFS85SKTEVM evaluation board

tegister map	M_FLAG (0x00)	CON, SHA	WU,R	1998,2	V80057,6	VINCET	VBUCK2,6	VINCKLO	Y5001,6			Erpan
Functional Bank 0 +0x00 0x00+		V.002,5	NISERVED	RESERVED	PAMOR	SPLW, AND	SPUM, CRE	05,00,045	QE,M,ABQ	0.0	0	[+] M_FLAG [0x00]
Bank 0 +0x00, 0x01+ Bank 1 +0x04, 0x07+											1000	[+] M_MODE (567)
Bank 2 <0x08, 0x08>	M_MODE (SHD1)	AUGUST AD	10525192	46524942	RESERVED	RESERVED	RESERVED	CURRENT	PASOCIAT			(+) M_REG_CTRL1 (0x02)
Bank 3 +0x23,0x25+		07,44,86,47	AESERV52	MAIN, NORMAL	ALSERVIS2	ALSERVED	W2015	w105	RESERVED	0x0	12	(+) M,REG_CTRL2 (0x03)
Safety Bank 0 +0x00, 0x0F>											_ 1	
Bank 1 +0x10.0x13+	MURBOLCTRU1 (DNO2)	VPREPODIS	4638452	RESERVED.	NISERVED	ALSERVED.	ANSERVED.	RESERVED	Carvager		2.22	
Bank 2 +0x14, 0x18>		ADDIRUSE	ABURNEZ	AGUNY52	CEVINEERA	Alserved	RESERVED	ADDRAND .	RESERVED	040	199	(+) M_FLAG (0x00)
Write init safety	M.RSG-CTRL2 (0x03)	V857542-0	VESTARNE	00057750010	8000752016	BUDQTSDCH	8400750015	1001710010	LDOUTSDOVE			1-1 M_MODE (9401)
Bank 0 +0x01, 0x04+ Bank 1 +0x05, 0x08+	artistic court band								Austrophysical			(+) M,REG_CTRL3 (0x02)
Bank 2 +0x09, 0x00>		40547/10	4538/90	4658PV92	VMEALEUR	Aberthetikul	RESERVED	Asetherelati	Anatheologi	Joa	1997) 1997)	(+) M,REG,CTRL2 (0v03)
120/001	M FLAG ID4001	ADDENVED	4555455	ABSENITS	RESERVED	ALSONID	RESERVED	Asserved	RESORVED			Register Expension
											_	
I2C/SPI	M_FLAG [De00]											Register Expension
I2C/SPI Registers	MUTLAG (SHOO)	ADDAVED ADDAVED	453545 453545	ACLEVID ACLEVID	NESENIES SPLMLGA	852543 54,9,880	AUSERIALD SPLUICORC	Atserves GC.M.CRC	RESOLVED QC.M.REQ	0x0	-	Register Expension
	MUTURO (SHOO) MULMODE (SHOT)									010		Register Expension
		KERAND	103419-10	X0507140	SHALLA	\$21,0,620	SUNCOR	aculate	00,90,990	0+0		Register Expension
		ettianet ettianet	8(525-42) 8(534-42)	KESERVED RESERVED	SPLALOX ADQAVED	SPLOCARD ADDAVID	SPLULOR MISIPVID	aculos Assaulto	QC.M.NRQ MISURVED			Register Expension
and the second second second	M, MODE (5471)	4529-455 4529-455 4529-455	800640 800640 845,246,045	ASSENSO ASSENSO ASSENSO	SPUALOX NEONIO NEONIO	571,90,480 40387-40 40587-40	SPLICER NUSIFIED W2DS	acular NSINID WIDS	OC.NUND NISLAND GOTOLTHY			Register Expension
	M, MODE (5471)	10221020 10222020 10222020 10222020	RODINO RODINO DITUNIOS VPDS	4038440 4038440 4058450 8005705	SPLALOX NUMPLO NUMPLO NUMPLO BACKTOS	\$21,40,480 40,88440 40,56540 84,55295	SPLALOR MOLEVAD WODS BLACODS	ac.w.ckc MSERVED W105 L00105	OC.W.REQ RESERVED GOTOETRY LDG2D5	040		Register Expension
and the second second second	M, MODE (SHOT) M, RED, CTREY (SHOT)		4000400 4004400 611,916,05 9005 9005	NSERVED ALSERVED ALSERVED ALSERVED ALSERVED ALSERVED	SPLALEA NUMAD NUMAD NUMAD NUMAD NUMAD	PLU,RQ 400MD ASSMD BUCQDS BUCQDN	PLALOC ADDIVID W2D5 BUCODS BUCODY	OC.N.CRC MISIRVED W105 L00105 L00105	OC.N.RIQ ADDAVED GOTOETRY LDOCDS LDOCDS	040		Register Expension
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	M, MODE (SHOT) M, RED, CTREY (SHOT)	852040 453040 452640 452645 452645 452645	REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND	NSERVED AGAINES ASSERVED BOOLTONS BOOLTONS BOOLTONS	PUALAA NUDAHD NUDAHD NUCCTSI NUCCTSICS	PR, M, RIQ RESERVED RUCCEPS RUCCEPS RUCCEPS	91,94,092 48389485 94205 8460805 8460805 8460805 8460805	OCHURE NORMO WIDS LOOIDS LOOIDS	OC.N.RR RESIRVED GOTODITY LIDGERS LIDGERS	040		Register Expension
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	M, MODE (SHOT) M, RED, CTREY (SHOT)	RESEASE RESEASE RESEASE RESEASE RESEASE RESEASE RESEASE	REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND	X858440 455840 455840 3005755 3005751 8005751 8005751 8005751	PUALAA NUDAHD NUDAHD NUCCTSI NUCCTSICS	SPUMING ADDRIVED ADDRIVED ADDRIVED AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUCODIS AUC	91,94,092 48389485 94205 8460805 8460805 8460805 8460805	OCHURE NORMO WIDS LOOIDS LOOIDS	OC.N.RR RESIRVED GOTODITY LIDGERS LIDGERS	040		Register Expension
	M, MODE (SAFT) M, MOL, CTRLE (SAFT) M, MOL, CTRLE (SAFT)	RESERVED RESERVED RESERVED RESERVED RESERVED RESERVED RESERVED	REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND REEND 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Figure 31. Register map

- **Register map**: allows access to functional register, safety register and write init register which are accessible only during initialization phase
- Read: allows you to read any register either individually or by bank
- Write: allows you to write any register either individually or by bank
- **Register expansion**: displays the value of each device parameter

8.4.2 Clocks



This tab allows: OTP: • Read current OTP configuration (write operation is not possible). To display the accurate data, the device needs to operate in Test mode.

SPI/I2C:

- Configure the device to work with FIN input
- · Select the signal to apply on FOUT pin
- · Play with manual frequencies and spread spectrum

8.4.3 Regulators

The regulator has two main areas:

- · Low voltage (LV) regulators configuration
- VPRE compensation network calculation

Each regulator can either be enabled or disabled by SPI/I2C. The thermal shutdown behavior can be configured to either shutdown the regulator, or shutdown the regulator and transition to deep fail-safe. The write button applies to the entire table. The VPRE compensation network calculator helps to define the value for VPRE external compensation network.

					 -	
	LV Buck1			LV Buck2	VPRE [V]	
nable in normal mode			Enable in normal mode		VPRE ILIM [mV]	
isable in normal mode			Disable in normal mode			
ehavior in case of TSD	Regulator_Shutdown	*	Behavior in case of TSD	Regulator_Shutdown	Switching Frequency (KHz)	
					Rshunt [mOhm]	
	West States			CONVERT.	Cout [uF]	
nable in normal mode	LV Buck3	-	Enable in normal mode	LDO1	Lvpre [uH]	
Disable in normal mode			Disable in normal mode		 Rcomp [KOhm]	N/A
Sehavior in case of TSD	Regulator_Shutdown	*	Behavior in case of TSD	Regulator_Shutdown	 Ccomp [nF]	N/A
					 Chf [pF]	N/A
	LD02			VBOOST	Current limit [A] Slope compensation [mV/us]	N/A
Enable in normal mode			Enable in normal mode			
Disable in normal mode			Disable in normal mode		Calcula	te
Behavior in case of TSD	Regulator_Shutdown		Behavior in case of TSD	Regulator_Shutdown		
		1.00	lite			
			ine			

8.4.4 Measurements

This tab enables two features:

- Read any of the AMUX signals over time
- Display regulator voltage summary

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8.4.5 Interrupt flags

This tab allows you to set or clear flags. It is also possible to mask the interruption.

	Over/und	ler-voltag	je			Over-tem	perature	
	Status	Clear		Mask		Status	Clear	Mask
VSUP UVH		\checkmark		INT_not_masked	LDO1 shutdown			INT_not_maske
VSUP UVL		\checkmark		INT_not_masked	LDO2 shutdown			INT_not_maske
VSUP UV7		\checkmark		INT_not_masked	BUCK1 shutdown			INT_not_maske
VPRE UVH		\checkmark		INT_not_masked	BUCK2 shutdown			INT_not_maske
VPRE UVL		\checkmark		INT_not_masked	BUCK3 shutdown			INT_not_maske
VPRE FB_OV				INT_not_masked	VBOOST shutdown			INT_not_maske
VBOS UVH		\checkmark		INT_not_masked	BOS			INT_not_maske
VBOOST UVH		\checkmark		INT_not_masked		Write Re	ad Poll	
VBOOST OV				INT_not_masked		THILE INC		
		current Clear		Mask		Miscella Status		Mask
LDQ1		Clear	-		IDO1 ST			Mask
LDO1		Clear		INT_not_masked	LDO1 ST			Mask
LDO1 LDO2 BUCK1		Clear		INT_not_masked INT_not_masked	LDO1 ST LDO2 ST BUCK1 ST			Mask
LDO2		Clear		INT_not_masked	LDO2 ST			Mask
LDO2 BUCK1		Clear		INT_not_masked INT_not_masked INT_not_masked	LDO2 ST BUCK1 ST			Mask
LDO2 BUCK1 BUCK2		Clear		INT_not_masked INT_not_masked INT_not_masked INT_not_masked	LDO2 ST BUCK1 ST BUCK2 ST			Mask
LDO2 BUCK1 BUCK2 BUCK3		Clear		INT_not_masked INT_not_masked INT_not_masked INT_not_masked INT_not_masked	LDO2 ST BUCK1 ST BUCK2 ST BUCK3 ST			
LDO2 BUCK1 BUCK2 BUCK3 VBOOST	Status			INT_not_masked INT_not_masked INT_not_masked INT_not_masked INT_not_masked	LDO2 ST BUCK1 ST BUCK2 ST BUCK3 ST VBOOST ST		Clear	INT_not_maske
LDO2 BUCK1 BUCK2 BUCK3 VBOOST	Status			INT_not_masked INT_not_masked INT_not_masked INT_not_masked INT_not_masked	LDO2 ST BUCK1 ST BUCK2 ST BUCK3 ST VBOOST ST WK1 FLG		Clear	INT_not_maske
LDO2 BUCK1 BUCK2 BUCK3 VBOOST	Status			INT_not_masked INT_not_masked INT_not_masked INT_not_masked INT_not_masked	LDO2 ST BUCK1 ST BUCK2 ST BUCK3 ST VBOOST ST WK1 FLG WK2 FLG		Clear	INT_not_maske
LDO2 BUCK1 BUCK2 BUCK3 VBOOST	Status			INT_not_masked INT_not_masked INT_not_masked INT_not_masked INT_not_masked	LDO2 ST BUCK1 ST BUCK2 ST BUCK3 ST VBOOST ST WK1 FLG WK2 FLG WK1 RT	Status	Clear	INT_not_maske
LDO2 BUCK1 BUCK2 BUCK3 VBOOST	Status			INT_not_masked INT_not_masked INT_not_masked INT_not_masked INT_not_masked	LDO2 ST BUCK1 ST BUCK2 ST BUCK3 ST VBOOST ST WK1 FLG WK2 FLG WK1 RT	Status	Clear	Mask INT_not_maske INT_not_maske

8.4.6 INIT safety

This tab allows you to manage all registers that can be configured to close the initialization phase. Note that the initialization phase is closed by the first good watchdog refresh before 256 ms timeout.

	Fault impac		Watchdog handling	OV/UV Safe Reaction 1
Fault source	Settings		Error counters limit	VCore ABIST2 🔛 No_ABIST
COREMON_OV	FSOB_R. ·		WD_ERR_LIMIT 6 • 6	VDDIO ABIST2 🔛 No_ABIST
DDIO_OV	FSOB_R		WD_RFR_LIMIT 6 ~ 6	VMon1 ABIST2 No_ABIST
MON1_OV	FSOB_R., +		FLT_ERR_CNT_LIMIT 6 + 6	VMon2 ABIST2 No_ABIST VMon3 ABIST2 No_ABIST
MON2_OV	FSOB_R +			VMon4 ABIST2 No_ABIST
MON3_OV	F508_R		Write Road	Write Read
MON4_OV	FSOB_R *		Error counters value	(THE PARTY)
COREMON_UV	FSOB *		WD_ERR_CNT 0	
VDDIO_UV	FSOB -		WD_RFR_CNT 0	
/MON1_UV	FS08 ×		FLT_ERR_CNT 1	
/MON2_UV	FSOB *		Read	
VMON3_UV	FSOB *			
/MON4_UV	FSO8 ~			
CCU12	FSOB_R *			
CCU1	FSOB_R			
ccns	FSOB_R., *			
RRMON	FSOB_R., *			
VD ERR IMPACT	FS08_R			
LT_ERR_IMPACT	FSOB_R. ·			
mpact				
io impact				
	Write	ad		
	Safe Inputs		Miscellaneous	Static Voltage Scaling
CCU pin config	FCCU1_FCC *	FCCU1_FCCU2_pair	RST8 pulse duration 10ms + 10ms	Static voltage scaling External_reg_ * External_regulator
CCU12 polarity		FCCU1_L_FCCU2_H	Assert RSTB on PS08 short 😥 RESET_asserter	Write Read
CCU1 polarity	8	FCCU1_L	Disable clock monitoring II Monitoring_ac	tive transmission transmission
CCU2 polarity		FCCU2_L	Disable 85 timer Counter_enabl	led .
CCU1 polarity impact	2	FS0B_RSTB	Write Read	
RRMON polarity		Negative_edge	NUCLEAR ADDRESS	
RRMON timing config	8ms •	8ms		
	Write Rev	bd		
	Contraction of South			aaa-032

8.4.7 Diag safety

The watchdog type configured in the OTP has to be manually selected in the dropdown list to play with the watchdog features. If the user is not aware about the type of watchdog configured in the OTP, it can be found in TestMode:Mirrors_Failsafe and Miscellaneous tabs.

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Report PGOOD change	100000	Diag.	Safety	INTE	Mask
Leport PGOOD event	N/V	FCCU12 error	N/V	VMON4 OV/UV int. enable	N/V
	N/V	FCCU1 error	N/V	VMON3 OV/UV int. enable	N/V
vternal recet	N/V	FCCU2 error	N/V	VMON2 OV/UV int. enable	N/V
	N/V	ERRMON acknowledge		VMON1 OV/UV int. enable	N/V
ISTB driver	N/V	ERRMON input error	N/V	VDDIO OV/UV int. enable	N/V
STB sense	N/V	ERRMON input status	N/V	VCOREMON OV/UV int, enable	N/V
IST8 event	N/V	WD refresh status	N/V	WD refresh int, enable	N/V
STB diag	N/V	WD timing	N/V	ERRMON int, enable	N/V
RST8 request		SPI CLK status	N/V	FCCU2 int. enable	N/V
S08 driver	N/V	SPI access status	N/V	FCCU1 int, enable	N/V
SOB sense	N/V	SPI CRC status	N/V	Contraction designed	
S08 diag	N/V	I2C CRC status	N/V		
FS08 request	87.50	I2C access status	N/V		
Soto INIT fail-safe			-		
Write Read		Wolte	Read	Write	Read
Watchdog manageme	nt	OV/UV	status	Flags an	d Status
Watchdog Type Simple_WD	· •	VCOREMON OV	N/V	Communication error	N/V
		VCOREMON UV	N/V	WD refresh error	N/V
600d watchdog refresh WD A/	NSWER Good	VDDIO OV	N/V	IO error	N/V
ad watchdog refresh WD A	WSWER Bad	VU OIDOV	N/V	Voltage monitoring error	N/V
SOB release FSRELEASE	E FS08 Command	VMON4 OV	N/V	ABIST1 status	N/V
	The second second second second	VMON4 UV	N/V	ABIST2 status	N/V
S08 release script FS08 r	release script	VMON3 OV	N/V	LBIST_OK status	N/V
WD_ERR_CNT		VMON3 UV	N/V	Test Mode Activation Status	N/V
WD_RFR_CNT		VMON2 OV	N/V	Leave debug mode	
FLT_ERR_CNT		VMON2 UV	N/V	Debug mode	N/V
NDW PERIOD Disable	▼ N/V	VMON1 OV		OTP bit corruption	N/V
		VMON1 UV	N/V	INIT register corruption	N/V
NDW_DC (Duty Cycle) 31.25	* N/V	FS DIG REF OV	N/V	Fail-safe machine state	N/V
VDW_RECOVERY Disable	• N/V	FS OSC DRIFT	N/V		
Write Read		Write	Read	Write	Read
TALINE DEGN		THOSE	INCOM.	TITLE	nees.

The FS_Release_FS0b command calculates and sends the right secure16-bit word to release FS0b.

A simplified way to release FS0b after power up is to, first, select the right type of watchdog configured in the OTP, then, hit FS0b Release script button. This sends the right sequence to close the initialization sequence, sets the error counter back to 0, then releases FS0b.

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8.4.8 **OTP** programming

This tab allows you to burn the OTP using a script generated by the excel file OTP configuration (see <u>Section 7.1 "Generating the OTP configuration file "</u>).



Figure 38. OTP burning

To set up the hardware before OTP burning, see <u>Section 7.3 "Programming the device</u> with an OTP configuration".

See Figure 38 and follow the steps:

- Browse and load the script file you want to burn. The program button will then be available.
- Click Program.

FlexGUI pops up to turn the 8.0 V On, and then turns Off. Note that the blue LED on the board indicates that an 8.0 V voltage is available on the Debug pin. This voltage is used only during the burning process, and should not be applied in any other configuration. At the end of the first OTP programming, the MTP index = 1, WP, BE and CRC flags are green.

The Sector Flags area provides status <u>Table 19</u> provides the state of main flags after a read. This helps to determine how many times the part was burned.

OTP burning step	BE	WP	CRC	MTP Index
OTP not burn Mirrors Empty	Red	Red	Red	1
OTP not Burn Mirrors Filled	Red	Red	Green	1
1	Green	Green	Green	1
2	Green	Green	Green	2
3	Green	Green	Green	3

Table 19. OTP burning flag status

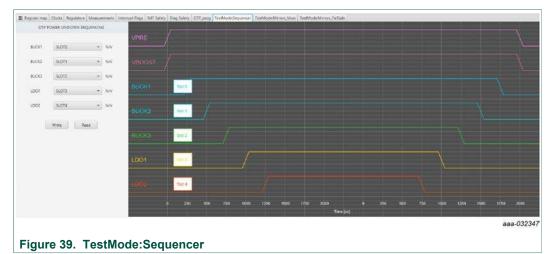
Example shown in Figure <u>38</u> corresponds to the OTP burning step 2 from <u>Table 19</u>.

To check if a valid OTP configuration is already burned, switch V_{BAT} Off, then On, and start the device. The device starts with the OTP configuration.

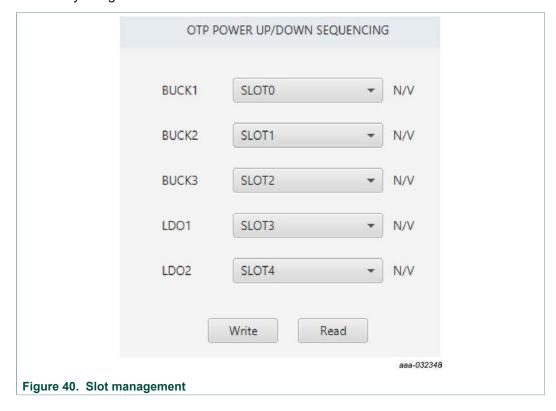
8.4.9 TestMode:Sequencer

The sequencer allows you to display the slot configuration for the device. To be able to access this tab, the device has to be in Test mode. The configuration is read from mirror register. It is possible to modify it and update the mirror register.

As an example, the slot sequence is filled at start up with the content of OTP fuses. Then the user can decide to modify any of the configurations coming from the OTP fuse. Note that all these actions are done with Debug pin at 5.0 V and in test mode.



Use the drop-down button (see <u>Figure 40</u>) to select the appropriate slot. The selection configuration can be sent to the device by clicking Write button. The current status can be read by using Read button.



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8.4.10 TestMode:Mirrors_Main and TestMode:Mirrors_Failsafe

The TestModeMirrors_Main and TestModeMirrors_FailSafe tabs allow access to the OTP main mirrors and fail-safe registers. These tabs are available in Test mode.

	VPRE			BOOST			LDOs	
utput voltage avenut imitation threshold on Sub silve rate control of Sub silve rate control off Sub severate control PRE phase (deling) selection with the UTE FVRF at device po PRE deck selection	3.3V 70mV/us 150mV 900mA 900mA NoDesay	 JJV 70mV/us 150mV 900mA 900mA 900mA NoDelay 250us CLK_DIV2 	VBD057 path to VB05 Output softage B0057 enable B0057 interimoun ON time VB0057 slope compensation Compensation Network Resistor - Compensation Network Resistor VB0057 current limitation VB0057 Low Side slew rate contr B0057 sloke adetation B0057 sloke adetation	Enabled 5.74V Enabled 60% 125mV/un 125mV/un 125pF 2A 0 500V/un NoDelay CUC,DV1	 Enabled S.74V Enabled Billis 125mV/us 750Cohm 125pF 2A S00V/us NoDelay CLK_DIV1 * Regulator, 	LDO1 sequencing slot Regulator behavior in case o	100x 400mA 5007 5009 5009 80guilto: Shuktown 400mA 1337 50x3 Regulato: Shuktown	 400mÅ 5.0V 5.0V Stot4 Repulstor.Shu 400mÅ 3.3V Stot3 Repulstor_Shu
80	re Read		6	write Read			wite Read	
	BROOT			8602		0	BUOG	
BUCK1 output voltage	1.025V ·	1.029V	VBUCK2 output voltage	1.250V	* 1,250V	V8UCK3 output voltage	2.30V	* 2.50V
UCK1 inductor selection	full -	:1uH	BUCK2 inductor selection.	foH	· 10H	BUCK3 enable	Enabled	* Enabled
BUCKI current limitation	4.54	4.5A	BUCK2 enable	Enabled	* Enabled	BUCK3 inductor selection	TuH	+ 16B
BUCKI & VBUCK2 multiphase o	Disabled •	Disabled	VBUCK2 current limitation	4.5A	* 4.5A	V8UCICI current limitation	4.5A	* 45A
UCKI Compensation Network	65GM ·	65GM	BUCK2 compensation network	695M	* 65GM	BUCK3 compensation resistor	Default	* Default
UCK1 sequencing slot	Slot0	Slot0	BUCK2 sequencing slot	Slotő	· Slot6	BUCK3 gain control	Default	· Default
UCK1 phase (delay) selection	NoDelay ·	NoDelay	BUCK2 phase (delay) selection	NoDelay	· NoDelay	BUCK3 sequencing slot	Slot2	- Slot2
UCK1 dock selection	CUK, DIV1	CLK, DIV1	BUCK2 clock selection	CUK_DIV1	· CLK_DIV1	BUCK3 phase (delay) selection	NoDelay	+ NoDelay
egulator behavior in case of TSD	Regulator_Shutdo	Regulator_Sh.	Regulator behavior in case o	Regulator_Shutdown	· Regulator, SP	ut. BUCK3 clock selection	CUK_DIV1	. CLK_DIVI
	re Read		6	erite Reed		Regulator behavior in case o	Regulator, Shuldown	Regulator_Shu
	CLOCK			SM			VSUP UV/OV	
U. exeble	Disabled - Disable	d	Deep fail-safe infinite autoretry e	nable Enabled	* Enable	VSUP Under Voltage Threshold	Configura 4.9V	+ 4.9V
kvider 1 setting	Divide9 + Divide9		Deep Fail-safe autoretry enable	Enabled	• Enable	Regulator assigned to VDDIO (OV) ExtRegOpti	. · ExtRegOp
ivider 2 setting	Divide44 + Divide4	4	Synchronization with 1x FS85 or 1	x PF82 2xF\$85	+ 25585			
			Synchronization with 2 devices	Disabled	+ Disable	d		
			Device I2C address	00	- 00			
14,7	Read		6	write Read			mite Read	
							2001 D	

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V	IONI		v	MON2		V7	MON3	
Overvoltage threshold [%]	112	* 112	Overvoltage threshold [%]	112 -	112	Overvoltage threshold [%]	112 *	112
Overvoltage Filtering Timing [us]	45	 45 	Overvoltage Filtering Timing [us]	45 *	45	Overvoltage Filtering Timing [us]	45 *	45
Undervoltage threshold [%]	68	- 88	Undervoltage threshold (%)	88 +	88	Undervoltage threshold [%]	88 *	88
Undervoltage Filtering Timing [us]	25	× 25	Undervoltage Filtering Timing [us]	25 *	25	Undervoltage Filtering Timing (us)	25 *	25
Assignment to PGOOD		Not_Assigned	Assignment to PGOOD		Not_Assigned	Assignment to PGOOD		Not_Assigned
Assignment to ABIST1		Not_Assigned	Assignment to ABIST1	编	Not_Assigned	Assignment to ABIST1		Not_Assigned
Monitoring		Disabled	Monitoring	60	Disabled	Monitoring	(B)	Disabled
write	Read		write	Read		write	Read	
v	4014			70010			CORE	
Overvoltage threshold [%]	112	• 112	Overvoltage threshold [%]	112 *	112	Overvoltage threshold (BUCK1) [%]	112 *	112
Overvoltage Filtering Timing [us]	45	* 45	Overvoltage Filtering Timing (us)	45 *	45	Overvoltage Filtering Timing [us]	45 ×	45
Undervoltage threshold [%]	88	* 88	Undervoltage threshold [%]	88 *	88	Undervoltage threshold (%)	\$8 *	88
Undervoltage Filtering Timing [us]	25	* 25	Undervoltage Filtering Timing [us]	25 *	25	Undervoltage Filtering Timing [us]	25 -	25
Assignment to PGOOD		Not_Assigned	Assignment to PGOOD		Not_Assigned	Assignment to PGOOD		Not_Assigne
Assignment to ABIST1	- 60	Not_Assigned	Assignment to ABIST1		Not_Assigned	Assignment to ABIST1	(II)	Not Assigned
Monitoring		Disabled	Voltage selection	3.3V -	3.3V	Monitoring voltage (VBUCK1)	1.25V *	1.25V
write	Read		write	Read		write	Read	
		Miscel	anedus					
SVS max value allowed NoSVS		SVS RST8 assign	ment to PGOOD	Not Assigned				
	101 I I I I I I I I I I I I I I I I I I	abled Watchdog e		 Simple_WD 				
		abled FCCU monit		Disabled				
Fault recovery strategy	Dis	abled Device I2C a	ddress D0	* 00				
		write	Read					

Figure 42. TestMode: Mirrors_FailSafe

The Read button provides the current status. The Write button changes the configuration in mirror register. This can be useful, for example, to modify few parameters from OTP fuse to start up the board.

9 References

- [1] **KITFS85SKTEVM** detailed information on this board, including documentation, downloads, and software and tools <u>http://www.nxp.com/KITFS85SKTEVM</u>
- [2] FS8500 product information on FS8500, Safety system basis chip for S32 microcontrollers, fit for ASIL D http://www.nxp.com/FS8500
- [3] FS8400 product information on FS8400, Safety system basis chip for S32 microcontroller, fit for ASIL B <u>http://www.nxp.com/FS8400</u>
- [4] FS85_FS84_OTP_Config.xlsm OTP configuration file

10 Revision history

Revision history

Rev	Date	Description
v.2	20190220	 Global: reorganized content to match latest template <u>Section 4.3.5</u>: updated <u>Table 12</u> <u>Section 6</u>: updated the configuration procedure <u>Section 8.4.7</u>: updated <u>Figure 37</u> <u>Section 8.4.9</u>: updated <u>Figure 39</u> and <u>Figure 40</u> <u>Section 8.4.10</u>: updated <u>Figure 41</u>
v.1	20190118	Initial version

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