

74ALVT16373

16-bit transparent D-type latch; 3-state

Rev. 5 — 14 July 2021

Product data sheet

1. General description

The 74ALVT16373 is a 16-bit D-type transparent latch with 3-state outputs. The device can be used as two 8-bit transparent latches or a single 16-bit transparent latch. The device features two latch enables (1LE and 2LE) and two output enables (1OE and 2OE), each controlling 8-bits. When nLE is HIGH, data at the inputs enter the latches. In this condition the latches are transparent, a latch output will change each time its corresponding D-input changes. When nLE is LOW the latches store the information that was present at the inputs a set-up time preceding the HIGH-to-LOW transition of nLE. A HIGH on nOE causes the outputs to assume a high-impedance OFF-state. Operation of the nOE input does not affect the state of the latches. Bus hold data inputs eliminate the need for external pull-up resistors to define unused inputs

2. Features and benefits

- Wide supply voltage range from 2.3 to 3.6 V
- Overvoltage tolerant inputs to 5.5 V
- BiCMOS high speed and output drive
- 16-bit transparent latch
- 5 V I/O compatible
- 3-state buffers
- Output capability: +64 mA/-32 mA
- Direct interface with TTL levels
- Input and output interface capability to systems at 5 V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power-up reset
- Power-up 3-State
- No bus current loading when output is tied to 5 V bus
- I_{OFF} circuitry provides partial Power-down mode operation
- Latch-up performance exceeds 500 mA per JESD 78 Class II Level B
- ESD protection:
 - MIL STD 883 method 3015: exceeds 2000 V
 - MM exceeds 200 V
- Specified from -40 °C to 85 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74ALVT16373DGG	-40 °C to +85 °C	TSSOP48	plastic thin shrink small outline package; 48 leads; body width 6.1 mm	SOT362-1

4. Functional diagram

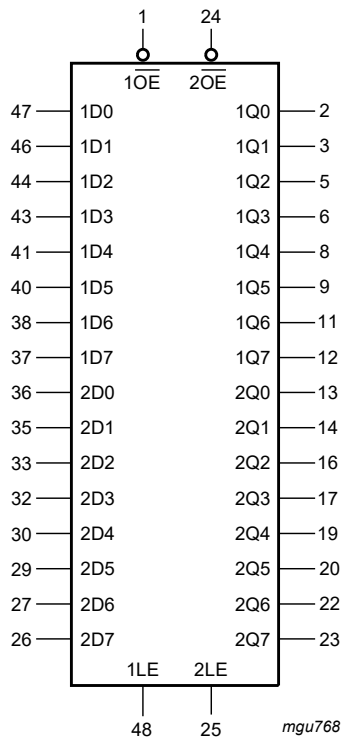


Fig. 1. Logic symbol

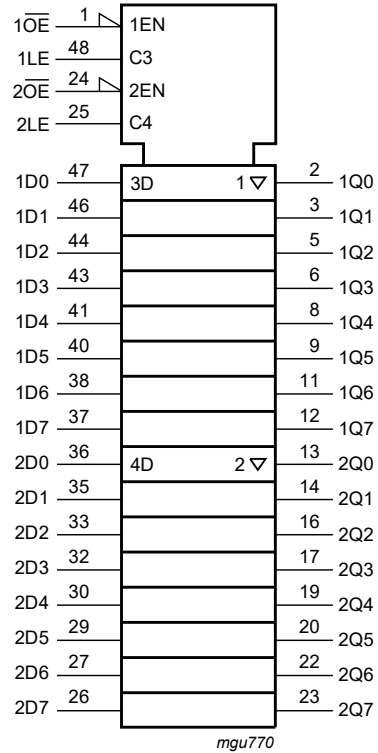


Fig. 2. IEC logic symbol

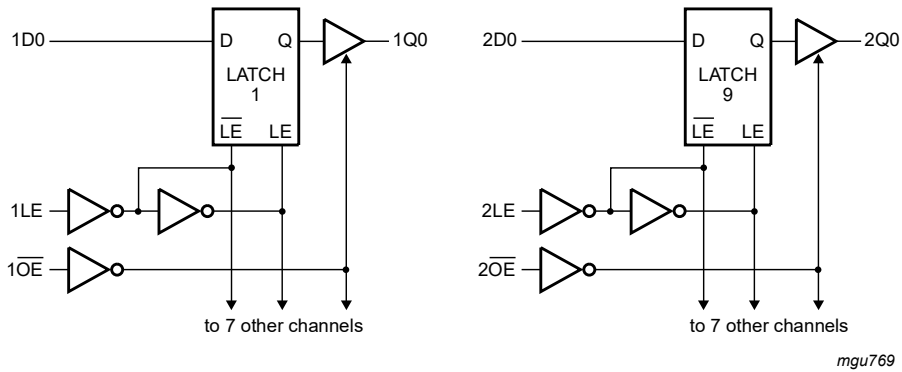


Fig. 3. Logic diagram

5. Pinning information

5.1. Pinning

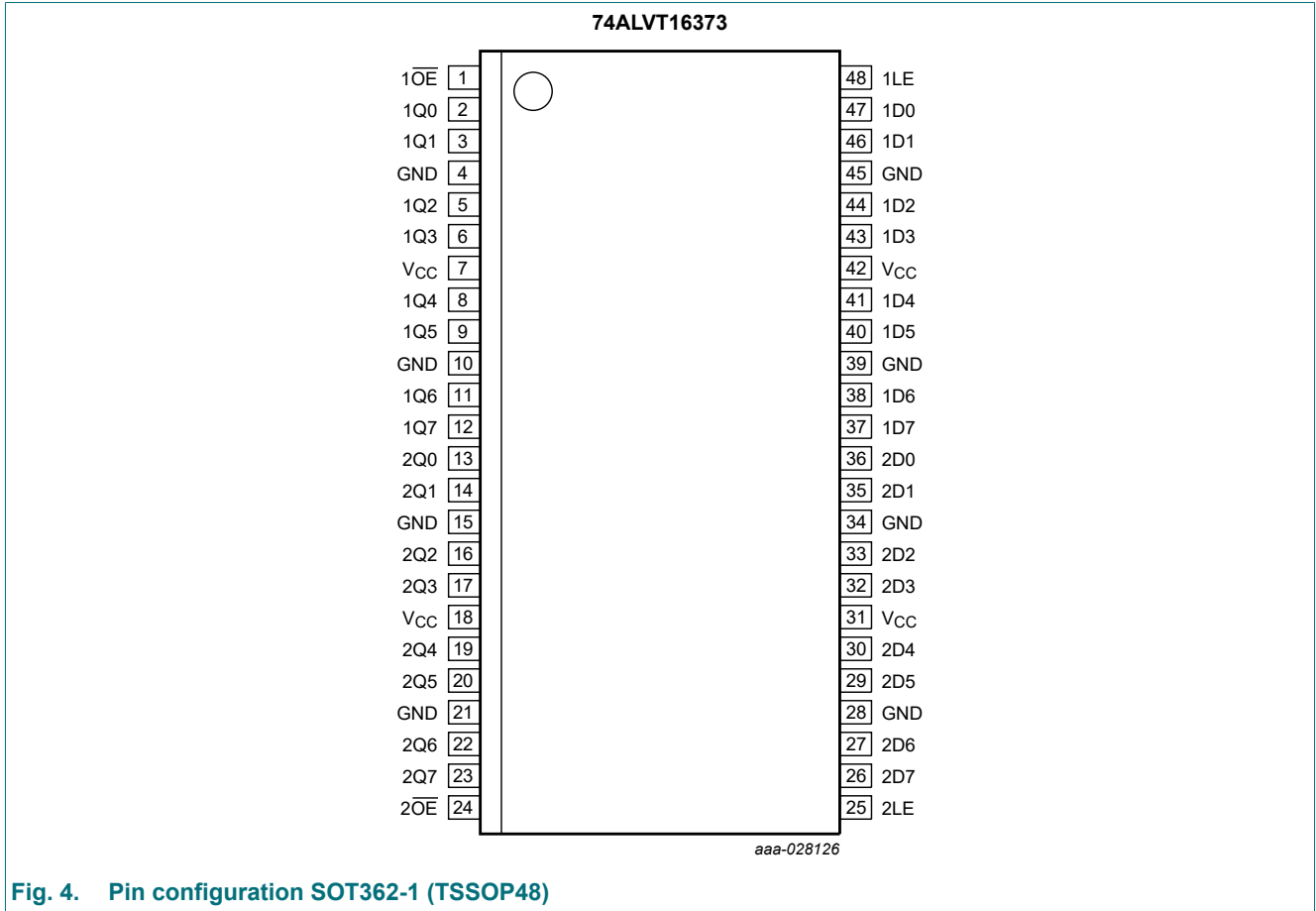


Fig. 4. Pin configuration SOT362-1 (TSSOP48)

5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1D0, 1D1, 1D2, 1D3, 1D4, 1D5, 1D6, 1D7	47, 46, 44, 43, 41, 40, 38, 37	data inputs
2D0, 2D1, 2D2, 2D3, 2D4, 2D5, 2D6, 2D7	36, 35, 33, 32, 30, 29, 27, 26	data inputs
1Q0, 1Q1, 1Q2, 1Q3, 1Q4, 1Q5, 1Q6, 1Q7	2, 3, 5, 6, 8, 9, 11, 12	data outputs
2Q0, 2Q1, 2Q2, 2Q3, 2Q4, 2Q5, 2Q6, 2Q7	13, 14, 16, 17, 19, 20, 22, 23	data outputs
1 \overline{OE} , 2 \overline{OE}	1, 24	output enable inputs (active LOW)
1LE, 2LE	48, 25	latch enable inputs (active HIGH)
GND	4, 10, 15, 21, 28, 34, 39, 45	ground (0 V)
V _{CC}	7, 18, 31, 42	supply voltage

6. Functional description

Table 3. Function table

H = HIGH voltage level; h = HIGH voltage level one set-up time prior to the HIGH-to-LOW LE transition;

L = LOW voltage level; l = LOW voltage level one set-up time prior to the HIGH-to-LOW LE transition;

↓ = HIGH-to-LOW LE transition;

X = don't care; NC = No change; Z = high-impedance OFF-state.

Operating mode	Inputs			Internal latches	Outputs nQn
	nOE	nLE	nDn		
enable and read register (transparent mode)	L	H	L	L	L
	L	H	H	H	H
latch and read register	L	↓	l	L	L
	L	↓	h	H	H
Hold	L	L	X	NC	NC
Latch register and disable outputs	H	L	X	NC	Z
	H	H	nDn	nDn	Z

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+4.6	V
V _I	input voltage	[1]	-0.5	+7.0	V
V _O	output voltage	output in OFF-state or HIGH-state [1]	-0.5	+7.0	V
I _{IK}	input clamping current	V _I < 0 V	-50	-	mA
I _{OK}	output clamping current	V _O < 0 V	-50	-	mA
I _O	output current	output in LOW-state	-	128	mA
		output in HIGH-state	-64	-	mA
T _{stg}	storage temperature		-65	+150	°C
T _j	junction temperature	[2]	-	+150	°C

[1] The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	$V_{CC} = 2.5 V \pm 0.2 V$		$V_{CC} = 3.3 V \pm 0.3 V$		Unit
			Min	Max	Min	Max	
V_{CC}	supply voltage		2.3	2.7	3.0	3.6	V
V_I	input voltage		0	5.5	0	5.5	V
I_{OH}	HIGH-level output current		-	-8	-	-32	mA
I_{OL}	LOW-level output current	none	-	8	-	32	mA
		current duty cycle $\leq 50\%$; $f_i \geq 1$ kHz	-	24	-	64	mA
$\Delta t/\Delta V$	input transition rise and fall rate	outputs enabled	-	10	-	10	ns/V
T_{amb}	ambient temperature	free-air	-40	+85	-40	+85	$^{\circ}C$

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; $T_{amb} = -40^{\circ}C$ to $+85^{\circ}C$; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
$V_{CC} = 2.5 V \pm 0.2 V$						
V_{IK}	input clamping voltage	$V_{CC} = 2.3 V$; $I_{IK} = -18$ mA	-	-0.85	-1.2	V
V_{IH}	HIGH-level input voltage		1.7	-	-	V
V_{IL}	LOW-level input voltage		-	-	0.7	V
V_{OH}	HIGH-level output voltage	$V_{CC} = 2.3 V$ to $2.7 V$; $I_O = -100$ μA	$V_{CC} - 0.2$	-	-	V
		$V_{CC} = 2.3 V$; $I_O = -8$ mA	1.8	-	-	V
V_{OL}	LOW-level output voltage	$V_{CC} = 2.3 V$; $I_O = 100$ μA	-	0.07	0.2	V
		$V_{CC} = 2.3 V$; $I_O = 24$ mA	-	0.3	0.5	V
$V_{OL(pu)}$	power-up LOW-level output voltage	$V_{CC} = 2.7 V$; $I_O = 1$ mA; $V_I = V_{CC}$ or GND [2]	-	-	0.55	V
I_I	input leakage current	all input pins [3]				
		$V_{CC} = 0 V$ or $2.7 V$; $V_I = 5.5 V$	-	0.1	10	μA
		control pins				
		$V_{CC} = 2.7 V$; $V_I = V_{CC}$ or GND	-	0.1	± 1	μA
		data pins; [3]				
		$V_{CC} = 2.7 V$; $V_I = V_{CC}$	-	0.1	1	μA
		$V_{CC} = 2.7 V$; $V_I = 0 V$	-	0.1	-5	μA
I_{OFF}	power-off leakage current	$V_{CC} = 0 V$; V_I or $V_O = 0 V$ to $4.5 V$	-	0.1	± 100	μA
I_{BHL}	bus hold LOW current	data inputs; $V_{CC} = 2.3 V$; $V_I = 0.7 V$ [4]	-	90	-	μA
I_{BHH}	bus hold HIGH current	data inputs; $V_{CC} = 2.3 V$; $V_I = 1.7 V$ [4]	-	-10	-	μA
I_{EX}	external current	output in HIGH-state when $V_O > V_{CC}$; $V_O = 5.5 V$; $V_{CC} = 2.3 V$	-	10	125	μA
$I_{O(pu/pd)}$	power-up/power-down output current	$V_{CC} \leq 1.2 V$; $V_O = 0.5 V$ to V_{CC} ; $V_I = GND$ or V_{CC} ; $n\overline{OE} = \text{don't care}$ [5]	-	1	100	μA

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
I _{OZ}	OFF-state output current	V _{CC} = 2.7 V; V _I = V _{IL} or V _{IH}				
		output HIGH: V _O = 2.3V	-	0.5	5	μA
		output LOW: V _O = 0.5 V	-	0.5	-5	μA
I _{CC}	supply current	V _{CC} = 2.7 V; V _I = GND or V _{CC} ; I _O = 0 A				
		outputs HIGH	-	0.04	0.1	mA
		outputs LOW	-	2.3	4.5	mA
		outputs disabled [6]	-	0.04	0.1	mA
ΔI _{CC}	additional supply current	per input pin; V _{CC} = 2.3 V to 2.7 V; one input at V _{CC} - 0.6 V; other inputs at V _{CC} or GND [7]	-	0.04	0.4	mA
C _I	input capacitance	V _I = 0 V or V _{CC}	-	3	-	pF
C _O	output capacitance	Outputs disabled; V _O = 0 V or 3 V	-	9	-	pF
V_{CC} = 3.3 V ± 0.3 V						
V _{IK}	input clamping voltage	V _{CC} = 3.0 V; I _{IK} = -18 mA	-	-0.85	-1.2	V
V _{IH}	HIGH-level input voltage		2.0	-	-	V
V _{IL}	LOW-level input voltage		-	-	0.8	V
V _{OH}	HIGH-level output voltage	V _{CC} = 3.3 V ± 0.3 V; I _O = -100 μA	V _{CC} - 0.2	V _{CC}	-	V
		V _{CC} = 3.0 V; I _O = -32 mA	2.0	2.3	-	V
V _{OL}	LOW-level output voltage	V _{CC} = 3.0 V; I _O = 100 μA	-	0.07	0.2	V
		V _{CC} = 3.0 V; I _O = 16 mA	-	0.25	0.4	V
		V _{CC} = 3.0 V; I _O = 32 mA	-	0.3	0.5	V
		V _{CC} = 3.0 V; I _O = 64 mA	-	0.4	0.55	V
V _{OL(pu)}	power-up LOW-level output voltage	V _{CC} = 3.6 V; I _O = 1 mA; V _I = V _{CC} or GND [2]	-	-	0.55	V
I _I	input leakage current	all input pins [3]				
		V _{CC} = 0 V or 3.6 V; V _I = 5.5 V	-	0.1	10	μA
		control pins				
		V _{CC} = 3.6 V; V _I = V _{CC} or GND	-	0.1	±1	μA
		data pins [3]				
		V _{CC} = 3.6 V; V _I = V _{CC}	-	0.5	1	μA
		V _{CC} = 3.6 V; V _I = 0 V	-	0.1	-5	μA
I _{OFF}	power-off leakage current	V _{CC} = 0 V; V _I or V _O = 0 V to 4.5 V	-	0.1	±100	μA
I _{BHL}	bus hold LOW current	data inputs; V _{CC} = 3 V; V _I = 0.8 V	75	130	-	μA
I _{BHH}	bus hold HIGH current	data inputs; V _{CC} = 3 V; V _I = 2.0 V	-75	-140	-	μA
I _{BHLO}	bus hold LOW overdrive current	data inputs; V _{CC} = 3.6 V; V _I = 0 V to 3.6 V [8]	500	-	-	μA
I _{BHHO}	bus hold HIGH overdrive current	data inputs; V _{CC} = 3.6 V; V _I = 0 V to 3.6 V [8]	-500	-	-	μA
I _{EX}	external current	output in HIGH-state when V _O > V _{CC} ; V _O = 5.5 V; V _{CC} = 3.0 V	-	10	125	μA
I _{O(pu/pd)}	power-up/power-down output current	V _{CC} ≤ 1.2 V; V _O = 0.5 V to V _{CC} ; V _I = GND or V _{CC} ; nOE = don't care [9]	-	1	±100	μA
I _{OZ}	OFF-state output current	V _{CC} = 3.6 V; V _I = V _{IL} or V _{IH}				
		output HIGH: V _O = 3.0V	-	0.5	5	μA
		output LOW: V _O = 0.5 V	-	0.5	-5	μA

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
I_{CC}	supply current	$V_{CC} = 3.6\text{ V}$; $V_I = \text{GND}$ or V_{CC} ; $I_O = 0\text{ A}$				
		outputs HIGH	-	0.04	0.1	mA
		outputs LOW	-	3.5	5	mA
		outputs disabled [6]	-	0.05	0.1	mA
ΔI_{CC}	additional supply current	per input pin; $V_{CC} = 3\text{ V}$ to 3.6 V ; one input at $V_{CC} - 0.6\text{ V}$; other inputs at V_{CC} or GND [7]	-	0.04	0.4	mA
C_I	input capacitance	$V_I = 0\text{ V}$ or V_{CC}	-	3	-	pF
C_O	output capacitance	output disabled; $V_O = 0\text{ V}$ or 3 V	-	9	-	pF

- [1] All typical values for $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ are measured at $V_{CC} = 2.5\text{ V}$ and $T_{amb} = 25\text{ }^\circ\text{C}$.
All typical values for $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ are measured at $V_{CC} = 3.3\text{ V}$ and $T_{amb} = 25\text{ }^\circ\text{C}$.
- [2] For valid test results, data must not be loaded into the latches after applying power.
- [3] Unused pins at V_{CC} or GND.
- [4] Not guaranteed.
- [5] This parameter is valid for any V_{CC} between 0 V and 1.2 V with a transition time of up to 10 ms .
From $V_{CC} = 1.2\text{ V}$ to $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ a transition time of $100\text{ }\mu\text{s}$ is permitted. This parameter is valid for $T_{amb} = 25\text{ }^\circ\text{C}$ only.
- [6] I_{CC} with outputs disabled is measured with outputs pulled to V_{CC} or GND.
- [7] This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND.
- [8] This is the bus hold overdrive current required to force the input to the opposite logic state.
- [9] This parameter is valid for any V_{CC} between 0 V and 1.2 V with a transition time of up to 10 ms .
From $V_{CC} = 1.2\text{ V}$ to $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ a transition time of $100\text{ }\mu\text{s}$ is permitted. This parameter is valid for $T_{amb} = 25\text{ }^\circ\text{C}$ only.

10. Dynamic characteristics

Table 7. Dynamic characteristics

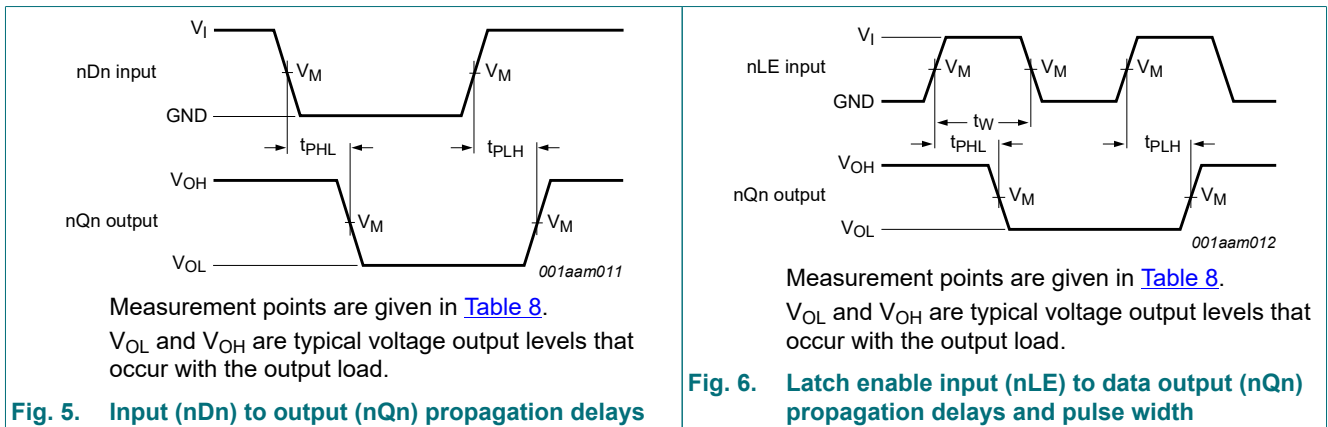
At recommended operating conditions; $T_{amb} = -40\text{ }^\circ\text{C}$ to $+85\text{ }^\circ\text{C}$; voltages are referenced to GND (ground = 0 V);
for test circuit see Fig. 9.

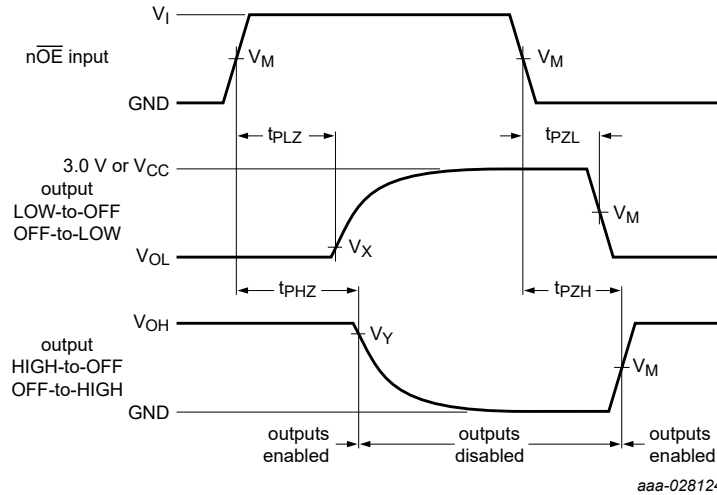
Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$						
t_{PLH}	LOW to HIGH propagation delay	nDn to nQn; see Fig. 5	1.0	2.0	3.2	ns
t_{PHL}	HIGH to LOW propagation delay	nDn to nQn; see Fig. 5	1.0	2.4	4.2	ns
t_{PLH}	LOW to HIGH propagation delay	nLE to nQn; see Fig. 6	1.5	2.6	4.2	ns
t_{PHL}	HIGH to LOW propagation delay	nLE to nQn; see Fig. 6	1.5	2.8	4.5	ns
t_{PZH}	OFF-state to HIGH propagation delay	\overline{nOE} to nQn; see Fig. 7	2.0	3.5	5.5	ns
t_{PZL}	OFF-state to LOW propagation delay	\overline{nOE} to nQn; see Fig. 7	1.5	2.6	4.7	ns
t_{PHZ}	HIGH to OFF-state propagation delay	\overline{nOE} to nQn; see Fig. 7	1.5	2.7	4.5	ns
t_{PLZ}	LOW to OFF-state propagation delay	\overline{nOE} to nQn; see Fig. 7	1.0	2.0	3.5	ns
$t_{su(H)}$	set-up time HIGH	nDn to nLE; see Fig. 8	0	-0.7	-	ns
$t_{su(L)}$	set-up time LOW	nDn to nLE; see Fig. 8	1.5	0.2	-	ns
$t_{h(H)}$	hold time HIGH	nDn to nLE; see Fig. 8	0.5	-0.2	-	ns
$t_{h(L)}$	hold time LOW	nDn to nLE; see Fig. 8	1.5	0.7	-	ns
t_{WH}	pulse width HIGH	nLE; see Fig. 6	1.5	-	-	ns

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
V_{CC} = 3.3 V ± 0.3 V						
t _{PLH}	LOW to HIGH propagation delay	nDn to nQn; see Fig. 5	0.5	1.6	2.5	ns
t _{PHL}	HIGH to LOW propagation delay	nDn to nQn; see Fig. 5	0.5	1.8	2.9	ns
t _{PLH}	LOW to HIGH propagation delay	nLE to nQn; see Fig. 6	1.0	2.0	3.1	ns
t _{PHL}	HIGH to LOW propagation delay	nLE to nQn; see Fig. 6	1.0	2.3	3.3	ns
t _{PZH}	OFF-state to HIGH propagation delay	n \overline{OE} to nQn; see Fig. 7	1.5	2.3	4.0	ns
t _{PZL}	OFF-state to LOW propagation delay	n \overline{OE} to nQn; see Fig. 7	1.0	1.9	3.1	ns
t _{PHZ}	HIGH to OFF-state propagation delay	n \overline{OE} to nQn; see Fig. 7	1.5	2.9	4.5	ns
t _{PLZ}	LOW to OFF-state propagation delay	n \overline{OE} to nQn; see Fig. 7	1.5	2.3	3.7	ns
t _{su(H)}	set-up time HIGH	nDn to nLE; see Fig. 8	0.5	-0.2	-	ns
t _{su(L)}	set-up time LOW	nDn to nLE; see Fig. 8	0.8	0.2	-	ns
t _{h(H)}	hold time HIGH	nDn to nLE; see Fig. 8	0.8	0	-	ns
t _{h(L)}	hold time LOW	nDn to nLE; see Fig. 8	1.0	0.2	-	ns
t _{WH}	pulse width HIGH	nLE; see Fig. 6	1.5	-	-	ns

[1] All typical values for V_{CC} = 2.5 V ± 0.2 V are measured at V_{CC} = 2.5 V and T_{amb} = 25 °C.
 All typical values for V_{CC} = 3.3 V ± 0.3 V are measured at V_{CC} = 3.3 V and T_{amb} = 25 °C.

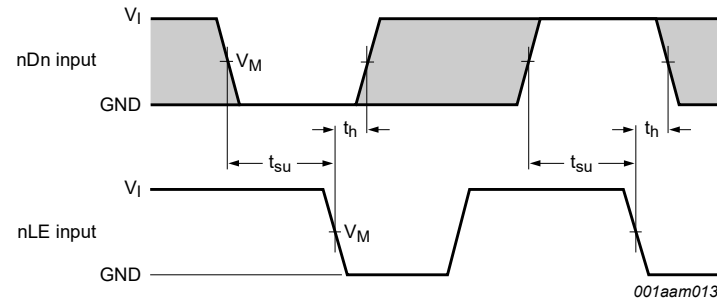
10.1. Waveforms and test circuit





Measurement points are given in [Table 8](#).
 V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 7. OFF-state to HIGH or LOW and HIGH or LOW to OFF-state propagation delays



Measurement points are given in [Table 8](#).

Fig. 8. Input (nDn) to input (nLE) data set-up and hold times

Table 8. Measurement points

V_{CC}	Input		Output		
	V_I	V_M	V_M	V_X	V_Y
$V_{CC} \leq 2.7 \text{ V}$	V_{CC}	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	$V_{OL} + 0.15 \text{ V}$	$V_{OH} - 0.15 \text{ V}$
$V_{CC} \geq 3.0 \text{ V}$	3.0 V	1.5 V	1.5 V	$V_{OL} + 0.3 \text{ V}$	$V_{OH} - 0.3 \text{ V}$

11. Package outline

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1 mm

SOT362-1

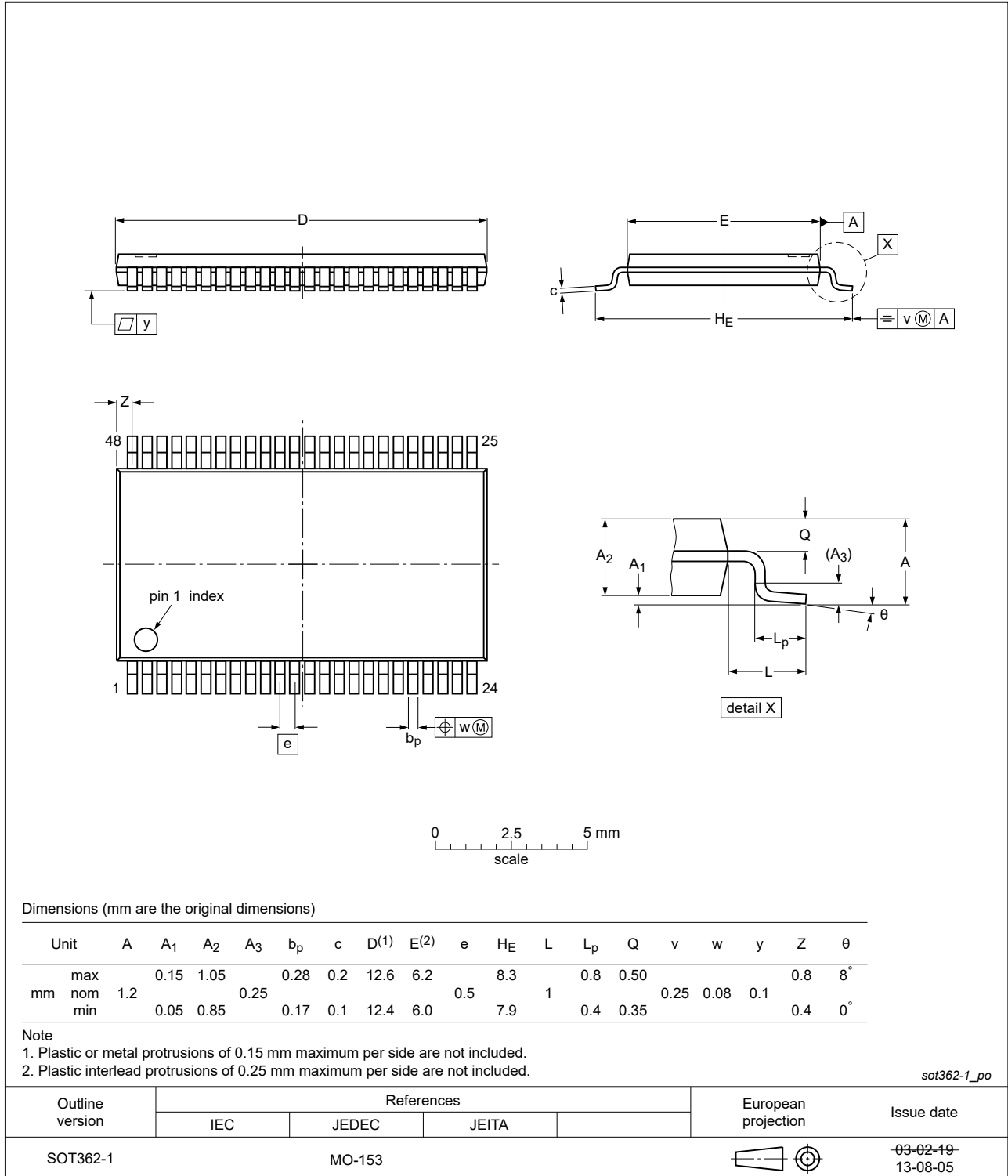


Fig. 10. Package outline SOT362-1 (TSSOP48)

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
BiCMOS	Bipolar Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
MIL	Military
MM	Machine Model
TTL	Transistor-Transistor Logic

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74ALVT16373 v.5	20210714	Product data sheet	-	74ALVT16373 v.4
Modifications:	<ul style="list-style-type: none"> • Section 1 and Section 2 updated. • Type number 74ALVT16373DL (SOT370-1/SSOP48) removed. 			
74ALVT16373 v.4	20180202	Product data sheet	-	74ALVT16373 v.3
Modifications:	<ul style="list-style-type: none"> • The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate. 			
74ALVT16373 v.3	19991018	Product specification	-	74ALVT16373 v.2
74ALVT16373 v.2	19980213	Product specification	-	74ALVT16373 v.1
74ALVT16373 v.1	19960529	Product specification	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. Nexperia does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local Nexperia sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between Nexperia and its customer, unless Nexperia and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the Nexperia product is deemed to offer functions and qualities beyond those described in the Product data sheet.

Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, Nexperia does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. Nexperia takes no responsibility for the content in this document if provided by an information source outside of Nexperia.

In no event shall Nexperia be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, Nexperia's aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of Nexperia.

Right to make changes — Nexperia reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — Nexperia products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an Nexperia product can reasonably be expected to result in personal

injury, death or severe property or environmental damage. Nexperia and its suppliers accept no liability for inclusion and/or use of Nexperia products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Quick reference data — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. Nexperia makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using Nexperia products, and Nexperia accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the Nexperia product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

Nexperia does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using Nexperia products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). Nexperia does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — Nexperia products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nexperia.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. Nexperia hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of Nexperia products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Non-automotive qualified products — Unless this data sheet expressly states that this specific Nexperia product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. Nexperia accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without Nexperia's warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond Nexperia's specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies Nexperia for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond Nexperia's standard warranty and Nexperia's product specifications.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

Contents

1. General description	1
2. Features and benefits	1
3. Ordering information	1
4. Functional diagram	2
5. Pinning information	3
5.1. Pinning.....	3
5.2. Pin description.....	3
6. Functional description	4
7. Limiting values	4
8. Recommended operating conditions	5
9. Static characteristics	5
10. Dynamic characteristics	7
10.1. Waveforms and test circuit.....	8
11. Package outline	11
12. Abbreviations	12
13. Revision history	12
14. Legal information	13

© Nexperia B.V. 2021. All rights reserved

For more information, please visit: <http://www.nexperia.com>
For sales office addresses, please send an email to: salesaddresses@nexperia.com
Date of release: 14 July 2021
