

Product Specification

NHD-3.5-320240JF-ASXP

TFT Liquid Crystal Display

NHD -	Newhaven Display
3.5 -	3.5" Diagonal
320240 -	320xRGBx240 Pixels
JF -	Model
A -	Built-in Driver / No Controller
S -	High Brightness, White LED Backlight
X -	TFT
P -	IPS, Wide Temperature

Table of Contents

Document Revision History	2
Mechanical Drawing	3
Pin Description	4
RGB Interface Mode Selection	4
Electrical Characteristics	5
Optical Characteristics	5
Driver Information	5
AC Characteristics	6
Timing Characteristics for TFT	7
Quality Information	12

Additional Resources

- **Support Forum:** <https://support.newhavendisplay.com/hc/en-us/community/topics>
- **Github:** <https://github.com/newhavendisplay>
- **Example Code:** https://www.newhavendisplay.com/example_code.html
- **Knowledge Center:** https://www.newhavendisplay.com/knowledge_center.html
- **Quality Center:** https://www.newhavendisplay.com/quality_center.html
- **Precautions for using LCDs/LCMs:** <https://www.newhavendisplay.com/specs/precautions.pdf>
- **Warranty / Terms & Conditions:** <https://www.newhavendisplay.com/terms.html>

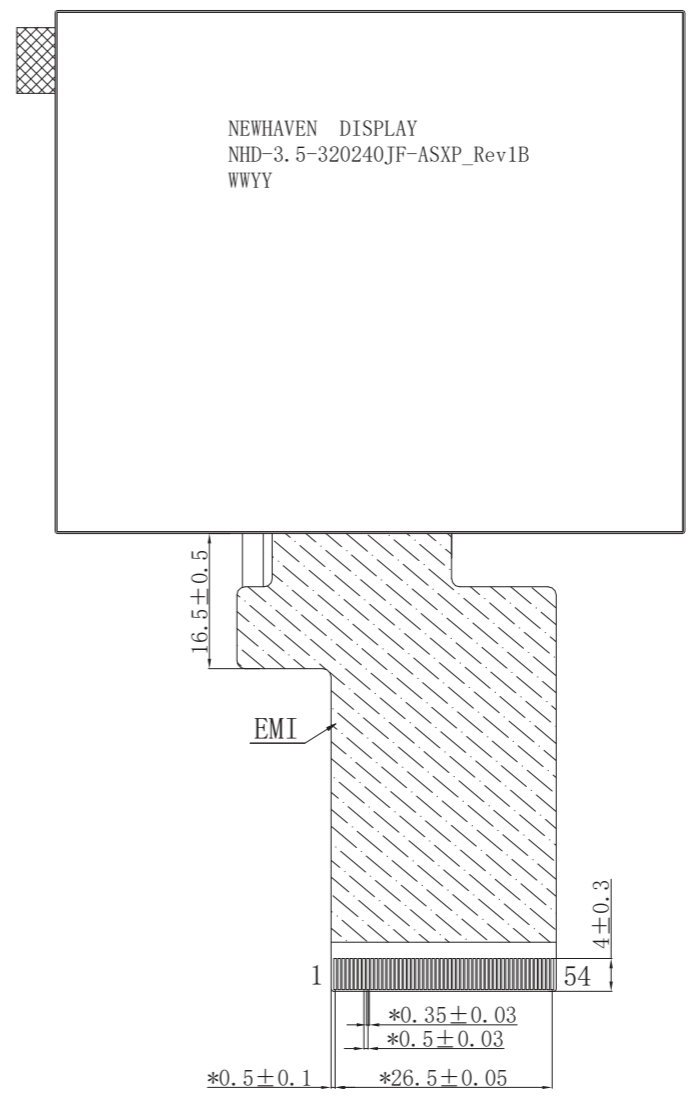
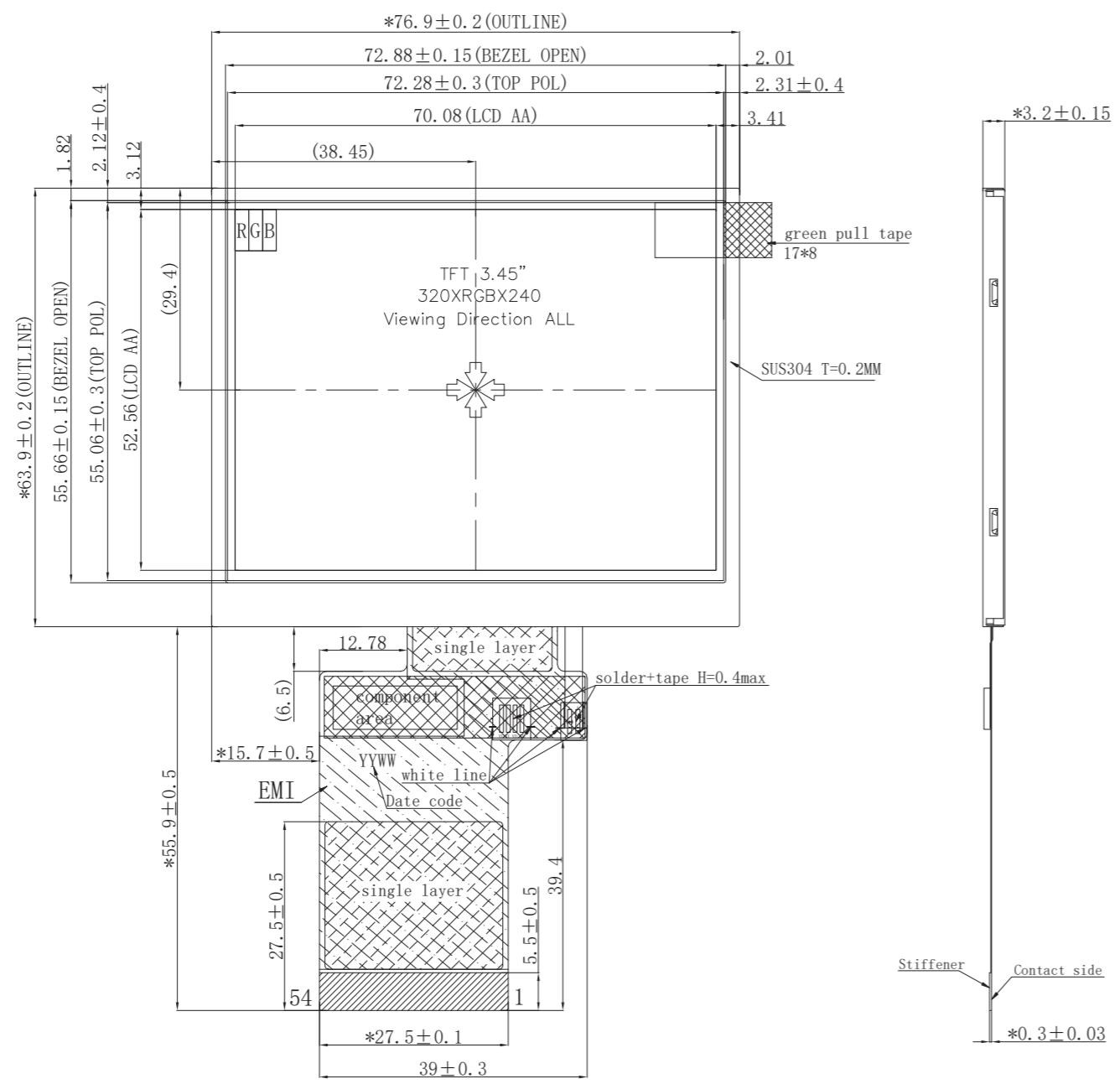


Document Revision History

Revision	Date	Description	Changed By
0	10/12/20	Initial Release	AS
1	2/4/22	Updated RGB Interface System Bus Timing table, Electrical Characteristics, Optical Characteristics, and Mechanical Drawing	CJ
2	6/6/22	Updated to add the RGB Interface Mode Selection section	CJ
3	6/9/22	Updated Optical Characteristics and Mechanical Drawing	CJ

Mechanical Drawing

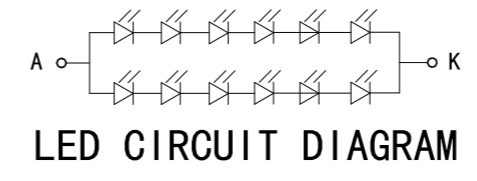
SYMBOL	REVISION	DATE



Pin No.	Symbol
1	LED_K
2	LED_K
3	LED_A
4	LED_A
5	NC
6	NC
7	NC
8	RSTB
9	SPENB
10	SPCK
11	SPDA
12-19	B0-B7
20-27	G0-G7
28-35	R0-R7
36	HSD
37	VSD
38	CLKIN
39	NC
40	NC
41	VDD
42	VDD
43	NC
44	NC
45	NC
46	NC
47	NC
48	NC
49	NC
50	NC
51	NC
52	DEN
53	GND
54	GND

Product Description: 3.5" IPS TFT

1. TFT Driver IC: ST7272A
2. TFT Interface: 24-Bit RGB
3. TFT Power Requirement: 3.3V, Backlight: 18.6V/40mA
4. Optical Features: Normally Black, Transmissive, Anti-Glare, 1100 cd/m²
5. TFT Mating Connector: 54pin, 0.5mm pitch; Ex. Molex 51296-5494



STANDARD TOLERANCE: (UNLESS OTHERWISE SPECIFIED)	NEWHAVEN DISPLAY INTERNATIONAL	
LINEAR: ±0.3mm	DRAWING/PART NUMBER: NHD-3.5-320240JF-ASXP	REVISION: 1B
UNLESS OTHERWISE SPECIFIED: - DIMENSIONS ARE IN MILLIMETERS - THIRD ANGLE PROJECTION	DRAWN BY: C. Johnson	APPROVED BY: C. Johnson
	DRAWN DATE: 6/9/22	APPROVED DATE: 6/9/22
	DO NOT SCALE DRAWING	
	SHEET 1 OF 1	
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Pin Description

TFT:

Pin No.	Symbol	External Connection	Function Description
1	LED_K	Power Supply	Backlight Cathode (Ground)
2	LED_K	Power Supply	Backlight Cathode (Ground)
3	LED_A	Power Supply	Backlight Anode (40mA @ 18.6V)
4	LED_A	Power Supply	Backlight Anode (40mA @ 18.6V)
5	NC	-	No Connect
6	NC	-	No Connect
7	NC	-	No Connect
8	RSTB	MPU	Active LOW Reset signal
9	SPENB	MPU	Active LOW Serial Chip Select signal
10	SPCK	MPU	Serial Clock signal
11	SPDA	MPU	Serial Data signal
12-19	B0-B7	MPU	Blue Data signals
20-27	G0-G7	MPU	Green Data signals
28-35	R0-R7	MPU	Red Data signals
36	HSD	MPU	Horizontal (Line) Sync signal
37	VSD	MPU	Vertical (Frame) Sync signal
38	CLKIN	MPU	Dot Clock signal
39-40	NC	-	No Connect
41	VDD	Power Supply	Supply Voltage for LCD and logic (3.3V)
42	VDD	Power Supply	Supply Voltage for LCD and logic (3.3V)
43-51	NC	-	No Connect
52	DEN	-	Data Enable signal (No Connect)
53	GND	Power Supply	Ground
54	GND	Power Supply	Ground

Recommended LCD connector: 0.5mm pitch 54-Conductor FFC. Molex p/n: 51296-5494

RGB Interface Mode Selection

The Sitronix ST7272A driver IC is user configurable for DE Mode, SYNC mode, or SYNC-DE mode RGB interface.

DE Mode is enabled when HSYNC and VSYNC signals are set to logic-low state, and DE signal is toggled high for valid pixel data. Data is clocked in using DCLK signal. DE mode is recommended to enable the ST7272A driver IC to synchronize the display image on TFT panel without depending on specific horizontal and vertical sync timing from host controller.

SYNC mode is enabled when the DE signal is set to logic-low state, and HSYNC and VSYNC signals are used to explicitly define the horizontal and vertical sync timing to synchronize the display image on TFT panel. Data is clocked in using DCLK signal. Any change to the HSYNC or VSYNC values may prevent the image from correctly appearing on the display.

SYNC-DE Mode is enabled when HSYNC and VSYNC signals are used to explicitly define the horizontal and vertical sync timing to synchronize the display image on TFT panel. DE signal is used as an additional indicator for transmission of valid pixel data. Data is clocked in using DCLK signal. Any change to the HSYNC or VSYNC values may prevent the image from correctly appearing on the display.

RGB Mode Selection Table	DCLK	HSYNC	VSYNC	DE
SYNC-DE Mode	Input	Input	Input	Input
SYNC Mode	Input	Input	Input	GND
DE Mode	Input	GND	GND	Input



Electrical Characteristics

TFT:

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating Temperature Range	T _{OP}	Absolute Max	-20	-	+70	°C
Storage Temperature Range	T _{ST}	Absolute Max	-30	-	+80	°C
Supply Voltage	V _{DD}	-	3.0	3.3	3.6	V
Supply Current	I _{DD}	V _{DD} = 3.3V	10	20	30	mA
"H" Level input	V _{IH}	-	0.7*V _{DD}	-	V _{DD}	V
"L" Level input	V _{IL}	-	V _{SS}	-	0.3*V _{DD}	V
"H" Level output	V _{OH}	-	V _{DD} -0.4	-	V _{DD}	V
"L" Level output	V _{OL}	-	V _{SS}	-	V _{SS} +0.4	V
Backlight Supply Current	I _{LED}	-	30	40	50	mA
Backlight Supply Voltage	V _{LED}	I _{LED} = 40mA	17.4	18.6	19.8	V
Backlight Lifetime*	-	T _{OP} = 25°C	30,000	50,000	-	Hrs.

*Backlight lifetime is rated as Hours until **half-brightness**, under normal operating conditions. The LED of the backlight is driven by current drain; drive voltage is for reference only. Drive voltage must be selected to ensure backlight current drain is below MAX level stated.

Optical Characteristics:

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	
Optimal Viewing Angles	Top	CR ≥ 10	70	80	-	°	
	Bottom		70	80	-	°	
	Left		70	80	-	°	
	Right		70	80	-	°	
Contrast Ratio	CR	-	640	800	-	-	
Luminance	L _V	I _{LED} = 40 mA	800	1100	-	cd/m ²	
Response Time (Rise + Fall)	T _R + T _F	T _{OP} = 25°C	-	30	40	ms	
Chromaticity	Red	X _R	-	0.582	0.632	0.682	-
		Y _R	-	0.296	0.346	0.396	-
	Green	X _G	-	0.311	0.361	0.411	-
		Y _G	-	0.546	0.596	0.646	-
	Blue	X _B	-	0.093	0.143	0.193	-
		Y _B	-	0.031	0.081	0.131	-
White	X _W	-	0.288	0.318	0.348	-	
	Y _W	-	0.290	0.320	0.350	-	

Driver Information

Built-in ST7272A driver. No controller.

Please download specification at:

https://www.newhavendisplay.com/resources_dataFiles/datasheets/LCDs/ST7272A.pdf

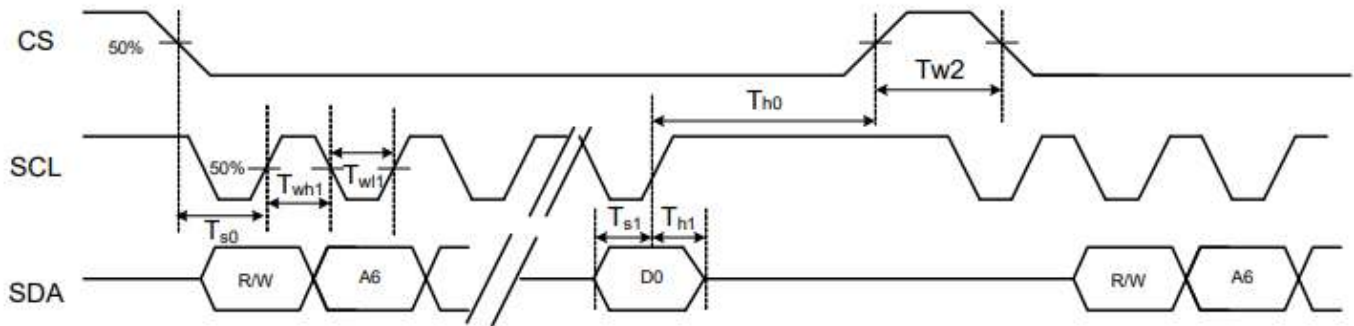


AC Characteristics

System Operation AC Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Conditions
VDD Power Source Slew Time	TPOR	-	-	20	ms	From 0V to 99% VDD
GRB Pulse Width	tRSTW	10	50	-	us	R=10Kohm, C=1uF
SD Output Stable Time	Tst	-	-	12	us	Output settled within +20mV Loading = 6.8k+28.2pF.
GD Output Rise and Fall Time	Tgst	-	-	6	us	Output settled (5%~95%), Loading = 4.7k+29.8pF

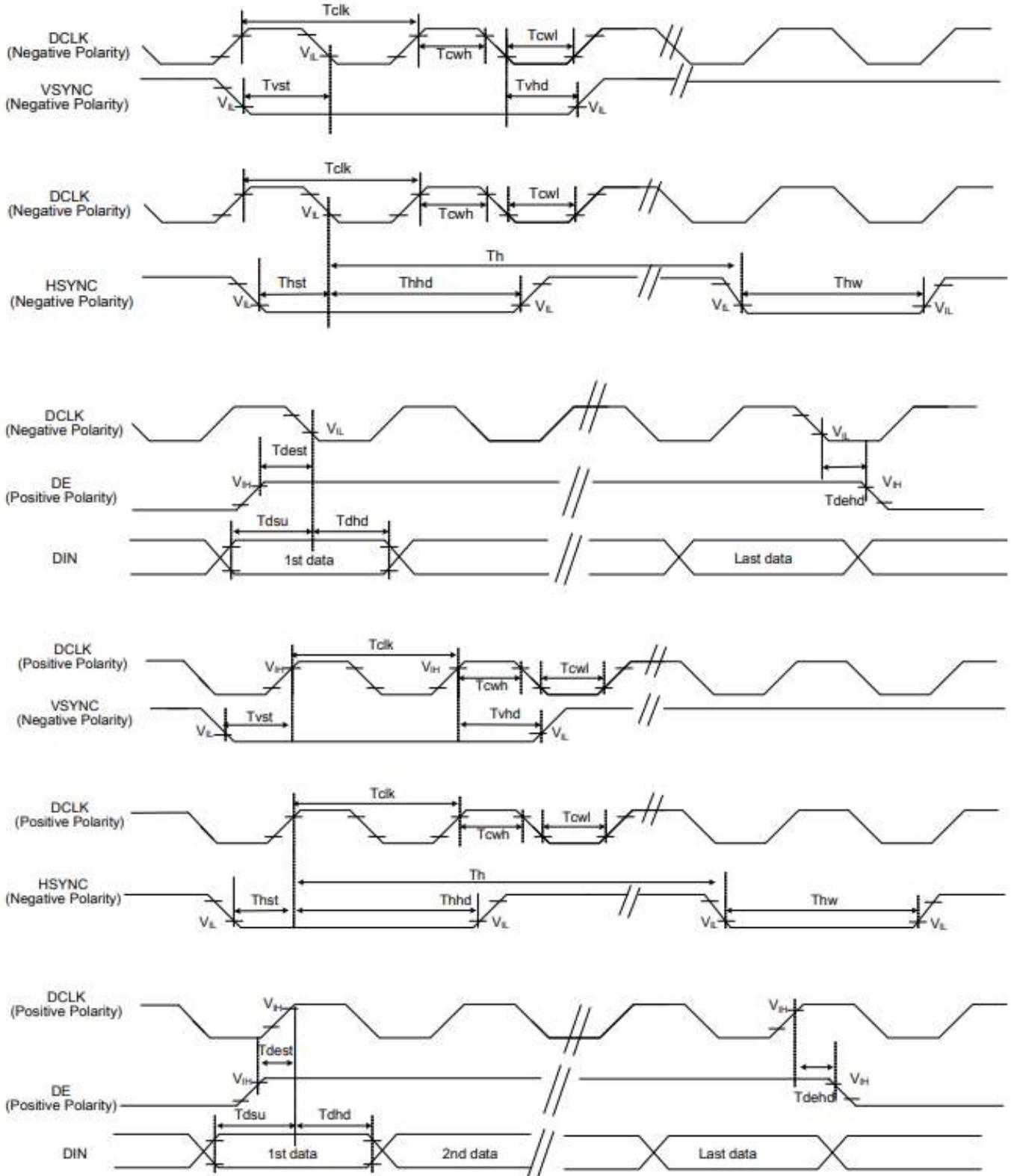
System Bus Timing for 3-Wire SPI Interface



Item	Symbol	Min.	Typ.	Max.	Unit	Conditions
CS Input Setup Time	Ts0	50	-	-	ns	
Serial Data Input Setup Time	Ts1	50	-	-	ns	
CS Input Hold Time	Th0	50	-	-	ns	
Serial Data Input Hold Time	Th1	50	-	-	ns	
SCL Write Pulse High Width	Twh1	50	-	-	ns	
SCL Write Pulse Low Width	Twl1	50	-	-	ns	
SCL Read Pulse High Width	Trh1	300			ns	
SCL Read Pulse Low Width	Trl1	300			ns	
CS Pulse High Width	Tw2	400	-	-	ns	

Timing Characteristics – TFT Display

System Bus Timing for RGB Interface



Parallel 24-bit RGB Input Timing (V_{DD} = 3.3V, GND = 0V, T_{OP} = 25°C)

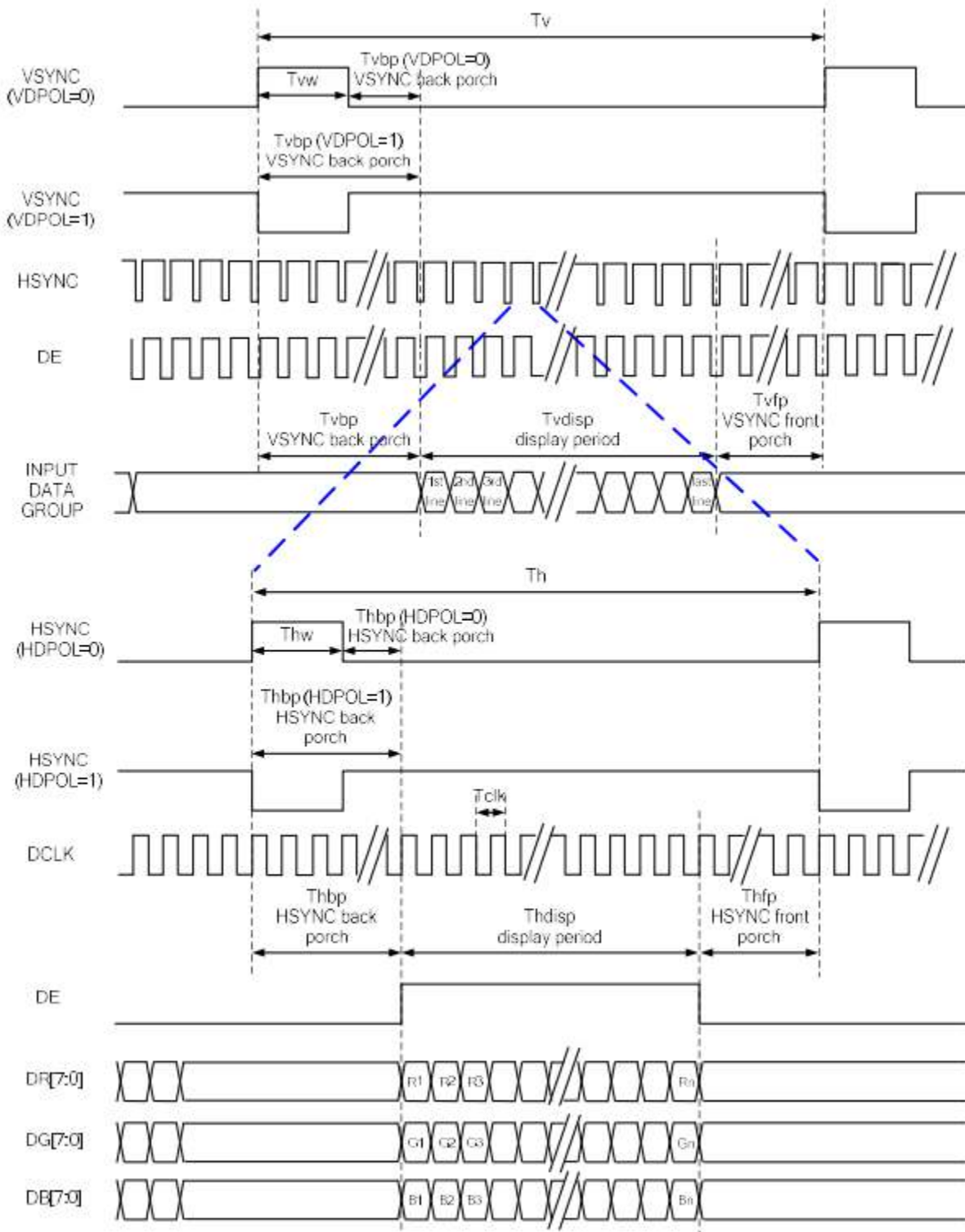
Parallel 24-bit RGB Input Timing Table							
Item	Symbol	Min.	Typ.	Max.	Unit	Note	
DCLK Frequency	Fclk	5	6	8	MHz		
DCLK Period	Tclk	125	167	200	ns		
HSYNC	Period Time	Th	325	371	438	DCLK	
	Display Period	Thdisp	-	320	-	DCLK	
	Back Porch	Thbp	3	43	43	DCLK	SYNC mode back porch control by H_BLANKING[7:0] setting Thbp= H_BLANKING[7:0]
	Front Porch	Thfp	2	8	75	DCLK	
	Pulse Width	Thw	2	4	43	DCLK	
VSYNC	Period Time	Tv	244	260	289	HSYNC	
	Display Period	Tvdisp	-	240	-	HSYNC	
	Back Porch	Tvbp	2	12	12	HSYNC	SYNC mode back porch control by V_BLANKING[7:0] setting Tvbp= V_BLANKING[7:0]
	Front Porch	Tvfp	2	8	37	HSYNC	
	Pulse Width	Tvw	2	4	12	HSYNC	

Note: It is necessary to keep Tvbp =12 and Thbp =43 in sync mode. DE mode is unnecessary to keep it.

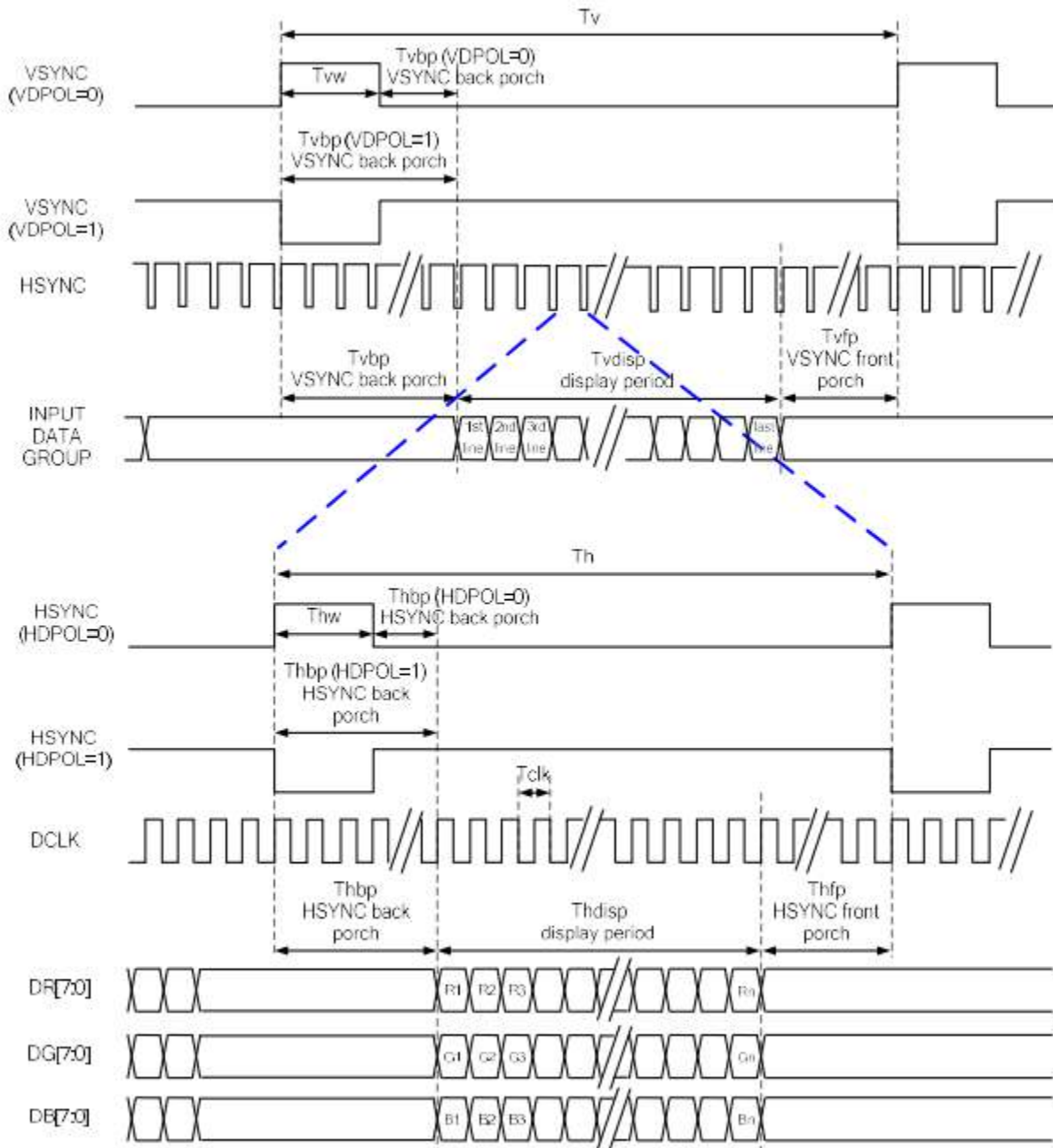
System Bus Timing

Item	Symbol	Min.	Typ.	Max.	Unit	Conditions
CLK Pulse Duty	Tclk	40	50	60	%	
HSYNC Width	Thw	2	-	-	DCLK	
HSYNC Period	Th	55	60	65	us	
VSYNC Setup Time	Tvst	12	-	-	ns	
VSYNC Hold Time	Tvhd	12	-	-	ns	
HSYNC Setup Time	Thst	12	-	-	ns	
HSYNC Hold Time	Thhd	12	-	-	ns	
Data Setup Time	Tdsu	12	-	-	ns	
Data Hold Time	Tdhd	12	-	-	ns	
DE Setup Time	Tdest	12	-	-	ns	
DE Hold Time	Tdehd	12	-	-	ns	

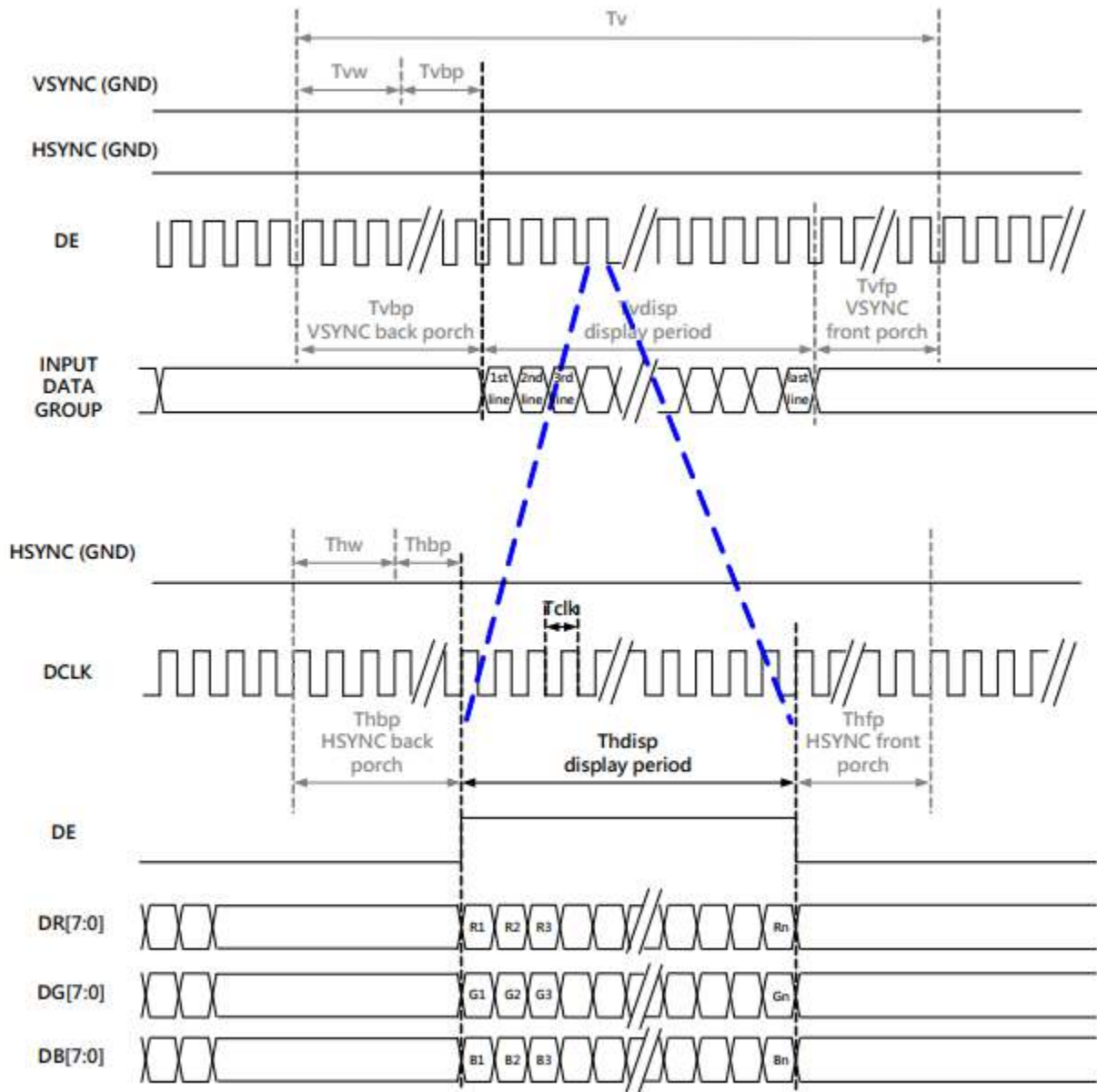
Parallel RGB Sync-DE Mode:



Parallel RGB Sync Mode:



Parallel RGB DE Mode:



Quality Information

Test Item	Content of Test	Test Condition	Note
High Temperature storage	Endurance test applying the high storage temperature for a long time.	+80°C , 240hrs	2
Low Temperature storage	Endurance test applying the low storage temperature for a long time.	-30°C , 240hrs	1,2
High Temperature Operation	Endurance test applying the electric stress (voltage & current) and the high thermal stress for a long time.	+70°C , 240hrs	2
Low Temperature Operation	Endurance test applying the electric stress (voltage & current) and the low thermal stress for a long time.	-20°C , 240hrs	1,2
High Temperature / Humidity Storage	Endurance test applying the electric stress (voltage & current) and the high thermal with high humidity stress for a long time.	+60°C , 90% RH , 240hrs	1,2
Thermal Shock resistance	Endurance test applying the electric stress (voltage & current) during a cycle of low and high thermal stress.	-30°C,30min -> 25°C,3min -> 80°C,30min = 1 cycle 20 cycles	
Vibration test	Endurance test applying vibration to simulate transportation and use.	10-55Hz , 1.5mm amplitude. 2G Acceleration 30min in each of 3 directions X,Y,Z	3
Static electricity test	Endurance test applying electric static discharge.	Air: ±8kV 150pF/330Ω, 5 Times	
		Contact: ±4kV 150pF/330Ω, 5 Times	

Note 1: No condensation to be observed.

Note 2: Conducted after 4 hours of storage at 25°C, 0%RH.

Note 3: Test performed on product itself, not inside a container.