

STD35NF3LL

General features

Туре	V _{DSS}	R _{DS(on)}	I _D
STD35NF3LL	30V	<0.0195Ω	35A

- Optimal R_{DS}(on) x Q_g trade-off @ 4.5V
- Conduction losses reduced
- Switching losses reduced
- Low threshold drive

Description

This application specific Power MOSFET is the third generation of STMicroelectronics unique "single feature size[™]" strip-based process. The resulting transistor shows the best trade-off between on-resistance and gate charge. When used as high and low side in buck regulators, it gives the best performance in terms of both conduction and switching losses. This is extremely important for motherboards where fast switching and high efficiency are of paramount importance. remarkable manufacturing reproducibility.

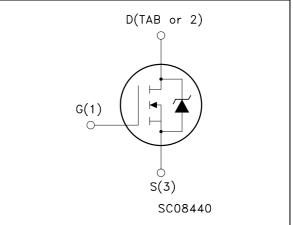
Applications

Switching application

Order codes

DPAK
olete r.

Internal schematic diagram



Part number	Marking	Package	Packaging
STD35NF3LLT4	35NF3LLT4 D35NF3LL		Tape & reel

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0050	Revision history



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Electrical ratings

Table 1.	Absolute maximum ratings
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Symbol	Parameter	Value	Unit				
V _{DS}	Drain-source voltage (V _{GS} = 0)	30	V				
V _{GS}	Gate- source voltage	± 16	V				
I _D	Drain current (continuous) at $T_C = 25^{\circ}C$	35	А				
I _D	Drain current (continuous) at T _C = 100°C	25	А				
I _{DM} ⁽¹⁾	Drain current (pulsed)	140	Α				
P _{tot}	Total dissipation at $T_C = 25^{\circ}C$	50					
	Derating factor	0.33	W/°C				
E _{AS} ⁽²⁾	Single pulse avalanche energy	300	mJ				
T _{stg}	Storage temperature						
Тj	Max. operating junction temperature	-55 to 175 °C					
1. Pulse width	. Pulse width limited by safe operating area.						
2. Starting $T_j = 25 \text{ °C}$, $I_D = 17.5A$, $V_{DD} = 24V$							
05-							
Table 2.	Thermal data						
D		-					

Table 2. Thermal data

	Rthj-case	Thermal resistance junction-case max	3	°C/W
	Rthj-amb	Thermal resistance junction-to ambient max	100	°C/W
	Т _Ј	Maximum lead temperature for soldering purpose	300	°C
005018				

Electrical characteristics 2

(T_{CASE}=25°C unless otherwise specified)

	0.40.000					
Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	I _D = 250μΑ, V _{GS} =0	30			V
I _{DSS}	Zero gate voltage drain current (V _{GS} = 0)	V_{DS} = Max rating V_{DS} = Max rating @125°C			1 10	μΑ μΑ
I _{GSS}	Gate-body leakage current (V _{DS} = 0)	$V_{GS} = \pm 16V$			±100	nA
V _{GS(th)}	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250 \mu A$	1	²	2.5	V
R _{DS(on)}	Static drain-source on resistance	$V_{GS} = 10V, I_D = 17.5A$ $V_{GS} = 4.5V, I_D = 17.5A$	21	0.014 0.016	0.0195 0.0215	Ω Ω
Table 4.	Dynamic	lete				

Table 3. **On/off states**

Table 4. Dynamic

	Bynamic					
Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
g _{fs} ⁽¹⁾	Forward transconductance	V _{DS} = 15V, I _D = 17.5A		19		S
C _{iss} C _{oss} C _{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V _{DS} = 25V, f = 1MHz, V _{GS} = 0		800 250 60		pF pF pF
t _{d(on)} t _r t _{d(off)} t _f	Turn-on delay time Rise time Turn-off delay time Fall time	$V_{DD} = 15V, I_D = 17.5A$ $R_G = 4.7\Omega V_{GS} = 4.5V$ (see <i>Figure 12</i>)		17 100 20 21		ns ns ns ns
Q _g Q _{gs} Q _{gd}	Total gate charge Gate-source charge Gate-drain charge	$V_{DD} = 24V$, $I_D = 35A$, $V_{GS} = 5V$, $R_G = 4.7\Omega$ (see <i>Figure 13</i>)		12.5 42 5.2	17	nC nC nC



Table J.	Source drain diode					
Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
las	Source-drain current				35	А
I _{SD} I _{SDM} ⁽¹⁾	Source-drain current				140	A
V _{SD} ⁽²⁾	(pulsed) Forward on voltage	I _{SD} = 35A, V _{GS} = 0			1.3	v
				25	1.5	
t _{rr} Q _{rr}	Reverse recovery time Reverse recovery charge	$I_{SD} = 35A$, di/dt = 100A/µs, $V_{DD} = 15V$, $T_i = 150^{\circ}C$		35 44		ns nC
I _{RRM}	Reverse recovery current	(see <i>Figure 17</i>)		2.5		A
1. Pulse wi	dth limited by safe operating are	a.	l	l		
2. Pulsed:	Pulse duration = 300 µs, duty cy	cle 1.5%			10	\mathbf{A}
					11-	
				111	0	
				0		
			220			
		XC				
		200				
		SO'				
		\sim				
		U.				
	.(5)					
0	$\langle O \rangle$					
20						
6						
		V _{DD} = 15V, 1 _j = 150°C (see <i>Figure 17</i>) a. cle 1.5%				

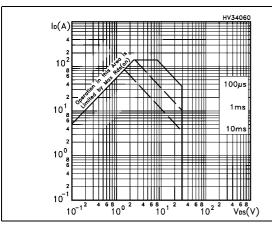
Table 5. Source drain diode

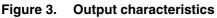
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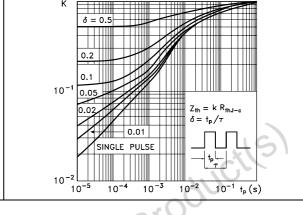
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Electrical characteristics (curves) 2.1

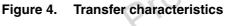
Figure 1. Safe operating area







Thermal impedance



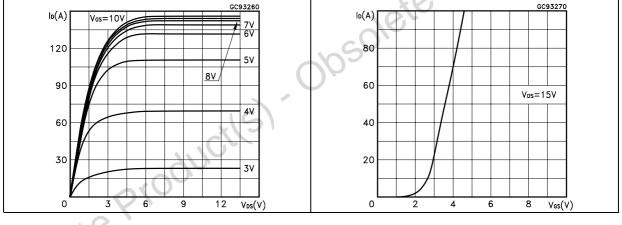
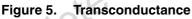
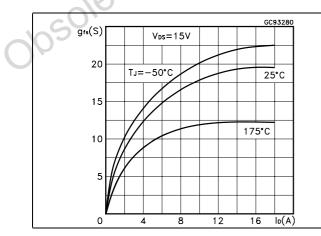
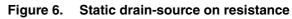


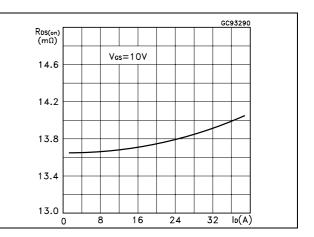
Figure 2.

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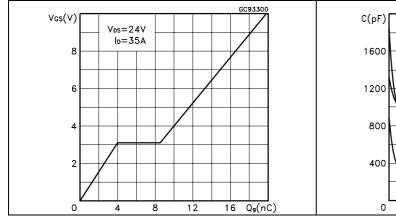
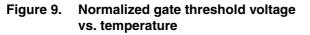
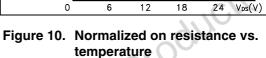


Figure 7. Gate charge vs. gate-source voltage Figure 8. Capacitance variations





Ciss

Coss

Crss

f=1MHz Vcs=0V

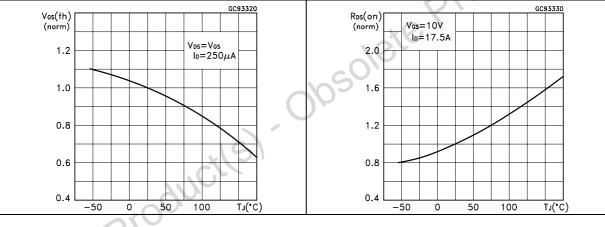
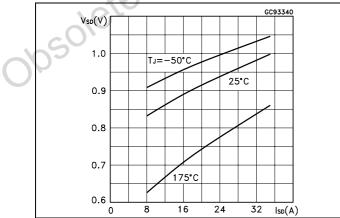


Figure 11. Source-drain diode forward characteristics





3 Test circuit

Figure 12. Switching times test circuit for resistive load

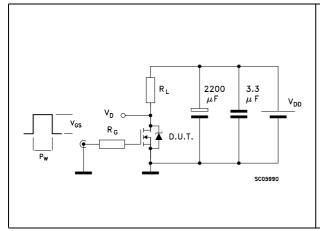


Figure 14. Test circuit for inductive load switching and diode recovery times

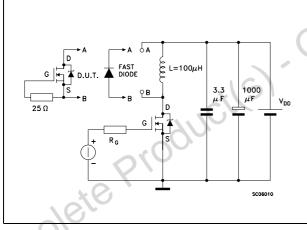
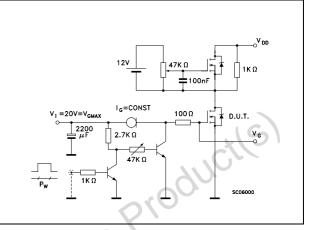
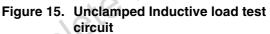


Figure 16. Unclamped inductive waveform





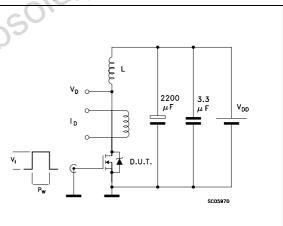


Figure 17. Switching time waveform

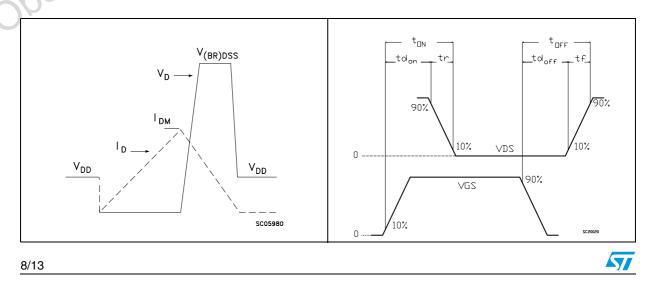


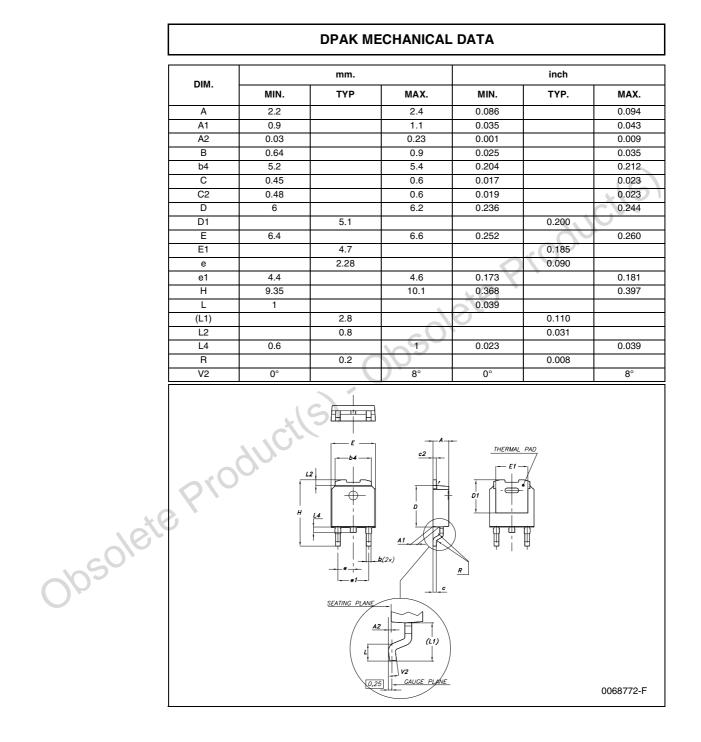
Figure 13. Gate charge test circuit

4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: *www.st.com*

Obsolete Product(s). Obsolete Product(s)

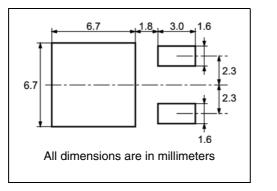
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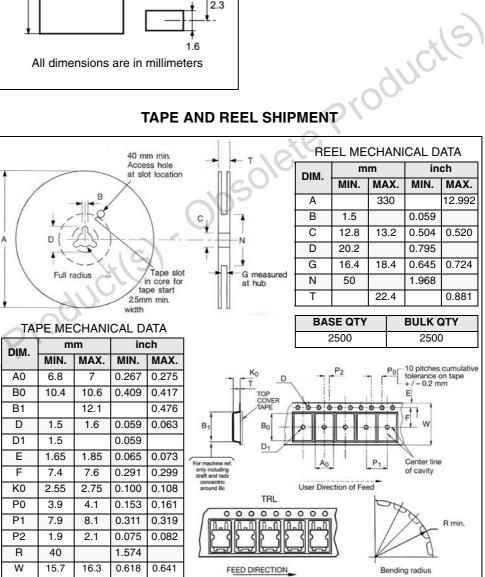


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Packing mechanical data 5

DPAK FOOTPRINT





TAPE AND REEL SHIPMENT

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3bsolet

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6 Revision history

Table 6. Revision history

	Date	Revision	Changes
	21-Jun-2004	2	Preliminary version
	06-Jul-2006	3	New template, no content change
	14-sep-2006	4	Removed IPAK
	20-Feb-2007	5	Typo mistake on page 1
005016	teprod	JUCILS	Typo mistake on page 1

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