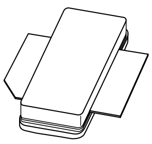

BLF4G10LS-120

UHF power LDMOS transistor

Rev. 01 — 10 January 2006 **Product data sheet**

1. Product profile

1.1 General description

120 W LDMOS power transistor for base station applications at frequencies from 800 MHz to 1000 MHz.

Table 1: Typical performance

f = 920 MHz to 960 MHz; T_h = 25 °C; in a class-AB production test circuit; typical values.

Mode of operation	V_{DS} (V)	P_L (W)	G_p (dB)	η_D (%)	$ACPR_{400}$ (dBc)	$ACPR_{600}$ (dBc)	EVM (%)	IMD3 (dBc)
CW	28	120	19	57	-	-	-	-
GSM EDGE	28	48 (AV)	19	40	–61 [1]	–72 [2]	1.5	-
2-tone	28	120 (PEP)	19	46	-	-	-	–31

[1] $ACPR_{400}$ at 30 kHz resolution bandwidth

[2] $ACPR_{600}$ at 30 kHz resolution bandwidth

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Therefore care should be taken during transport and handling.

1.2 Features

- Typical GSM EDGE performance at a frequency of 920 MHz and 960 MHz, a supply voltage of 28 V and an I_{Dq} of 650 mA
  - Load power = 48 W (AV)
  - Gain = 19 dB (typ)
  - Efficiency = 40 % (typ)
  - $ACPR_{400}$ = –61 dBc (typ)
  - $ACPR_{600}$ = –72 dBc (typ)
  - EVM_{rms} = 1.5 % (typ)
- Easy power control
- Excellent ruggedness
- High efficiency
- Excellent thermal stability
- Designed for broadband operation (800 MHz to 1000 MHz)
- Internally matched for ease of use

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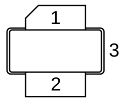
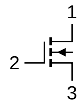
1.3 Applications

- RF power amplifiers for GSM, GSM EDGE and CDMA base stations and multicarrier applications in the 868 MHz to 961 MHz frequency range.

2. Pinning information

Table 2: Pinning

Pin	Description	Simplified outline	Symbol
1	drain		 sym039
2	gate		
3	source [1]		

[1] Connected to flange

3. Ordering information

Table 3: Ordering information

Type number	Package		
	Name	Description	Version
BLF4G10LS-120	-	earless flanged LDMOST ceramic package; 2 leads	SOT502B

4. Limiting values

Table 4: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	65	V
V_{GS}	gate-source voltage		–0.5	+15	V
I_D	drain current		-	12	A
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		-	200	°C

5. Thermal characteristics

Table 5: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-case)}$	thermal resistance from junction to case	T_{case} = 80 °C				
		P_L = 60 W	-	0.62	0.71	K/W
		P_L = 120 W	-	0.52	0.61	K/W

6. Characteristics

Table 6: Characteristics

T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.9 mA	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 180 mA	2.5	3.1	3.5	V
V_{GSq}	gate-source quiescent voltage	V_{DS} = 28 V; I_D = 900 mA	2.70	3.20	3.70	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 28 V	-	-	2.5	μA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 9 V; V_{DS} = 10 V	27	30	-	A
I_{GSS}	gate leakage current	V_{GS} = 15 V; V_{DS} = 0 V	-	-	300	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 10 A	-	9.0	-	S
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 6 V; I_D = 6 A	-	90	-	mΩ
C_{rs}	feedback capacitance	V_{GS} = 0 V; V_{DS} = 28 V; f = 1 MHz	-	2.5	-	pF

7. Application information

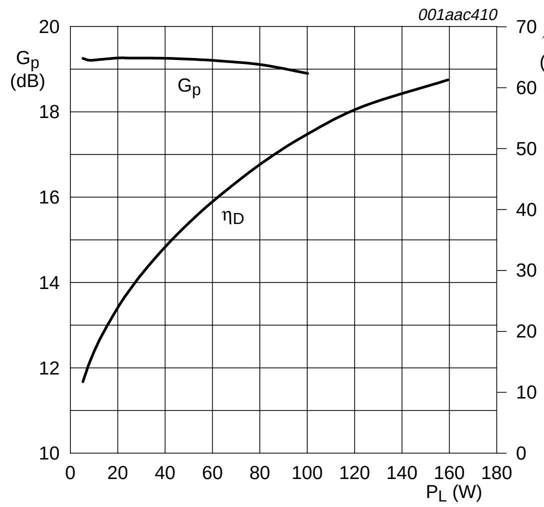
Table 7: Application information

Mode of operation: GSM EDGE; f = 920 MHz and 960 MHz; RF performance at V_{DS} = 28 V; I_{Dq} = 650 mA; T_{case} = 25 °C; unless otherwise specified, in a class AB production test circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	$P_{L(AV)}$ = 48 W	17.5	19	-	dB
IRL	input return loss	$P_{L(AV)}$ = 48 W	-	–8.0	–5.5	dB
η_D	drain efficiency	$P_{L(AV)}$ = 48 W	35.8	40	-	%
$ACPR_{400}$	adjacent channel power ratio (400 kHz)	$P_{L(AV)}$ = 48 W	-	–61	–58	dBc
$ACPR_{600}$	adjacent channel power ratio (600 kHz)	$P_{L(AV)}$ = 48 W	-	–72	–68	dBc
EVM_{rms}	rms EDGE signal distortion error	$P_{L(AV)}$ = 48 W	-	1.5	2.5	%
EVM_M	peak EDGE signal distortion error	$P_{L(AV)}$ = 48 W	-	5	8.5	%

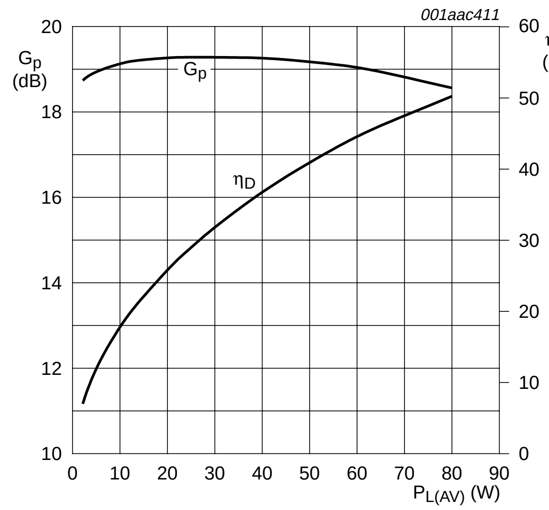
7.1 Ruggedness in class-AB operation

The BLF4G10LS-120 is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 28 V; I_{Dq} = 650 mA; P_L = 120 W (CW); f = 960 MHz.



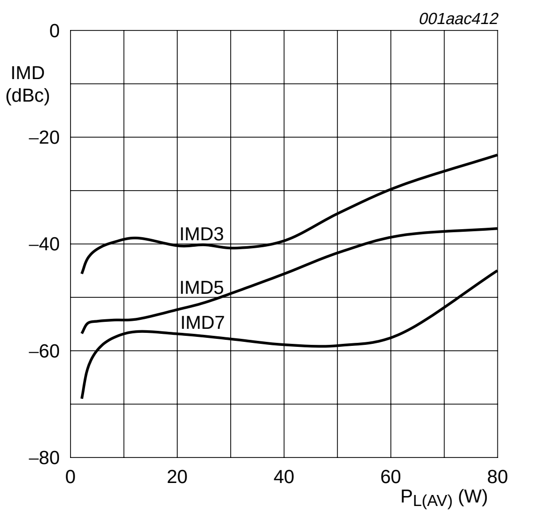
V_{DS} = 28 V; I_{Dq} = 650 mA; T_{case} = 25 °C;
f = 960 MHz

Fig 1. One-tone CW power gain and drain efficiency as functions of load power; typical values



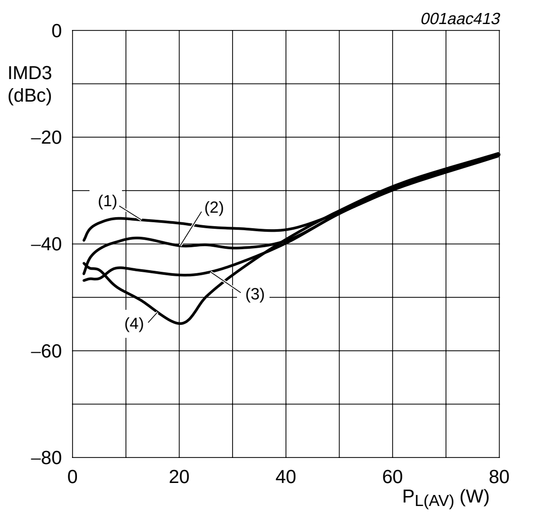
V_{DS} = 28 V; I_{Dq} = 650 mA; T_{case} = 25 °C;
f = 960 MHz

Fig 2. Two-tone CW power gain and drain efficiency as functions of average load power; typical values



V_{DS} = 28 V; I_{Dq} = 650 mA; T_{case} = 25 °C;
f = 960 MHz

Fig 3. Intermodulation distortion as a function of average load power; typical values



V_{DS} = 28 V; T_{case} = 25 °C; f = 960 MHz

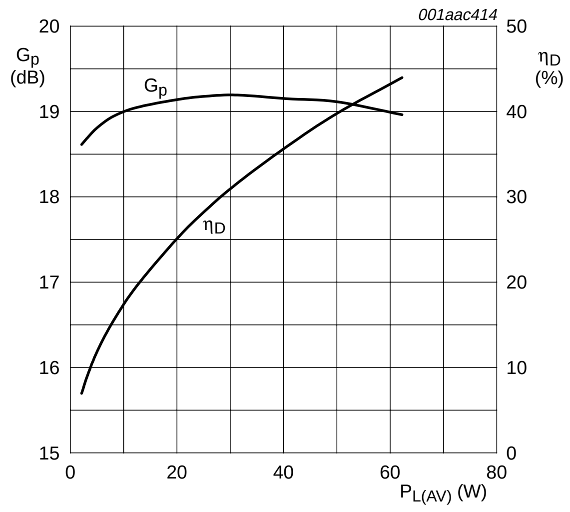
(1) I_{Dq} = 550 mA

(2) I_{Dq} = 650 mA

(3) I_{Dq} = 750 mA

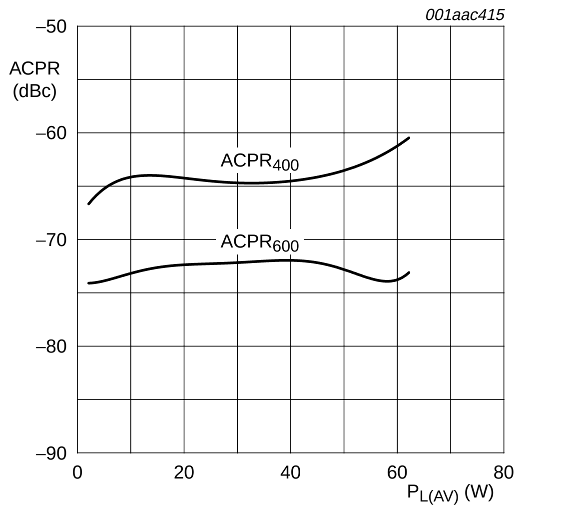
(4) I_{Dq} = 850 mA

Fig 4. Third order intermodulation distortion as a function of average load power; typical values



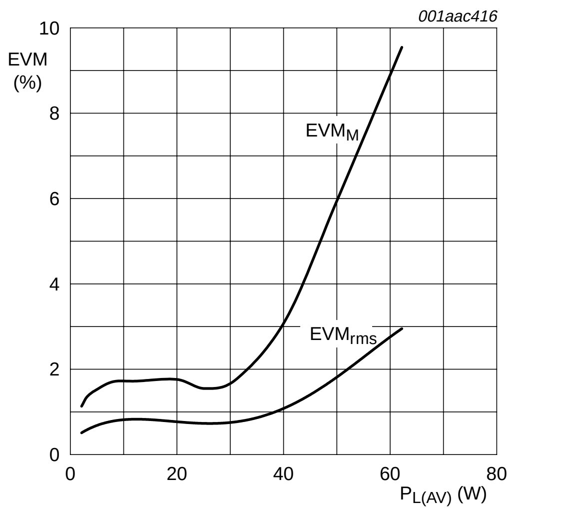
V_{DS} = 28 V; I_{Dq} = 650 mA; T_{case} = 25 °C;
f = 960 MHz

Fig 5. GSM EDGE power gain and drain efficiency as functions of average load power; typical values



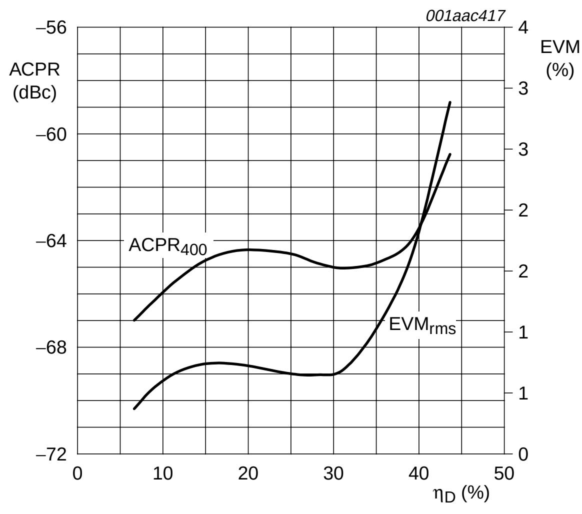
V_{DS} = 28 V; I_{Dq} = 650 mA; T_{case} = 25 °C;
f = 960 MHz

Fig 6. GSM EDGE ACPR at 400 kHz and at 600 kHz as a function of average load power; typical values



V_{DS} = 28 V; I_{Dq} = 650 mA; T_{case} = 25 °C;
f = 960 MHz

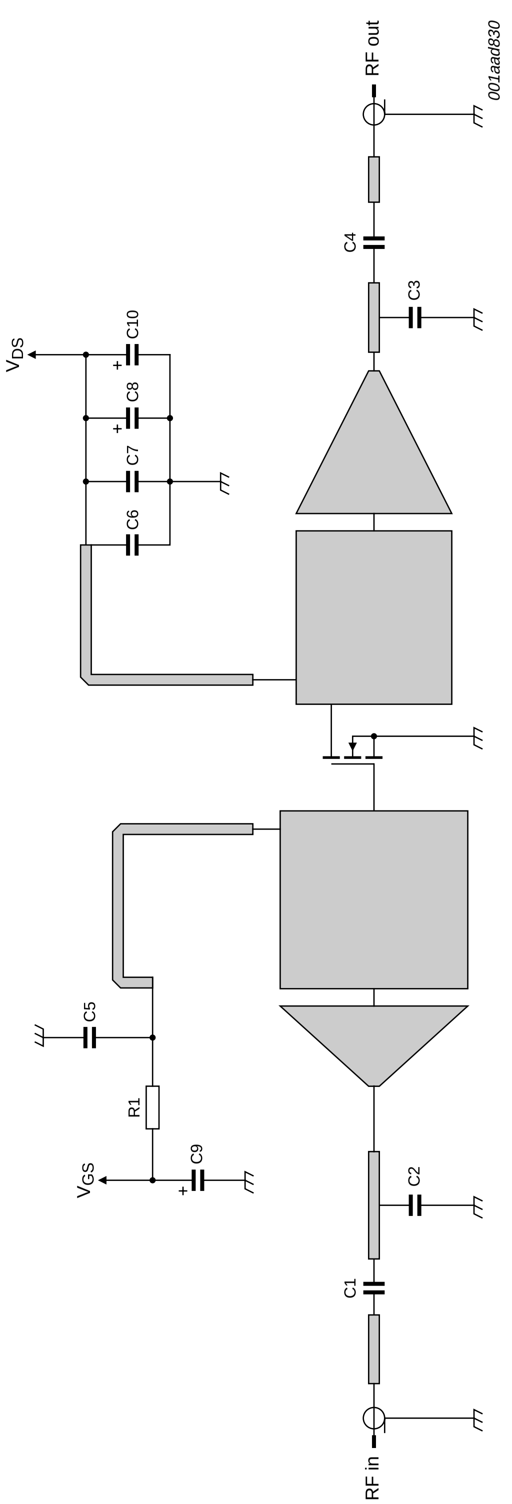
Fig 7. GSM EDGE rms EVM and peak EVM as functions of average load power; typical values



V_{DS} = 28 V; I_{Dq} = 650 mA; T_{case} = 25 °C;
f = 960 MHz

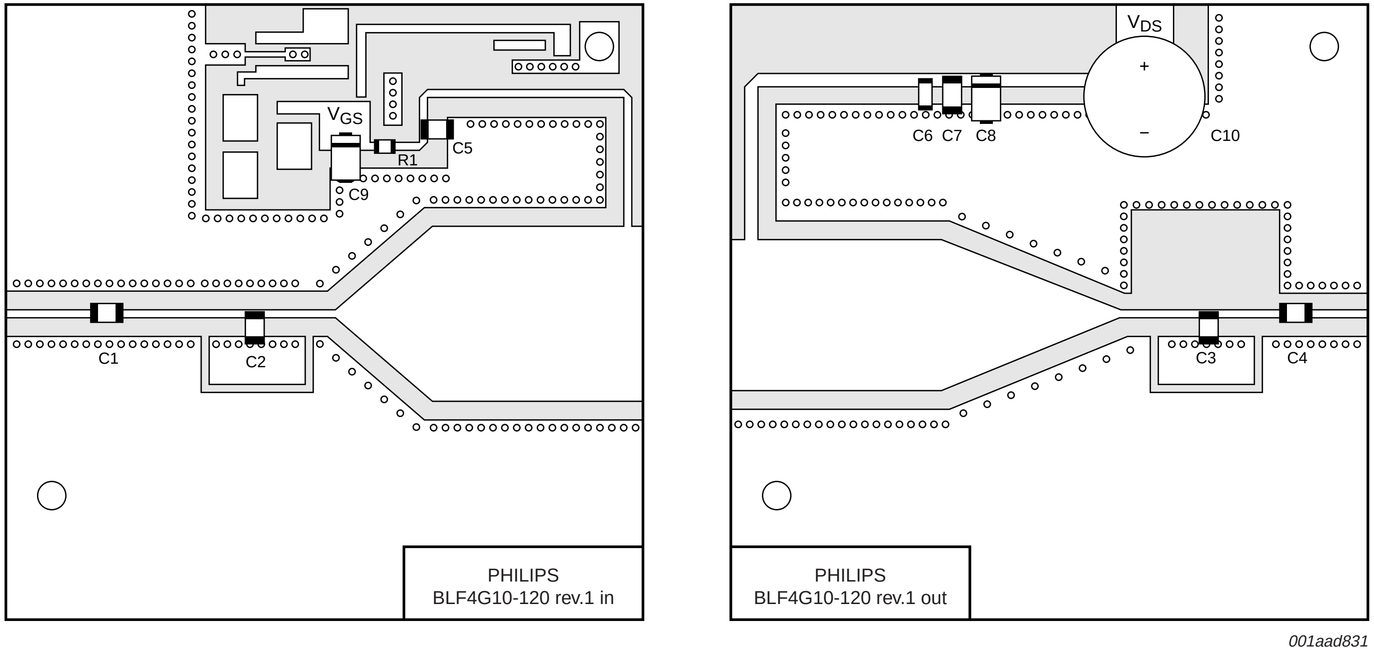
Fig 8. GSM EDGE ACPR at 400 kHz and rms EVM as functions of drain efficiency; typical values

8. Test information



See Table 8 for list of components.

Fig 9. Class-AB test circuit at f = 960 MHz



Striplines are on a double copper-clad Rogers 6006 Printed-Circuit Board (PCB) (ε_r = 6.2); thickness = 0.025 inches.

See Table 8 for list of components.

Fig 10. Component layout for 960 MHz test circuit

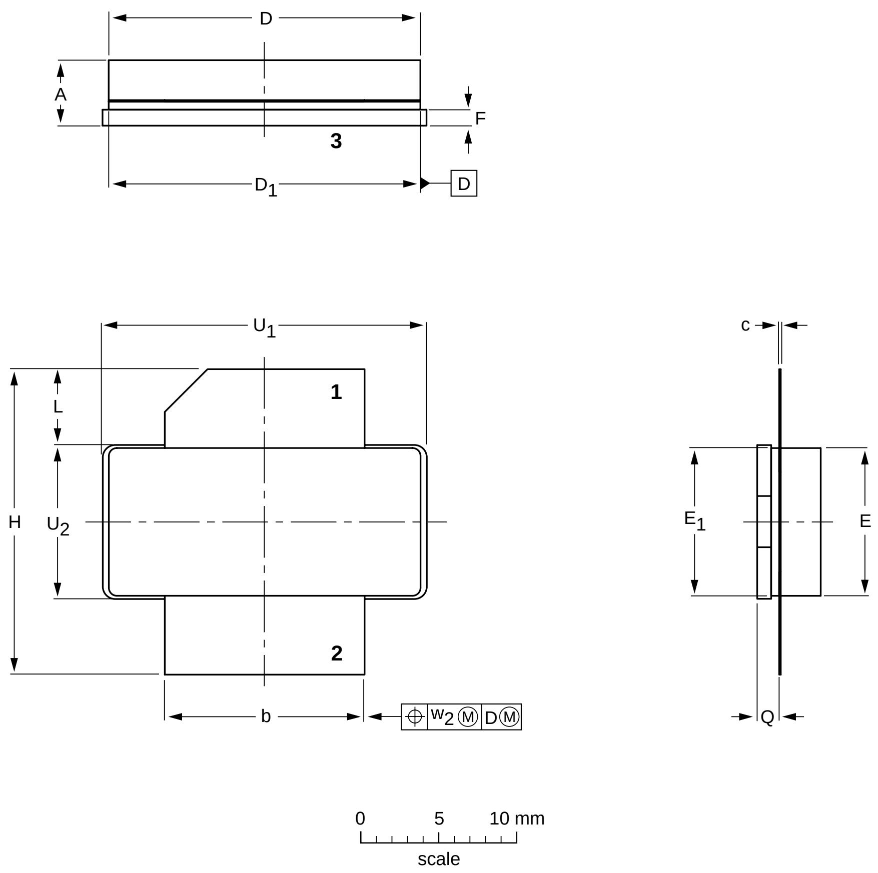
Table 8: List of components (see Figure 9 and Figure 10)

Component	Description		Value	Dimensions	Catalogue number
C1, C4, C5, C6	multilayer ceramic chip capacitor	[1]	68 pF		
C2	multilayer ceramic chip capacitor	[1]	5.1 pF		
C3	multilayer ceramic chip capacitor	[1]	3.0 pF		
C7	multilayer ceramic chip capacitor		1 μF		1812X7R105KL2AB
C8, C9	tantalum capacitor		10 μF; 35 V		
C10	Philips electrolytic capacitor		220 μF		
R1	Philips chip resistor		5.1 Ω	0603	

[1] American Technical Ceramics type 100B or capacitor of same quality.

9. Package outline

Earless flanged LDMOST ceramic package; 2 leads **SOT502B**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	E	E_1	F	H	L	Q	U_1	U_2	w_2
mm	4.72 3.43	12.83 12.57	0.15 0.08	20.02 19.61	19.96 19.66	9.50 9.30	9.53 9.25	1.14 0.89	19.94 18.92	5.33 4.32	1.70 1.45	20.70 20.45	9.91 9.65	0.25
inches	0.186 0.135	0.505 0.495	0.006 0.003	0.788 0.772	0.786 0.774	0.374 0.366	0.375 0.364	0.045 0.035	0.785 0.745	0.210 0.170	0.067 0.057	0.815 0.805	0.390 0.380	0.010

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT502B						~~99-12-28~~ 03-01-10

Fig 11. Package outline SOT502B

10. Abbreviations

Table 9: Abbreviations

Acronym	Description
CDMA	Code Division Multiple Access
CW	Continuous Wave
EDGE	Enhanced Data rates for GSM Evolution
ESR	Equivalent Series Resistance
EVM	Error Vector Magnitude
GSM	Global System for Mobile communications
I_{Dq}	quiescent drain current
LDMOS	Laterally Diffused Metal Oxide Semiconductor
PEP	Peak Envelope Power
RF	Radio Frequency
SMD	Surface Mount Device
VSWR	Voltage Standing Wave Ratio

11. Revision history

Table 10: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
BLF4G10LS-120_1	20060110	Product data sheet	-	9397 750 14547	-

12. Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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17. Contents

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