

# Instruction Set

## Data Transfer Operations

Instruction	Operation	bytes	DSP	Operands
MOV A,Rn		1	1	
MOV A,@Ri		1	2	
MOV A,direct		2	2	
MOV A,#data		2	2	
MOV Rn,A		1	1	
MOV Rn,direct		2	2	
MOV Rn,#data		2	2	
MOV direct,A		2	2	
MOV direct,Rn	move	2	2	
MOV direct,@Ri		2	2	
MOV direct,direct		3	3	
MOV direct,#data		3	3	
MOV @Ri,A		1	2	
MOV @Ri,direct		2	2	
MOV @Ri,#data		2	2	
MOV DPTR,#data16		3	3	
MOVC A,@A+DPTR	move from code memory	1	4	
MOVC A,@A+PC		1	4	
MOVC A,@Ri		1	4	
MOVC A,@DPTR	move to/from data memory	1	4	
MOVC @Ri,A		1	4	
MOVC @DPTR,A		1	4	
PUSH direct	push onto stack	2	2	
POP direct	pop from stack	2	2	
XCH A,Rn		1	1	
XCH A,@Ri	exchange bytes	1	2	
XCH A,direct		2	2	
XCHD A,@Ri	exchg low digits	1	2	

## Arithmetic Operations

Instruction	Operation	bytes	DSP	Operands
ADD A,Rn		1	1	
ADD A,@Ri	add source to A	1	2	
ADD A,direct		2	2	
ADD A,#data		2	2	
ADDC A,Rn		1	1	
ADDC A,@Ri	add with carry	1	2	
ADDC A,direct		2	2	
ADDC A,#data		2	2	
SUBB A,Rn		1	1	
SUBB A,@Ri	subtract from A	1	2	
SUBB A,direct	with borrow	2	2	
SUBB A,#data		2	2	
INC A		1	1	
INC Rn		1	1	
INC @Ri	increment	1	2	
INC direct		2	2	
INC DPTR *		1	3	
DEC A		1	1	
DEC Rn		1	1	
DEC @Ri	decrement	1	2	
DEC direct		2	2	
MUL AB	multiply A by B	1	9	
DIV AB	divide A by B	1	9	
DA A	decimal adjust	1	2	

\* INC DPTR increments the 24bit value DPP/DPH/PL

## Logical Operations

Instruction	Operation	bytes	DSP	Operands
ANL A,Rn		1	1	
ANL A,@Ri		1	2	
ANL A,direct	logical AND	2	2	
ANL A,#data		2	2	
ANL direct,A		2	2	
ANL direct,#data		3	3	
ORL A,Rn		1	1	
ORL A,@Ri		1	2	
ORL A,direct	logical OR	2	2	
ORL A,#data		2	2	
ORL direct,A		2	2	
ORL direct,#data		3	3	
XRL A,Rn		1	1	
XRL A,@Ri		1	2	
XRL A,direct	logical XOR	2	2	
XRL A,#data		2	2	
XRL direct,A		2	2	
XRL direct,#data		3	3	
CLR A	clear A to zero	1	1	
CPL A	complement A	1	1	
RL A	rotate A left	1	1	
RLC A	...through C	1	1	
RR A	rotate A right	1	1	
RRC A	...through C	1	1	
SWAP A	swap nibbles	1	1	

## Legend

Rn	register addressing using R0-R7
@Ri	indirect addressing using R0 or R1
direct	8bit internal address (00h-FFh)
#data	8bit constant included in instruction
#data16	16bit constant included in instruction
bit	8bit direct address of bit
rel	signed 8bit offset
addr11	11bit address in current 2K page
addr16	16bit address
x	any of Rn, @Ri, direct, #data

## Boolean Variable Manipulation

Instruction	Operation	bytes	DSP	Operands
CLR C	clear bit to zero	1	1	
CLR bit		2	2	
SETB C	set bit to one	1	1	
SETB bit		2	2	
CPL C	complement bit	1	1	
CPL bit		2	2	
ANL C,bit	AND bit with C	2	2	
ANL C,bit	AND (NOTbit) with C	2	2	
ORL C,bit	OR bit with C	2	2	
ORL C,bit	OR (NOTbit) with C	2	2	
MOV C,bit	move bit to bit	2	2	
MOV bit,C		2	2	

## Program Branching

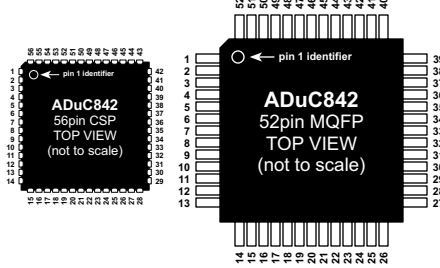
Instruction	Operation	bytes	DSP	Operands
ACALL addr11	call subroutine	2	3	
LCALL addr16		3	4	
RET	return from sub.	1	4	
RETI	return from int.	1	4	
AJMP addr11		2	3	
LJMP addr16		3	4	
SJMP rel	jump	2	3	
JMP @A+DPTR		1	3	
JC rel	jump if C set	2	3	
JNC rel	jmp if C not set	2	3	
JNB bit,rel	jump if bit set	3	4	
JNB bit,rel	jmp if bit not set	3	4	
JBC bit,rel	jmp&clear if set	3	4	
JZ rel	jump if A = 0	2	3	
JNZ rel	jump if A not 0	2	3	
CJNE A,direct,rel		3	4	
CJNE A,#data,rel	compare and jump if not equal	3	4	
CJNE Rn,#data,rel		3	4	
CJNE @Ri,#data,rel		3	4	
DJNZ Rn,rel	decrement and jump if not zero	2	3	
DJNZ direct,rel		3	4	
NOP	no operation	1	1	

## Instructions That Affect Flags

ADD A,x	C = carry out of bit 7 AC = carry out of bit 3 OV = carry out of bit 6, but not 7	DA A	C = C or (x>100)
ADDC A,x	C = carry out of bit 7 AC = carry out of bit 3 OV = carry out of bit 6, but not 7	RRC A	C = ACC.7
SUBB A,x	C = borrow into bit 7 AC = borrow into bit 3 OV = borrow into bit 6, but not 7	RLC A	C = ACC.0
MUL AB	C = 0 OV = (result>255)	SETB C	C = 1
DIV AB	C = 0 OV = divide by zero	CLR C	C = 0
		ANL C,bit	C = C and bit
		ANL C,bit	C = C and NOTbit
		ORL C,bit	C = C or bit
		ORL C,bit	C = C or NOTbit
		MOV C,bit	C = bit
		CJNE x,y,rel	C = (x<y)

# Pin Functions

Pin	Function
1	56 P1.0 / ADC0 / T2
2	1 P1.1 / ADC1 / T2EX
3	2 P1.2 / ADC2
4	3 P1.3 / ADC3
5, 4, 5	AVDD
6, 6, 7, 8	AGND
7	9 CREF
8	10 VREF
9	11 DAC0
10	12 DAC1
11	13 P1.4 / ADC4
12	14 P1.5 / ADC5 / SS
13	15 P1.6 / ADC6

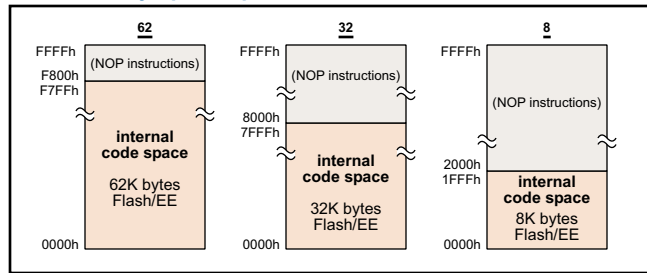


Pin	Function
14	16 P1.7 / ADC7
15	17 RESET
16	18 P3.0 / RxD
17	19 P3.1 / TxD
18	20 P3.2 / INT0
19	21 P3.3/INT1/MISO/PWM1
20	22 DVDD
21	23 DGND
22	24 P3.4 / T0 / PWM0 / PWM0 / EXTCLK
23	25 P3.5 / T1 / CONVST
24	26 P3.6 / WR
25	27 P3.7 / RD
26	28 SCLOCK

Pin	Function
27	29 SDATA / MOSI
28	30 P2.0 / A8 / A16
29	31 P2.1 / A9 / A17
30	32 P2.2 / A10 / A18
31	33 P2.3 / A11 / A19
32	34 XTAL1 (in)
33	35 XTAL2 (out)
34	36 DVDD
35	37,38 DGND
36	39 P2.4 / A12 / A20
37	40 P2.5 / A13 / A21
38	41 P2.6/A14/A22/PWM0
39	42 P2.7/A15/A23/PWM1

Pin	Function
40	43 EA
41	44 PSEN
42	45 ALE
43	46 P0.0 / AD0
44	47 P0.1 / AD1
45	48 P0.2 / AD2
46	49 P0.3 / AD3
47	50 DGND
48	51 DVDD
49	52 P0.4 / AD4
50	53 P0.5 / AD5
51	54 P0.6 / AD6
52	55 P0.7 / AD7

## Code Memory Space Options



## Interrupt Vector Addresses

Interrupt Bit	Interrupt Name	Vector Address	Relative Priority
PSMCON.5	Power Supply Monitor Interrupt	43h	1
WDS	WatchDog Timer Interrupt	5Bh	2
IE0	External Interrupt 0	03h	3
ADCI	End of ADC Conversion Interrupt	33h	4
TF0	Timer0 Overflow Interrupt	0Bh	5
IE1	External Interrupt 1	13h	6
TF1	Timer1 Overflow Interrupt	1Bh	7
ISPI/I2CI	SPI/I <sup>2</sup> C Interrupt	3Bh	8
RI/TI	UART Interrupt	23h	9
TF2/EXF2	Timer2 Interrupt	2Bh	10
TIMECON.2	Time Interval Counter Interrupt	53h	11

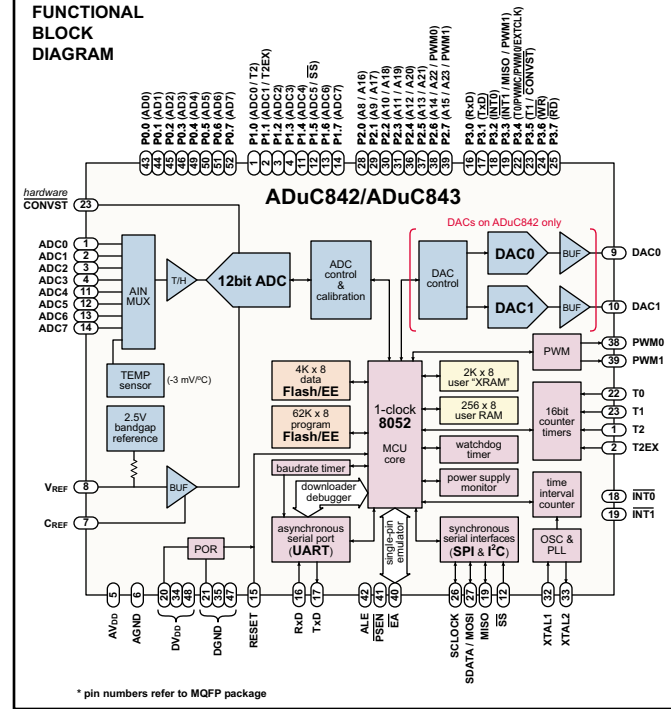
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# ADuC842/843 MicroConverter® Quick Reference Guide

## FUNCTIONAL BLOCK DIAGRAM



## A Precision Analog Flash MCU

The ADuC842/ADuC843 is:

**ADC:** 12bit, 5us, 8channel, self calibrating 0.5LSB INL & 70dB SNR

**DAC (ADuC842 only):** dual, 12bit, 15µs, voltage output <1LSB DNL

**Flash/EEPROM:** 62K bytes Flash/EE program memory 4K bytes Flash/EE data memory

**Microcontroller:** "single-cycle" 8052, up to 16.8MIPS 32 I/O lines, programmable PLL clock (131KHz to 16.8MHz with 32KHz crystal)

**Embedded Tools Support:** on-chip download/debug & single-pin emulation functions

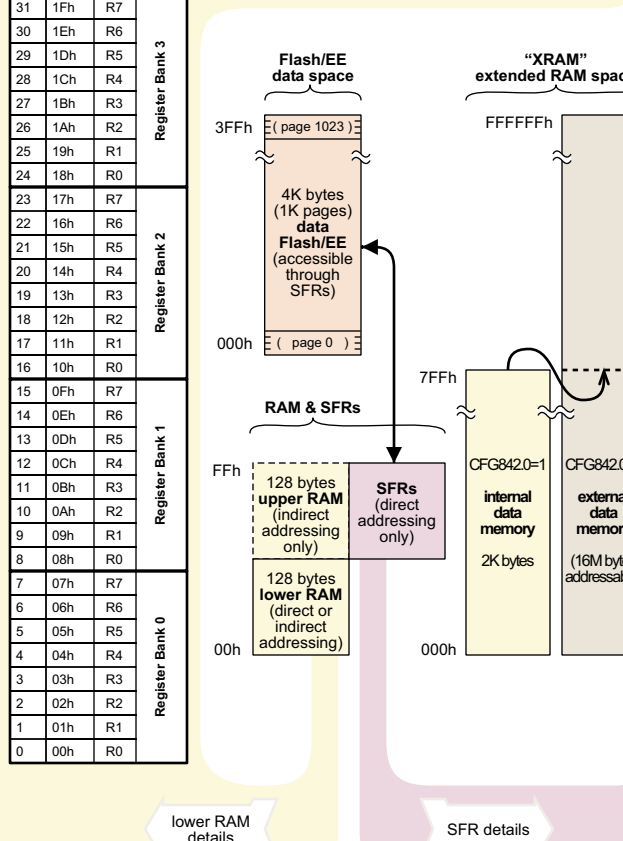
**Other on-chip features:** temperature monitor, power supply monitor, watchdog timer, flexible serial interface ports, voltage reference, time interval counter, dual 8/16bit PWM, power-on-reset



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**Data Memory: RAM, SFRs, user Flash/EE (all read/write)**

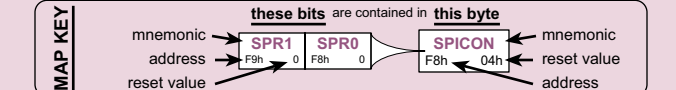
decimal address	HEX address	MSB address	LSB address
127	7Fh	7Fh	78h
...	...	...	...
48	30h	7Fh	78h
47	2Fh	7Eh	78h
46	2Eh	7Dh	78h
45	2Dh	7Ch	78h
44	2Ch	7Bh	78h
43	2Bh	7Ah	78h
42	2Ah	79h	78h
41	29h	78h	78h
40	28h	77h	78h
39	27h	76h	78h
38	26h	75h	78h
37	25h	74h	78h
36	24h	73h	78h
35	23h	72h	78h
34	22h	71h	78h
33	21h	70h	78h
32	20h	6Fh	78h
31	1Fh	6Eh	78h
30	1Eh	6Dh	78h
29	1Dh	6Ch	78h
28	1Ch	6Bh	78h
27	1Bh	6Ah	78h
26	1Ah	69h	78h
25	19h	68h	78h
24	18h	67h	78h
23	17h	66h	78h
22	16h	65h	78h
21	15h	64h	78h
20	14h	63h	78h
19	13h	62h	78h
18	12h	61h	78h
17	11h	60h	78h
16	10h	5Fh	78h
15	0Fh	5Eh	78h
14	0Eh	5Dh	78h
13	0Dh	5Ch	78h
12	0Ch	5Bh	78h
11	0Bh	5Ah	78h
10	0Ah	59h	78h
9	09h	58h	78h
8	08h	57h	78h
7	07h	56h	78h
6	06h	55h	78h
5	05h	54h	78h
4	04h	53h	78h
3	03h	52h	78h
2	02h	51h	78h
1	01h	50h	78h
0	00h	4Fh	78h



**SFR Map**

decimal address	HEX address	mnemonic	reset value
...	...	...	...
48	30h	DACCON3	00h
47	2Fh	DACCON2	00h
46	2Eh	DACCON1	00h
45	2Dh	DACCON0	00h
44	2Ch	DAC1H	00h
43	2Bh	DAC1L	00h
42	2Ah	DAC0H	00h
41	29h	DAC0L	00h
40	28h	DAC0H	00h
39	27h	DAC0L	00h
38	26h	DAC0H	00h
37	25h	DAC0L	00h
36	24h	DAC0H	00h
35	23h	DAC0L	00h
34	22h	DAC0H	00h
33	21h	DAC0L	00h
32	20h	DAC0H	00h
31	1Fh	DAC0L	00h
30	1Eh	DAC0H	00h
29	1Dh	DAC0L	00h
28	1Ch	DAC0H	00h
27	1Bh	DAC0L	00h
26	1Ah	DAC0H	00h
25	19h	DAC0L	00h
24	18h	DAC0H	00h
23	17h	DAC0L	00h
22	16h	DAC0H	00h
21	15h	DAC0L	00h
20	14h	DAC0H	00h
19	13h	DAC0L	00h
18	12h	DAC0H	00h
17	11h	DAC0L	00h
16	10h	DAC0H	00h
15	0Fh	DAC0L	00h
14	0Eh	DAC0H	00h
13	0Dh	DAC0L	00h
12	0Ch	DAC0H	00h
11	0Bh	DAC0L	00h
10	0Ah	DAC0H	00h
9	09h	DAC0L	00h
8	08h	DAC0H	00h
7	07h	DAC0L	00h
6	06h	DAC0H	00h
5	05h	DAC0L	00h
4	04h	DAC0H	00h
3	03h	DAC0L	00h
2	02h	DAC0H	00h
1	01h	DAC0L	00h
0	00h	DAC0H	00h

decimal address	HEX address	mnemonic	reset value
...	...	...	...
48	30h	DACCON3	00h
47	2Fh	DACCON2	00h
46	2Eh	DACCON1	00h
45	2Dh	DACCON0	00h
44	2Ch	DAC1H	00h
43	2Bh	DAC1L	00h
42	2Ah	DAC0H	00h
41	29h	DAC0L	00h
40	28h	DAC0H	00h
39	27h	DAC0L	00h
38	26h	DAC0H	00h
37	25h	DAC0L	00h
36	24h	DAC0H	00h
35	23h	DAC0L	00h
34	22h	DAC0H	00h
33	21h	DAC0L	00h
32	20h	DAC0H	00h
31	1Fh	DAC0L	00h
30	1Eh	DAC0H	00h
29	1Dh	DAC0L	00h
28	1Ch	DAC0H	00h
27	1Bh	DAC0L	00h
26	1Ah	DAC0H	00h
25	19h	DAC0L	00h
24	18h	DAC0H	00h
23	17h	DAC0L	00h
22	16h	DAC0H	00h
21	15h	DAC0L	00h
20	14h	DAC0H	00h
19	13h	DAC0L	00h
18	12h	DAC0H	00h
17	11h	DAC0L	00h
16	10h	DAC0H	00h
15	0Fh	DAC0L	00h
14	0Eh	DAC0H	00h
13	0Dh	DAC0L	00h
12	0Ch	DAC0H	00h
11	0Bh	DAC0L	00h
10	0Ah	DAC0H	00h
9	09h	DAC0L	00h
8	08h	DAC0H	00h
7	07h	DAC0L	00h
6	06h	DAC0H	00h
5	05h	DAC0L	00h
4	04h	DAC0H	00h
3	03h	DAC0L	00h
2	02h	DAC0H	00h
1	01h	DAC0L	00h
0	00h	DAC0H	00h



decimal address	HEX address	mnemonic	reset value
...	...	...	...
48	30h	DACCON3	00h
47	2Fh	DACCON2	00h
46	2Eh	DACCON1	00h
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44	2Ch	DAC1H	00h
43	2Bh	DAC1L	00h
42	2Ah	DAC0H	00h
41	29h	DAC0L	00h
40	28h	DAC0H	00h
39	27h	DAC0L	00h
38	26h	DAC0H	00h
37	25h	DAC0L	00h
36	24h	DAC0H	00h
35	23h	DAC0L	00h
34	22h	DAC0H	00h
33	21h	DAC0L	00h
32	20h	DAC0H	00h
31	1Fh	DAC0L	00h
30	1Eh	DAC0H	00h
29	1Dh	DAC0L	00h
28	1Ch	DAC0H	00h
27	1Bh	DAC0L	00h
26	1Ah	DAC0H	00h
25	19h	DAC0L	00h
24	18h	DAC0H	00h
23	17h	DAC0L	00h
22	16h	DAC0H	00h
21	15h	DAC0L	00h
20	14h	DAC0H	00h
19	13h	DAC0L	00h
18	12h	DAC0H	00h
17	11h	DAC0L	00h
16	10h	DAC0H	00h
15	0Fh	DAC0L	00h
14	0Eh	DAC0H	00h
13	0Dh	DAC0L	00h
12	0Ch	DAC0H	00h
11	0Bh	DAC0L	00h
10	0Ah	DAC0H	00h
9	09h	DAC0L	00h
8	08h	DAC0H	00h
7	07h	DAC0L	00h
6	06h	DAC0H	00h
5	05h	DAC0L	00h
4	04h	DAC0H	00h
3	03h	DAC0L	00h
2	02h	DAC0H	00h
1	01h	DAC0L	00h
0	00h	DAC0H	00h

\* calibration coefficients are preconfigured at power-up to factory calibrated values