Version 2.1, 19 Nov 2012

CoolSET™-F3

ICE3B0365L
ICE3A1065L
ICE3A1565L

Off-Line SMPS Current Mode Controller with integrated 650V Startup Cell/Depletion CoolMOS™ and Latched off Mode

Power Management & Supply

Never stop thinking.

Previous Version: 2.0

Page	Subjects (major changes since last revision)
22	revised outline dimension for PG-DIP-8 package

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Off-Line SMPS Current Mode Controller with integrated 650V Startup Cell/Depletion CoolMOS™ and Latched off Mode

PG-DIP-8

Product Highlights

- **Active Burst Mode to reach the lowest Standby Power Requirements < 100mW**
- **Latched Off Mode and Auto Restart Mode to increase robustness and safety of the system**
- **Adjustable Blanking Window for high load jumps to increase system reliability**
- **Pb-free lead plating DIP package; RoHS compilant**

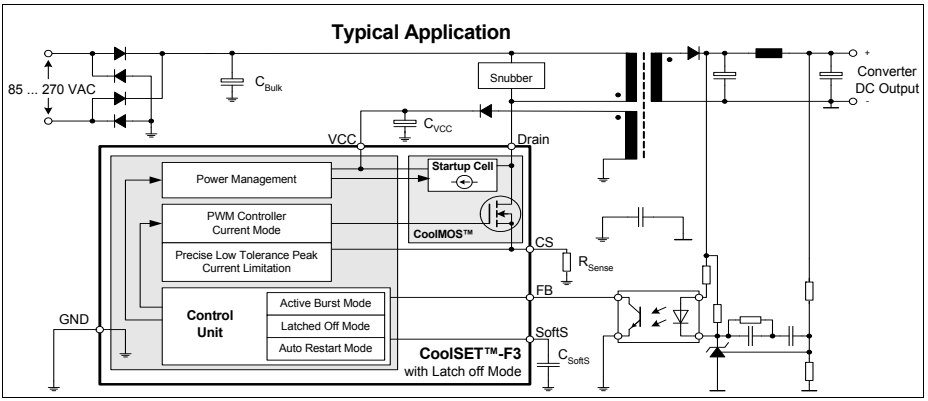
Features

- 650V avalanche rugged CoolMOS™ with built in switchable Startup Cell
- Active Burst Mode for lowest Standby Power @ light load controlled by Feedback Signal
- Fast load jump response in Active Burst Mode
- 67/100kHz internally fixed switching frequency
- Latched Off Mode for Overtemperature Detection
- Latched Off Mode for Overvoltage Detection
- Latched Off Mode for Short Winding Detection
- Auto Restart Mode for Overload and Open Loop
- Auto Restart Mode for VCC Undervoltage
- Blanking Window for short duration high current
- User defined Soft Start
- Minimum of external components required
- Max Duty Cycle 72%
- Overall tolerance of Current Limiting < ±5%
- Internal PWM Leading Edge Blanking
- Soft driving for low EMI

Description

The new generation CoolSET™-F3 Controller provides Active Burst Mode to reach the lowest Standby Power Requirements <100mW at no load. As the controller is always active during Active Burst Mode, there is an immediate response on load jumps without any black out in the SMPS. In Active Burst Mode the ripple of the output voltage can be reduced <1%. Furthermore, to increase the robustness and safety of the system, the device enters into Latched Off Mode in the cases of Overtemperature, Overvoltage or Short Winding. The Latched Off Mode can only be reset by disconnecting the main line. Auto Restart Mode is entered for cases like open loop or overload. By means of an internal precise peak current limitation, the dimension of the transformer and the secondary diode can be lowered which leads to more cost efficiency. An adjustable blanking window prevents the IC from entering Auto Restart Mode or Active Burst Mode unintentionally in case of high load jumps.

Typical Application



Type	Package	Marking	V_{DS}	F_{OSC}	R_{DSon} [1]	230VAC ±15% [2]	85-265 VAC [2]
ICE3B0365L	PG-DIP-8	ICE3B0365L	650V	67KHz	6.45	22W	10W
ICE3A1065L	PG-DIP-8	ICE3A1065L	650V	100kHz	2.95	32W	16W
ICE3A1565L	PG-DIP-8	ICE3A1565L	650V	100KHz	1.70	42W	20W

[1] typ @ T=25°C

[2] Calculated maximum input power rating at T_a=75°C, T_j=125°C and without copper area as heat sink.

Table of Contents **Page**

1 Pin Configuration and Functionality

1.1 Pin Configuration with PG-DIP-8

Pin	Symbol	Function
1	SoftS	Soft-Start
2	FB	Feedback
3	CS	Current Sense/ 650V[1] Depl. CoolMOS™ Source
4	Drain	650V[1] Depl. CoolMOS™ Drain
5	Drain	650V[1] Depl. CoolMOS™ Drain
6	n.c.	Not Connected
7	VCC	Controller Supply Voltage
8	GND	Controller Ground

[1] at T_j = 110°C

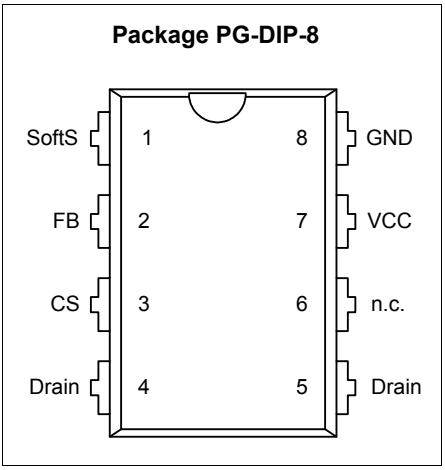


Figure 1 Pin Configuration PG-DIP-8(top view)

Note: Pin 4 and 5 are shorted within the DIP 8 package.

1.2 Pin Functionality

SoftS (Soft Start & Auto Restart Control)

The SoftS pin combines the functions of Soft Start during Start Up and error detection for Auto Restart Mode. These functions are implemented and can be adjusted by means of an external capacitor at SoftS to ground. This capacitor also provides an adjustable blanking window for high load jumps, before the IC enters into Auto Restart Mode.

FB (Feedback)

The information about the regulation is provided by the FB Pin to the internal Protection Unit and to the internal PWM-Comparator to control the duty cycle. The FB-Signal controls in case of light load the Active Burst Mode of the controller.

CS (Current Sense)

The Current Sense pin senses the voltage developed on the series resistor inserted in the source of the integrated Depl. CoolMOS™. If CS reaches the internal threshold of the Current Limit Comparator, the Driver output is immediately switched off. Furthermore the current information is provided for the PWM-Comparator to realize the Current Mode.

Drain (Drain of integrated Depl. CoolMOS™)

Pin Drain is the connection to the Drain of the internal Depl. CoolMOS™.

VCC (Power supply)

The VCC pin is the positive supply of the IC. The operating range is between 8.5V and 21V.

GND (Ground)

The GND pin is the ground of the controller.

2 Representative Blockdiagram

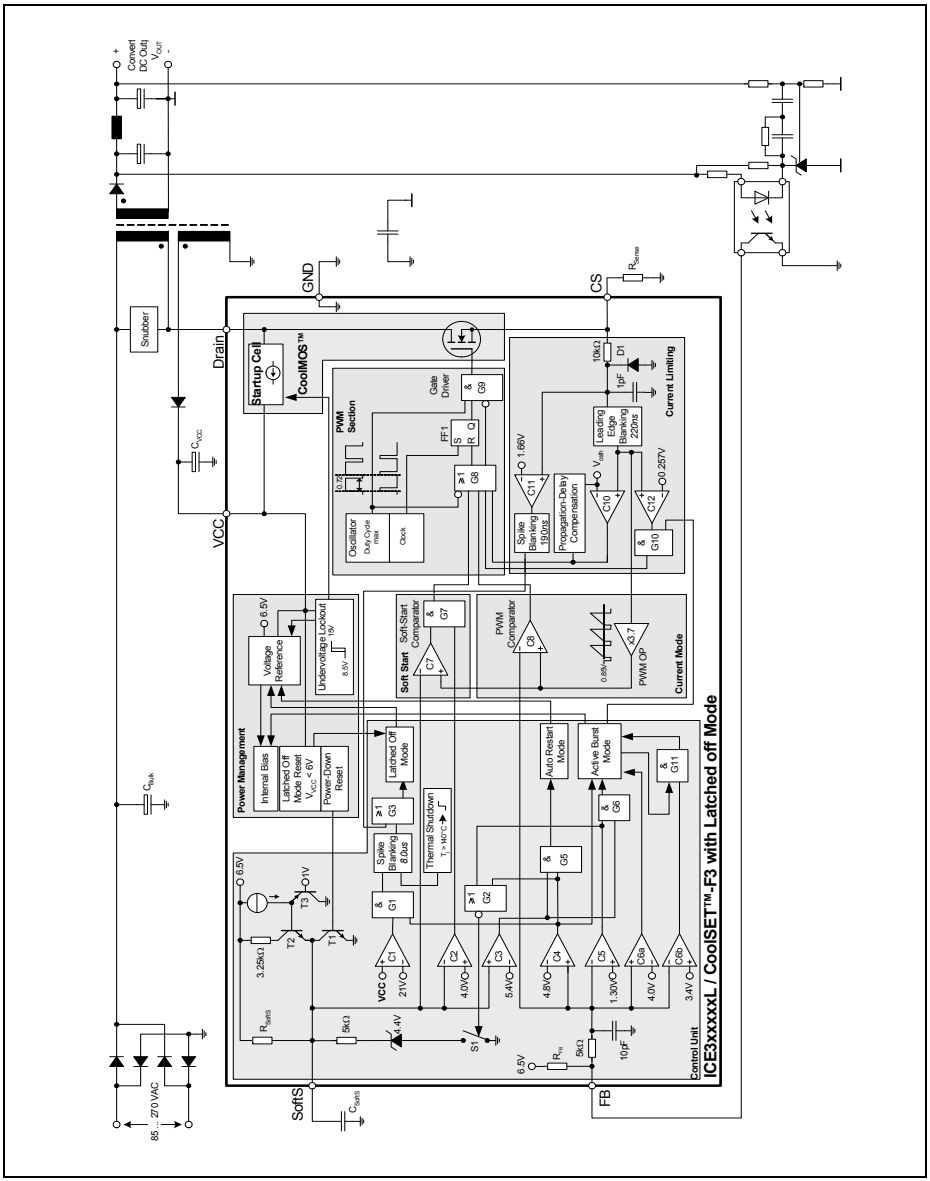


Figure 2 Representative Blockdiagram

3 Functional Description

All values which are used in the functional description are typical values. For calculating the worst cases the min/max values which can be found in section 4 Electrical Characteristics have to be considered.

3.1 Introduction

CoolSET™-F3 is the further development of the CoolSET™-F2 to meet the requirements for the lowest Standby Power at minimum load and no load conditions. A new fully integrated Standby Power concept is implemented into the IC in order to keep the application design easy. Compared to CoolSET™-F2 no further external parts are needed to achieve the lowest Standby Power. An intelligent Active Burst Mode is used for this Standby Mode. After entering this mode there is still a full control of the power conversion by the secondary side via the same optocoupler that is used for the normal PWM control. The response on load jumps is optimized. The voltage ripple on V_{out} is minimized. V_{out} is further on well controlled in this mode.

The usually external connected RC-filter in the feedback line after the optocoupler is integrated in the IC to reduce the external part count.

Furthermore a high voltage Startup Cell is integrated into the IC which is switched off once the Undervoltage Lockout on-threshold of 15V is exceeded. This Startup Cell is part of the integrated Depl. CoolMOS™. The external startup resistor is no longer necessary as this Startup Cell is connected to the Drain. Power losses are therefore reduced. This increases the efficiency under light load conditions drastically.

The Soft-Start capacitor is also used for providing an adjustable blanking window for high load jumps. During this time window the overload detection is disabled. With this concept no further external components are necessary to adjust the blanking window.

In order to increase the robustness and safety of the system, the IC provides 2 levels of protection modes: Latched Off Mode and Auto Restart Mode. The Latched Off Mode is only entered under dangerous conditions which can damage the SMPS if not switched off immediately. A restart of the system can only be done by disconnecting the AC line.

The Auto Restart Mode reduces the average power conversion to a minimum under unsafe operating conditions. This is necessary for a prolonged fault condition which could otherwise lead to a destruction of the SMPS over time. Once the malfunction is removed, normal operation is automatically initiated after the next Start Up Phase.

The internal precise peak current limitation reduces the costs for the transformer and the secondary diode. The influence of the change in the input voltage on the power limitation can be avoided together with the integrated Propagation Delay Compensation. Therefore the maximum power is nearly independent on the input voltage which is required for wide range SMPS. There is no need for an extra over-sizing of the SMPS, e.g. the transformer or the secondary diode.

3.2 Power Management

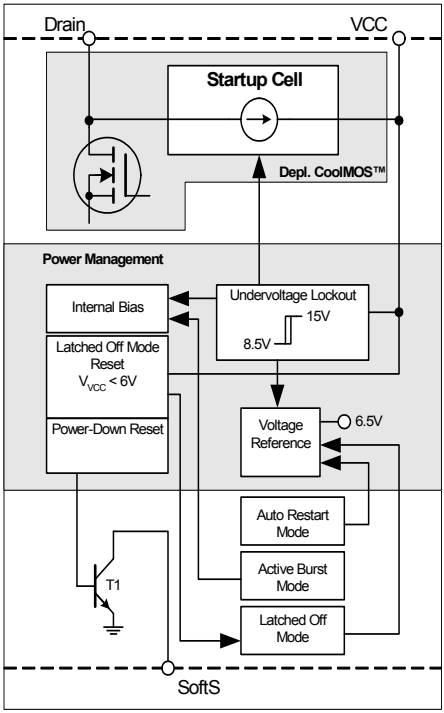


Figure 3 Power Management

The Undervoltage Lockout monitors the external supply voltage V_{VCC}. When the SMPS is plugged to the main line the internal Startup Cell is biased and starts to charge the external capacitor C_{VCC} which is connected to the VCC pin. This VCC charge current which is provided by the Startup Cell from the Drain pin is 1.05mA. When V_{VCC} exceeds the on-threshold V_{CCon}=15V the internal voltage reference and bias circuit are switched on. Then the Startup Cell is switched off by the Undervoltage Lockout and therefore no power losses present due to the connection of the Startup Cell to the Drain voltage. To avoid uncontrolled ringing at switch-on a hysteresis is implemented. The switch-off of the controller can only take place after Active Mode was entered and V_{VCC} falls below 8.5V.

The maximum current consumption before the controller is activated is about 160µA.

When V_{VCC} falls below the off-threshold V_{CCoff}=8.5V the internal reference is switched off and the Power Down reset let T1 discharging the soft-start capacitor C_{SoftS} at pin SoftS. Thus it is ensured that at every startup cycle the voltage ramp at pin SoftS starts at zero.

The internal Voltage Reference is switched off if Latched Off Mode or Auto Restart Mode is entered. The current consumption is then reduced to 300µA.

Once the malfunction condition is removed, this block will then turn back on. The recovery from Auto Restart Mode does not require disconnecting the SMPS from the AC line. In case Latched Off Mode is entered, VCC needs to be lowered below 6V to reset the Latched Off Mode. This is done usually by disconnecting the SMPS from the AC line.

When Active Burst Mode is entered the internal Bias is switched off in order to reduce the current consumption below 1.05mA while keeping the Voltage Reference still active as this is necessary in this mode.

3.3 Startup Phase

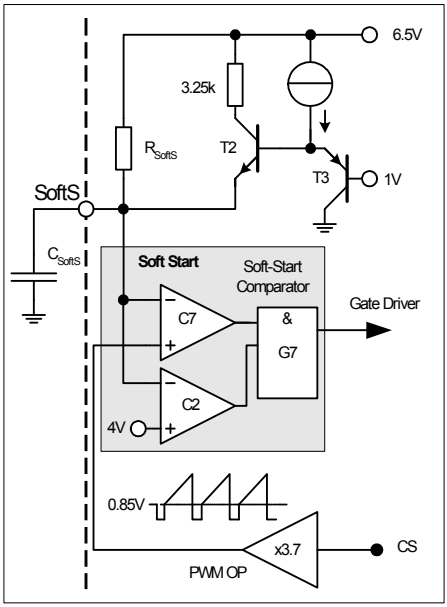


Figure 4 Soft Start

At the beginning of the Startup Phase, the IC provides a Soft Start duration whereby it controls the maximum primary current by means of a duty cycle limitation. A signal V_{SoftS} which is generated by the external capacitor C_{Softs} in combination with the internal pull up resistor R_{SoftS}, determines the duty cycle until V_{SoftS} exceeds 4V.

When the Soft Start begins, C_{SoftS} is immediately charged up to approx. 1V by T2. Therefore the Soft Start Phase takes place between 1V and 4V. Above V_{SoftsS} = 4V there is no longer duty cycle limitation DC_{max} which is controlled by comparator C7 since comparator C2 blocks the gate G7 (see Figure 4). This maximum charge current in the very first stage when V_{SoftS} is below 1V, is limited to 1.30mA.

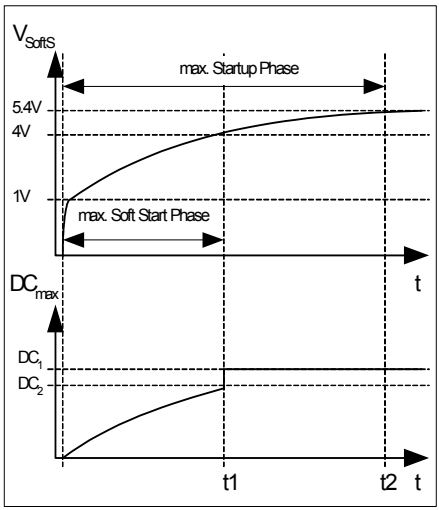


Figure 5 Startup Phase

By means of this extra charge stage, there is no delay in the beginning of the Startup Phase when there is still no switching. Furthermore Soft Start is finished at 4V to have faster the maximum power capability. The duty cycles DC_1 and DC_2 are depending on the mains and the primary inductance of the transformer. The limitation of the primary current by DC_2 is related to V_{SoftS} = 4V. But DC_1 is related to a maximum primary current which is limited by the internal Current Limiting with CS = 1V. Therefore the maximum Startup Phase is divided into a Soft Start Phase until t1 and a phase from t1 until t2 where maximum power is provided if demanded by the FB signal.

3.4 PWM Section

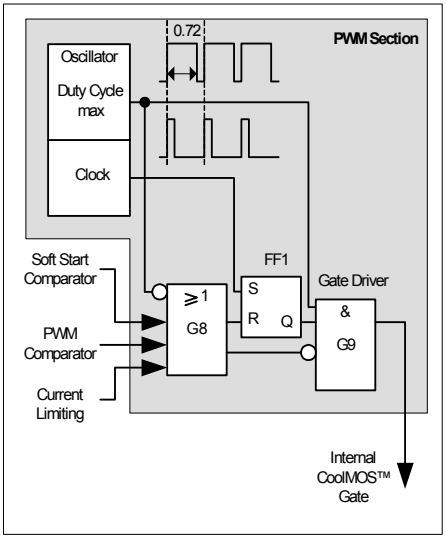


Figure 6 PWM Section Block

3.4.1 Oscillator

The oscillator generates a fixed frequency. The switching frequency for ICE3Axx65L is f_{OSC} = 100kHz and ICE3Bxx65L is f_{OSC} = 67kHz. A resistor, a capacitor and a current source and current sink which determine the frequency are integrated. The charging and discharging current of the implemented oscillator capacitor are internally trimmed, in order to achieve a very accurate switching frequency. The ratio of controlled charge to discharge current is adjusted to reach a maximum duty cycle limitation of D_{max}=0.72.

3.4.2 PWM-Latch FF1

The oscillator clock output provides a set pulse to the PWM-Latch when initiating the internal CoolMOS™ conduction. After setting the PWM-Latch can be reset by the PWM comparator, the Soft Start comparator or the Current-Limit comparator. In case of resetting, the driver is shut down immediately.

3.4.3 Gate Driver

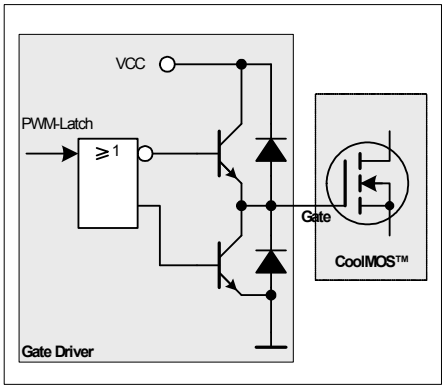


Figure 7 Gate Driver

The driver-stage is optimized to minimize EMI and to provide high circuit efficiency. This is done by reducing the switch on slope when exceeding the internal CoolMOS™ threshold. This is achieved by a slope control of the rising edge at the driver's output (see Figure 8).

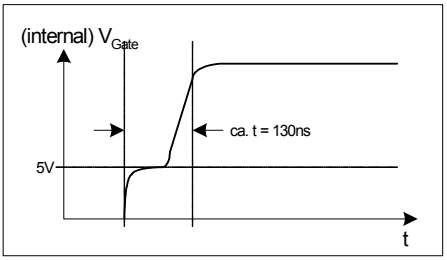


Figure 8 Gate Rising Slope

Thus the leading switch on spike is minimized. When the integrated CoolMOS™ is switched off, the falling shape of the driver is slowed down when reaching 2V to prevent an overshoot below ground. Furthermore the driver circuit is designed to eliminate cross conduction of the output stage.

During powerup when VCC is below the undervoltage lockout threshold V_{VCCoff}, the output of the Gate Driver is low to disable power transfer to the secondary side.

3.5 Current Limiting

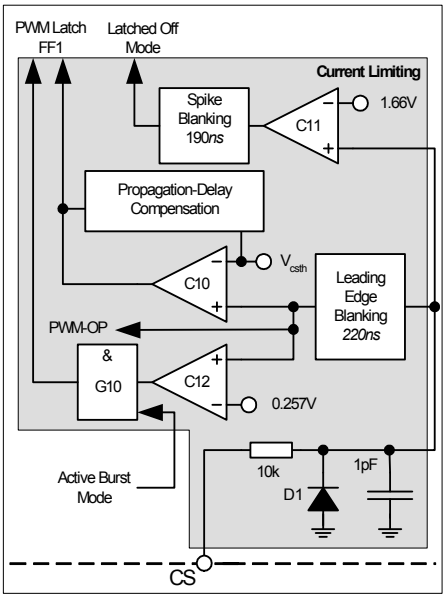


Figure 9 Current Limiting Block

There is a cycle by cycle Current Limiting realized by the Current-Limit comparator C10 to provide an overcurrent detection. The source current of the internal CoolMOS™ is sensed via an external sense resistor R_{Sense} . By means of R_{Sense} the source current is transformed to a sense voltage V_{Sense} which is fed into the pin CS. If the voltage V_{Sense} exceeds the internal threshold voltage V_{csth} the comparator C10 immediately turns off the gate drive by resetting the PWM Latch FF1. A Propagation Delay Compensation is added to support the immediate shut down without delay of the internal CoolMOS™ in case of Current Limiting. The influence of the AC input voltage on the maximum output power can thereby be avoided.

To prevent the Current Limiting from distortions caused by leading edge spikes a Leading Edge Blanking is integrated in the current sense path for the comparators C10, C12 and the PWM-OP.

The output of comparator C12 is activated by the Gate G10 if Active Burst Mode is entered. Once activated the current limiting is thereby reduced to 0.257V. This voltage level determines the power level when the Active Burst Mode is left if there is a higher power demand.

A further comparator C11 is implemented to detect dangerous current levels which could occur if there is a short winding in the transformer or the secondary diode is shorten. To ensure that there is no accidentally entering of the Latched Mode by the comparator C11 a spike blanking with 190ns is integrated in the output path of comparator C11.

3.5.1 Leading Edge Blanking

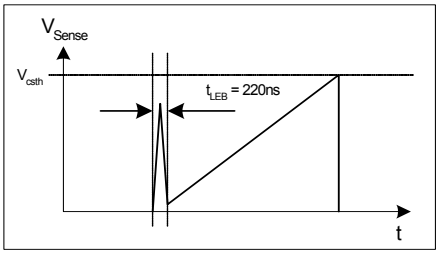


Figure 10 Leading Edge Blanking

Each time when the internal CoolMOS™ is switched on, a leading edge spike is generated due to the primary-side capacitances and secondary-side rectifier reverse recovery time. This spike can cause the gate drive to switch off unintentionally. To avoid a premature termination of the switching pulse, this spike is blanked out with a time constant of t_{LEB} = 220ns. During this time, the gate drive will not be switched off.

3.5.2 Propagation Delay Compensation

In case of overcurrent detection, the switch-off of the internal CoolMOS™ is delayed due to the propagation delay of the circuit. This delay causes an overshoot of the peak current I_{peak} which depends on the ratio of dI/dt of the peak current (see Figure 11).

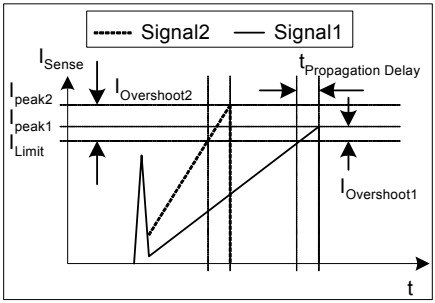


Figure 11 Current Limiting

The overshoot of Signal2 is bigger than of Signal1 due to the steeper rising waveform. This change in the slope is depending on the AC input voltage. Propagation Delay Compensation is integrated to limit the overshoot dependency on dI/dt of the rising primary

current. That means the propagation delay time between exceeding the current sense threshold V_{csth} and the switch off of the internal CoolMOS™ is compensated over temperature within a wide range. Current Limiting is now possible in a very accurate way.

E.g. I_{peak} = 0.5A with R_{Sense} = 2. Without Propagation Delay Compensation the current sense threshold is set to a static voltage level V_{csth}=1V. A current ramp of dI/dt = 0.4A/µs, that means dV_{Sense}/dt = 0.8V/µs, and a propagation delay time of i.e. $t_{Propagation\ Delay}$ =180ns leads then to an I_{peak} overshoot of 14.4%. By means of propagation delay compensation the overshoot is only about 2% (see Figure 12).

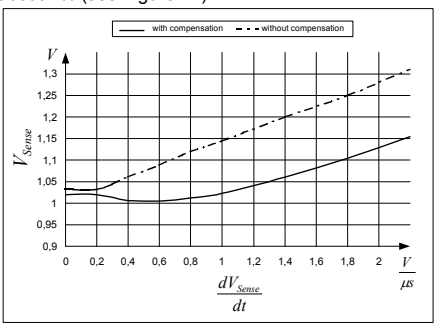


Figure 12 Overcurrent Shutdown

The Propagation Delay Compensation is realized by means of a dynamic threshold voltage V_{csth} (see Figure 13). In case of a steeper slope the switch off of the driver is earlier to compensate the delay.

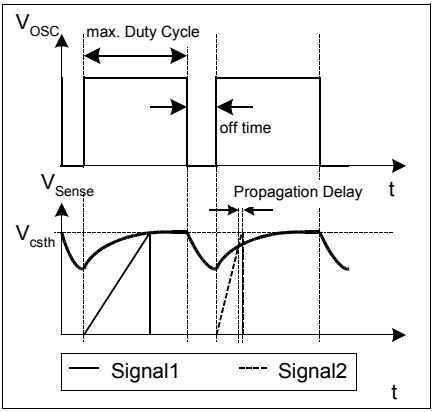


Figure 13 Dynamic Voltage Threshold V_{csth}

3.6 Control Unit

The Control Unit contains the functions for Active Burst Mode, Auto Restart Mode and Latched Off Mode. The Active Burst Mode and the Auto Restart Mode are combined with an Adjustable Blanking Window which is depending on the external Soft Start capacitor. By means of this Adjustable Blanking Window, the IC avoids entering into these two modes accidentally. Furthermore it also provides a certain time whereby the overload detection is delayed. This delay is useful for applications which normally works with a low current and occasionally require a short duration of high current.

3.6.1 Adjustable Blanking Window

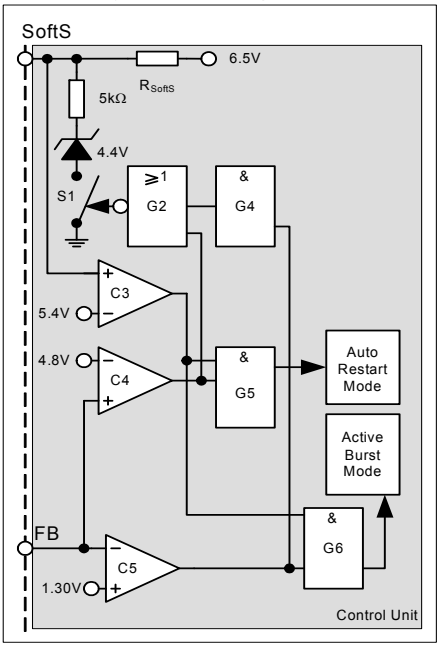


Figure 14 Adjustable Blanking Window

V_{SoftS} is clamped at 4.4V by the closed switch S1 after the SMPS is settled. If overload occurs V_{FB} is exceeding 4.8V. Auto Restart Mode can't be entered as the gate G5 is still blocked by the comparator C3. But after V_{FB} has exceeded 4.8V the switch S1 is opened via the gate G2. The external Soft Start capacitor can now be charged further by the integrated pull up resistor R_{SoftS}. The comparator C3 releases the gates G5 and G6 once V_{Softs} has exceeded 5.4V. Therefore there is no entering of Auto Restart Mode possible during this charging time of the external capacitor

C_{SoftS}. The same procedure happens to the external Soft Start capacitor if a low load condition is detected by comparator C5 when V_{FB} is falling below 1.30V. Only after V_{SoftS} has exceeded 5.4V and V_{FB} is still below 1.30V Active Burst Mode is entered.

3.6.2 Active Burst Mode

The controller provides Active Burst Mode for low load conditions at V_{OUT}. Active Burst Mode increases significantly the efficiency at light load conditions while supporting a low ripple on V_{OUT} and fast response on load jumps. During Active Burst Mode which is controlled only by the FB signal the IC is always active and can therefore immediately response on fast changes at the FB signal. The Startup Cell is kept switched off to avoid increased power losses for the self supply.

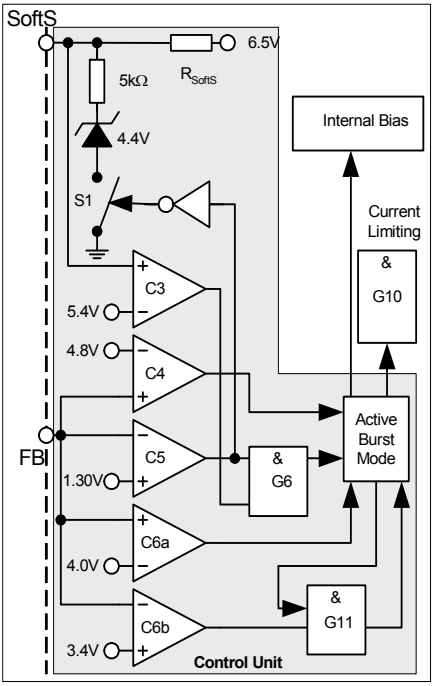


Figure 15 Active Burst Mode

The Active Burst Mode is located in the Control Unit. Figure 15 shows the related components.

3.6.2.1 Entering Active Burst Mode

The FB signal is always observed by the comparator C5 if the voltage level falls below 1.30V. In that case the switch S1 is released which allows the capacitor C_{SoftS} to be charged starting from the clamped voltage level at 4.4V in normal operating mode. If V_{SoftS} exceeds 5.4V the comparator C3 releases the gate G6 to enter the Active Burst Mode. The time window that is generated by combining the FB and SoftS signals with gate G6 avoids a sudden entering of the Active Burst Mode due to large load jumps. This time window can be adjusted by the external capacitor C_{SoftS}.

After entering Active Burst Mode a burst flag is set and the internal bias is switched off in order to reduce the current consumption of the IC down to approx. 1.05mA. In this Off State Phase the IC is no longer self supplied so that therefore C_{VCC} has to provide the VCC current (see Figure 16). Furthermore gate G11 is then released to start the next burst cycle once V_{FB} has 3.4V exceeded.

It has to be ensured by the application that the VCC remains above the Undervoltage Lockout Level of 8.5V to avoid that the Startup Cell is accidentally switched on. Otherwise power losses are significantly increased. The minimum VCC level during Active Burst Mode is depending on the load conditions and the application. The lowest VCC level is reached at no load conditions at V_{OUT}.

3.6.2.2 Working in Active Burst Mode

After entering the Active Burst Mode the FB voltage rises as V_{OUT} starts to decrease due to the inactive PWM section. Comparator C6a observes the FB signal if the voltage level 4V is exceeded. In that case the internal circuit is again activated by the internal Bias to start with switching. As now in Active Burst Mode the gate G10 is released the current limit is only 0.257V to reduce the conduction losses and to avoid audible noise. If the load at V_{OUT} is still below the starting level for the Active Burst Mode the FB signal decreases down to 3.4V. At this level C6b deactivates again the internal circuit by switching off the internal Bias. The gate G11 is released as after entering Active Burst Mode the burst flag is set. If working in Active Burst Mode the FB voltage is changing like a saw tooth between 3.4V and 4V (see Figure 16).

3.6.2.3 Leaving Active Burst Mode

The FB voltage immediately increases if there is a high load jump. This is observed by comparator C4. As the current limit is ca. 26% during Active Burst Mode a certain load jump is needed that FB can exceed 4.8V. At this time C4 resets the Active Burst Mode which also

blocks C12 by the gate G10. Maximum current can now be provided to stabilize V_{OUT}.

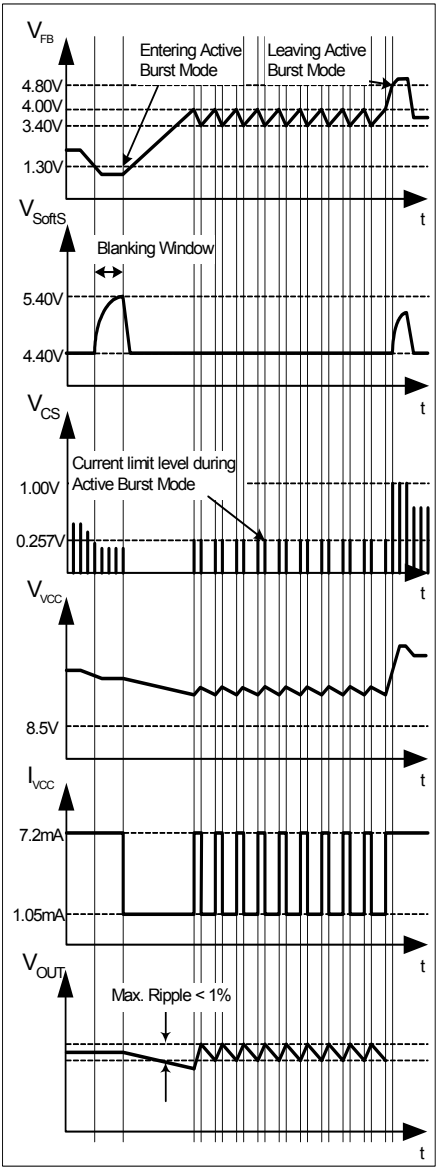


Figure 16 Signals in Active Burst Mode

3.6.3 Protection Modes

The IC provides several protection features which are separated into two categories. Some enter Latched Off Mode, the others enter Auto Restart Mode. The Latched Off Mode can only be reset if VCC is falling below 6V. Both modes prevent the SMPS from destructive states. The following table shows the relationship between possible system failures and the chosen protection modes.

VCC Overvoltage	Latched Off Mode
Overtemperature	Latched Off Mode
Short Winding/Short Diode	Latched Off Mode
Overload	Auto Restart Mode
Open Loop	Auto Restart Mode
VCC Undervoltage	Auto Restart Mode
Short Optocoupler	Auto Restart Mode

3.6.3.1 Latched Off Mode

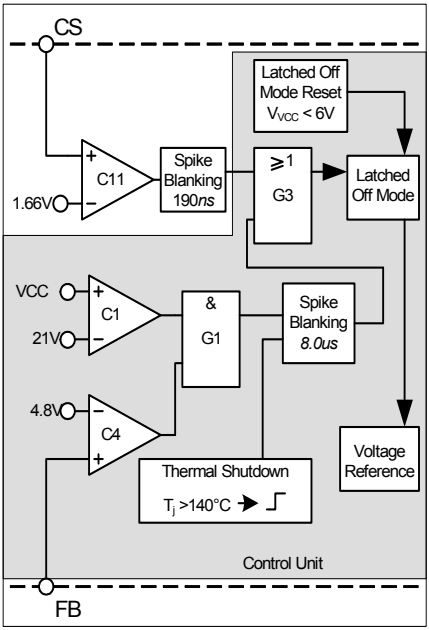


Figure 17 Latched Off Mode

The VCC voltage is observed by comparator C1 if 21V is exceeded. The output of C1 is combined with the output of C4 which observes FB signal if 4.8V is

exceeded. Therefore the overvoltage detection is only activated if the FB signal is outside the operating range > 4.8V, e.g. when Open Loop happens. This means any small voltage overshoots of V_{VCC} during normal operating can not start the Latched Off Mode.

The internal Voltage Reference is switched off once Latched Off Mode is entered in order to reduce the current consumption of the IC as much as possible. Latched Off Mode can only be reset by decreasing V_{VCC} < 6V. In this stage, only the UVLO is working which controls the Startup Cell by switching on/off at V_{VCCon}/V_{VCCoff}. During this phase, the average current consumption is only 300µA. As there is no longer a self-supply by the auxiliary winding, VCC drops. The Undervoltage Lockout switches on the integrated Startup Cell when VCC falls below 8.5V. The Startup Cell is switched off again when VCC has exceeded 15V. Once the Latched Off Mode was entered, there is no Start Up Phase after VCC has exceeded the switch-on level of the Undervoltage Lockout. Therefore VCC changes between the switch-on and switch-off levels of the Undervoltage Lockout with a saw tooth shape (see Figure 18).

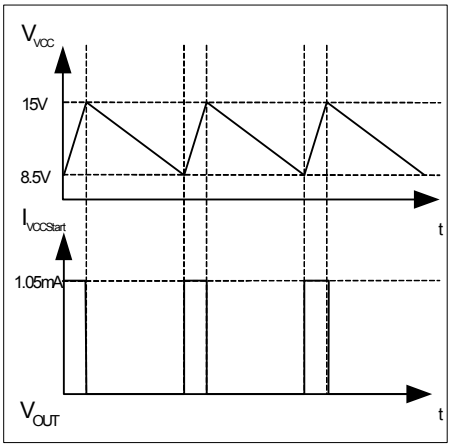


Figure 18 Signals in Latched Off Mode

The Thermal Shutdown block monitors the junction temperature of the IC. After detecting a junction temperature higher than 140°C, Latched Off Mode is entered.

The signals coming from the temperature detection and VCC overvoltage detection are fed into a spike blanking with a time constant of 8.0µs to ensure system reliability.

Furthermore, a short winding or short diode on the secondary side can be detected by the comparator C11 which is in parallel to the propagation delay compensated current limit comparator C10. In normal operating mode comparator C10 keeps the maximum level of the CS signal at 1V. If there is a failure such as short winding or short diode, C10 is no longer able to limit the CS signal at 1V. C11 detects then the over current and enters immediately the Latched Off Mode to keep the SMPS in a safe stage.

3.6.3.2 Auto Restart Mode

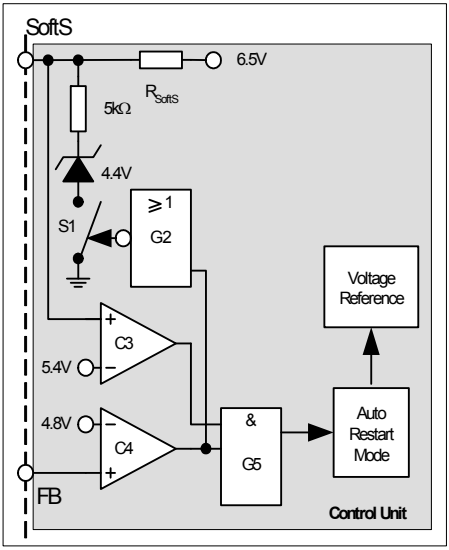


Figure 19 Auto Restart Mode

In case of Overload or Open Loop, FB exceeds 4.8V which will be observed by C4. At this time S1 is released that V_{SoftS} can increase. If V_{SoftS} exceeds 5.4V which is observed by C3, Auto Restart Mode is entered as both inputs of the gate G5 are high. In combining the FB and SoftS signals, there is a blanking window generated which prevents the system to enter Auto Restart Mode due to large load jumps. This time window is the same as for the Active Burst Mode and can therefore be adjusted by the external C_{SoftS}.

In case of VCC undervoltage, the IC enters into the Auto Restart Mode and starts a new startup cycle.

Short Optocoupler also leads to VCC undervoltage as there is no self supply after activating the internal reference and bias.

In contrast to the Latched Off Mode, there is always a Startup Phase with switching cycles in Auto Restart Mode. After this Start Up Phase, the conditions are again checked whether the failure mode is still present. Normal operation is resumed once the failure mode is removed that had caused the Auto Restart Mode.

4 Electrical Characteristics

Note: All voltages are measured with respect to ground (Pin 8). The voltage levels are valid if other ratings are not violated.

4.1 Absolute Maximum Ratings

Note: Absolute maximum ratings are defined as ratings, which when being exceeded may lead to destruction of the integrated circuit. For the same reason make sure, that any capacitor that will be connected to pin 7 (VCC) is discharged before assembling the application circuit.

Parameter		Symbol	Limit Values		Unit	Remarks
			min.	max.		
Drain Source Voltage		V_{DS}	-	650	V	T_j=110°C
Pulse drain current, t_p limited by T_{jmax}	ICE3B0365L	I_{D_Puls1}	-	1.6	A	
	ICE3A1065L	I_{D_Puls2}	-	3.4	A	
	ICE3A1565L	I_{D_Puls3}	-	6.1	A	
Avalanche energy, repetitive t_{AR} limited by max. T_j=150°C[1]	ICE3B0365L	E_{AR1}	-	0.005	mJ	
	ICE3A1065L	E_{AR2}	-	0.07	mJ	
	ICE3A1565L	E_{AR3}	-	0.15	mJ	
Avalanche current, repetitive t_{AR} limited by max. T_j=150°C	ICE3B0365L	I_{AR1}	-	0.3	A	
	ICE3A1065L	I_{AR2}	-	1.0	A	
	ICE3A1565L	I_{AR3}	-	1.5	A	
VCC Supply Voltage		V_{VCC}	-0.3	22	V	
FB Voltage		V_{FB}	-0.3	6.5	V	
SoftS Voltage		V_{SoftS}	-0.3	6.5	V	
CS Voltage		V_{CS}	-0.3	6.5	V	
Junction Temperature		T_j	-40	150	°C	
Storage Temperature		T_S	-55	150	°C	
Thermal Resistance Junction -Ambient		R_{thJA}	-	90	K/W	PG-DIP-8
ESD Capability(incl. Drain Pin)		V_{ESD}	-	3	kV	Human body model[2]

[1] Repetitive avalanche causes additional power losses that can be calculated as $P_{AV}=E_{AR}*f$

[2] According to EIA/JESD22-A114-B (discharging a 100pF capacitor through a 1.5kΩ series resistor)

4.2 Operating Range

Note: Within the operating range the IC operates as described in the functional description.

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
VCC Supply Voltage	V_{VCC}	V_{VCCoff}	20	V	
Junction Temperature of Controller	T_{jCon}	-25	130	°C	Max value limited due to thermal shut down of controller
Junction Temperature of CoolMOS™	$T_{jCoolMOS}$	-25	150	°C	

4.3 Characteristics

4.3.1 Supply Section

Note: The electrical characteristics involve the spread of values within the specified supply voltage and junction temperature range T_J from – 25 °C to 130 °C. Typical values represent the median values, which are related to 25°C. If not otherwise stated, a supply voltage of V_{CC} = 15 V is assumed.

Parameter		Symbol	Limit Values			Unit	Test Condition
			min.	typ.	max.		
Start Up Current		$I_{VCCstart}$	-	160	220	µA	V_{VCC} =14V
VCC Charge Current		$I_{VCCcharge1}$	0.55	1.05	1.60	mA	V_{VCC} = 0V
		$I_{VCCcharge2}$	-	0.88	-	mA	V_{VCC} =14V
Leakage Current of Start Up Cell and CoolMOS™		$I_{StartLeak}$	-	0.2	50	µA	V_{VCC}=16V, V_{Drain} = 450V at T_j=100°C
Supply Current with Inactive Gate		I_{VCCsup_ng}	-	5.5	7.0	mA	
Supply Current with Active Gate	ICE3B0365L	I_{VCCsup_g1}	-	5.5	7.0	mA	V_{SoftS} = 4.4V I_{FB} = 0,
	ICE3A1065L	I_{VCCsup_g2}	-	5.9	7.5	mA	
	ICE3A1565L	I_{VCCsup_g3}	-	6.3	8.0	mA	
Supply Current in Latched Off Mode		$I_{VCClatch}$	-	300	-	µA	I_{FB} = 0 I_{Softs} = 0
Supply Current in Auto Restart Mode with Inactive Gate		$I_{VCCrestart}$	-	300	-	µA	I_{FB} = 0 I_{Softs} = 0
Supply Current in Active Burst Mode with Inactive Gate		$I_{VCCburst1}$	-	1.05	1.25	mA	V_{VCC} =15V V_{FB} = 3.7V, V_{SoftS} = 4.4V
		$I_{VCCburst2}$	-	0.95	1.15	mA	V_{VCC} = 9.5V V_{FB} = 3.7V, V_{SoftS} = 4.4V
VCC Turn-On Threshold VCC Turn-Off Threshold VCC Turn-On/Off Hysteresis		V_{VCCon} V_{VCCoff} V_{VCChys}	14.2 8.0 -	15.0 8.5 6.5	15.8 9.0 -	V V V	

4.3.2 Internal Voltage Reference

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Trimmed Reference Voltage	V_{REF}	6.37	6.50	6.63	V	measured at pin FB I_{FB} = 0

4.3.3 PWM Section

Parameter		Symbol	Limit Values			Unit	Test Condition
			min.	typ.	max.		
Fixed Oscillator Frequency	ICE3Axx65L	f_{OSC_A1}	92	100	108	kHz	
		f_{OSC_A2}	94	100	106	kHz	T_j = 25°C
Fixed Oscillator Frequency	ICE3Bxx65L	f_{OSC_B1}	61	67	73	kHz	
		f_{OSC_B2}	63	67	71	kHz	T_j = 25°C
Max. Duty Cycle		D_{max}	0.67	0.72	0.77		
Min. Duty Cycle		D_{min}	0	-	-		V_{FB} < 0.3V
PWM-OP Gain		A_V	3.5	3.7	3.9		
Voltage Ramp Max Level		$V_{Max\text{-}Ramp}$	-	0.85	-	V	
V_{FB} Operating Range Min Level		V_{FBmin}	0.3	0.7	-	V	
V_{FB} Operating Range Max level		V_{FBmax}	-	-	4.75	V	CS=1V, limited by Comparator C4[1)]
FB Pull-Up Resistor		R_{FB}	16	20	27	kΩ	
SoftS Pull-Up Resistor		R_{SoftS}	39	50	62	kΩ	

1) The parameter is not subjected to production test - verified by design/characterization

4.3.4 Control Unit

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Deactivation Level for SoftS Comparator C7 by C2	$V_{SoftSC2}$	3.85	4.00	4.15	V	V_{FB} > 5V
Clamped V_{SoftS} Voltage during Normal Operating Mode	$V_{SoftSclmp}$	4.23	4.40	4.57	V	V_{FB} = 4V
Activation Limit of Comparator C3	$V_{SoftSC3}$	5.20	5.40	5.60	V	V_{FB} > 5V
SoftS Startup Current	$I_{SoftSstart}$	-	1.3	-	mA	V_{SoftS} = 0V
Over Load & Open Loop Detection Limit for Comparator C4	V_{FBC4}	4.62	4.80	4.98	V	V_{SoftS} > 5.6V
Active Burst Mode Level for Comparator C5	V_{FBC5}	1.23	1.30	1.37	V	V_{SoftS} > 5.6V
Active Burst Mode Level for Comparator C6a	V_{FBC6a}	3.85	4.00	4.15	V	After Active Burst Mode is entered
Active Burst Mode Level for Comparator C6b	V_{FBC6b}	3.25	3.40	3.55	V	After Active Burst Mode is entered
Overvoltage Detection Limit	V_{VCCOVP}	20	21	22	V	V_{FB} > 5V
Latched Thermal Shutdown[1)]	T_{jSD}	130	140	150	°C	
Spike Blanking	t_{Spike}	-	8.0	-	µs	
Power Down Reset for Latched Mode	V_{VCCPD}	4.0	6.0	7.5	V	After Latched Off Mode is entered

[1)] The parameter is not subjected to production test - verified by design/characterization

Note: The trend of all the voltage levels in the Control Unit is the same regarding the deviation except V_{VCCOVP} *and* V_{VCCPD}

4.3.5 Current Limiting

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Peak Current Limitation (incl. Propagation Delay)	V_{csth}	0.97	1.02	1.07	V	dV_{sense} / dt = 0.6V/µs (see Figure 12)
Peak Current Limitation during Active Burst Mode	V_{CS2}	0.232	0.257	0.282	V	
Leading Edge Blanking	t_{LEB}	-	220	-	ns	V_{SoftS} = 4.4V
CS Input Bias Current	I_{CSbias}	-1.0	-0.2	0	µA	V_{CS} =0V
Over Current Detection for Latched Off Mode	V_{CS1}	1.570	1.66	1.764	V	
CS Spike Blanking for Comparator C11	$t_{CSspike}$	-	190	-	ns	

4.3.6 CoolMOS™ Section

Parameter		Symbol	Limit Values			Unit	Test Condition
			min.	typ.	max.		
Drain Source Breakdown Voltage		$V_{(BR)DSS}$	600 650	- -	- -	V V	T_j = 25°C T_j = 110°C
Drain Source On-Resistance	ICE3B0365L	R_{DSon1}	- -	6.45 13.7	7.50 17.0	Ω Ω	T_j = 25°C T_j=125°C[1)] at I_D = 0.3A
	ICE3A1065L	R_{DSon2}	- -	2.95 6.60	3.42 7.56	Ω Ω	T_j = 25°C T_j=125°C[1)] at I_D = 1.0A
	ICE3A1565L	R_{DSon3}	- -	1.70 3.57	1.96 4.12	Ω Ω	T_j = 25°C T_j=125°C[1)] at I_D = 1.5A
Effective output capacitance, energy related	ICE3B0365L	$C_{o(er)1}$	-	3.65	-	pF	V_{DS} = 0V to 480V
	ICE3A1065L	$C_{o(er)2}$	-	7.0	-	pF	
	ICE3A1565L	$C_{o(er)3}$	-	11.63	-	pF	
Rise Time		t_{rise}	-	30[2)]	-	ns	
Fall Time		t_{fall}	-	30[2)]	-	ns	

1) The parameter is not subjected to production test - verified by design/characterization

2) Measured in a Typical Flyback Converter Application

5 Temperature derating curve

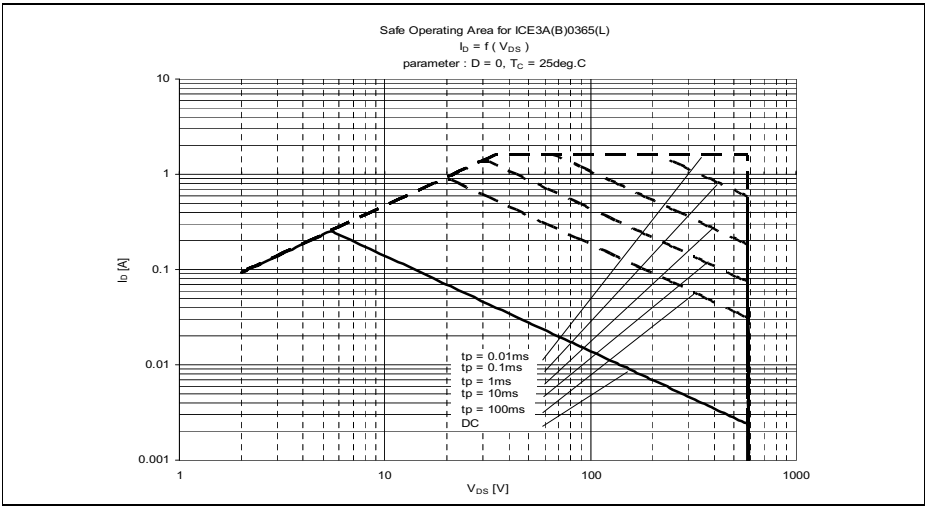


Figure 20 Safe Operating area (SOA) curve for ICE3B03065L

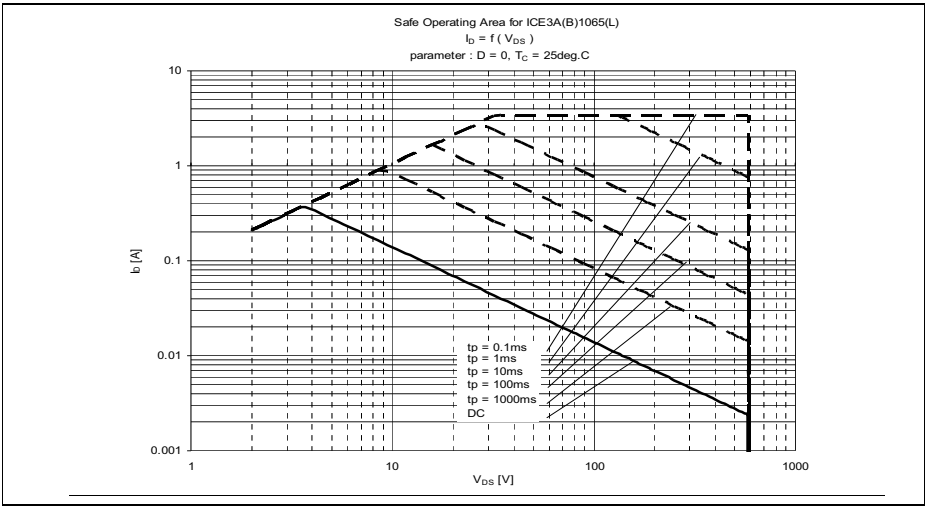


Figure 21 Safe Operating area (SOA) curve for ICE3A1065L

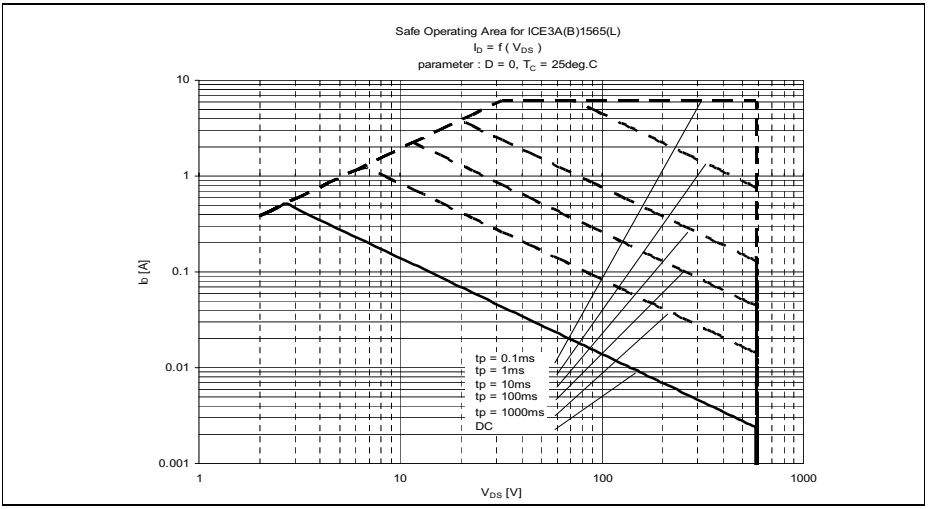


Figure 22 Safe Operating area (SOA) curve for ICE3A1565L

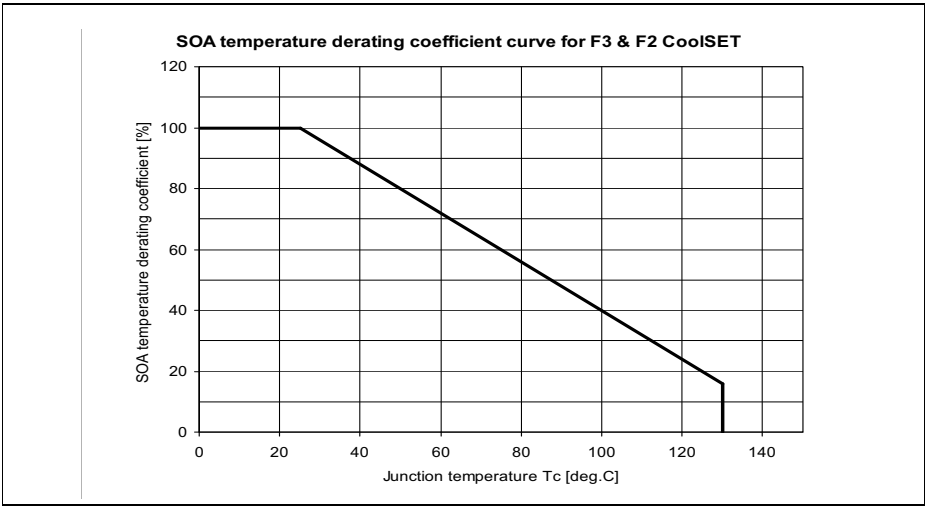
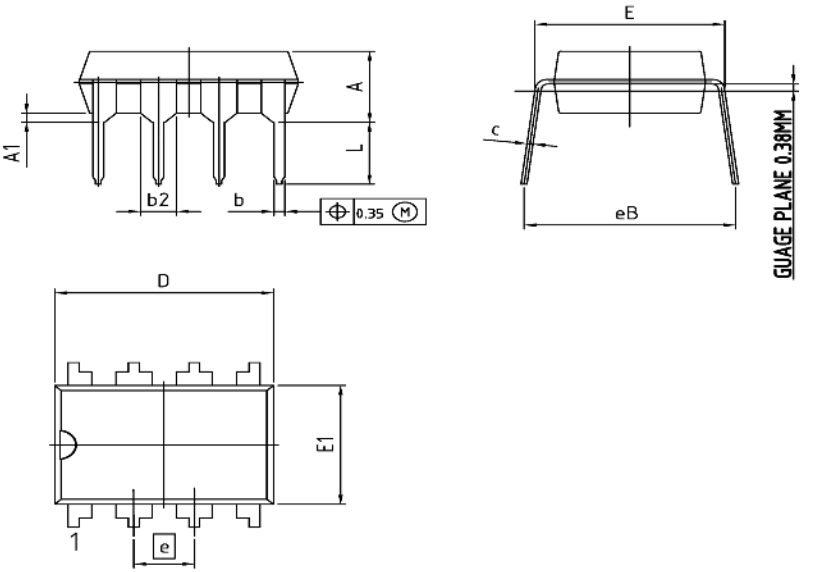


Figure 23 SOA temperature derating coefficient curve

6 Outline Dimension

PG-DIP-8
(Plastic Dual In-Line Outline)



1) DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	-	4.80	-	0.189
A1	0.38	-	0.015	-
b	0.36	0.56	0.014	0.022
b2	-	1.70	-	0.067
c	0.15	0.36	0.006	0.014
D	9.10	9.77	0.358	0.385
E	7.49	8.26	0.295	0.325
E1	6.10	6.60	0.240	0.260
e	2.54 BSC		0.1 BSC	
N	8		8	
eB	7.90	9.90	0.311	0.390
L	3.00	-	0.118	-

DOCUMENT NO.
Z8B00155363

SCALE 0 1.0 0 1.0 2mm

EUROPEAN PROJECTION

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REVISION
02

Figure 24 PG-DIP-8 (Pb-free lead plating Platic Dual-in-Line Outline)

7 Marking

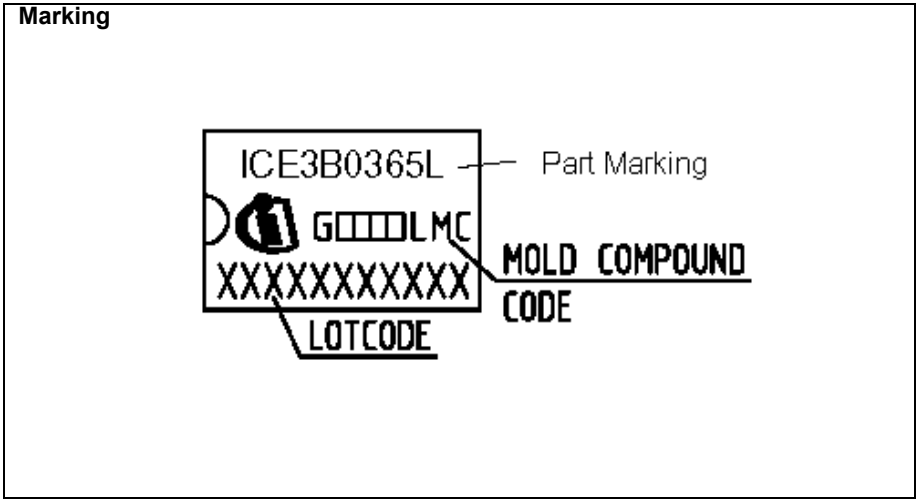

Figure 25 Marking for ICE3B0365L

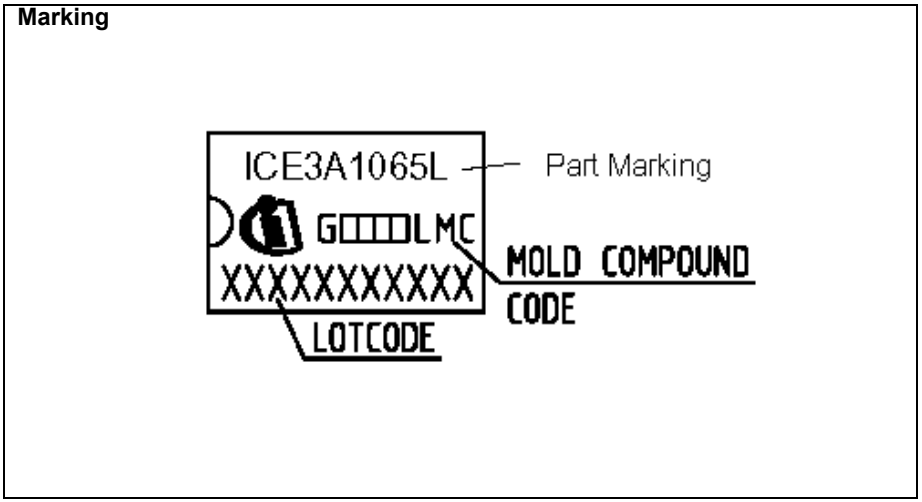

Figure 26 Marking for ICE3A1065L

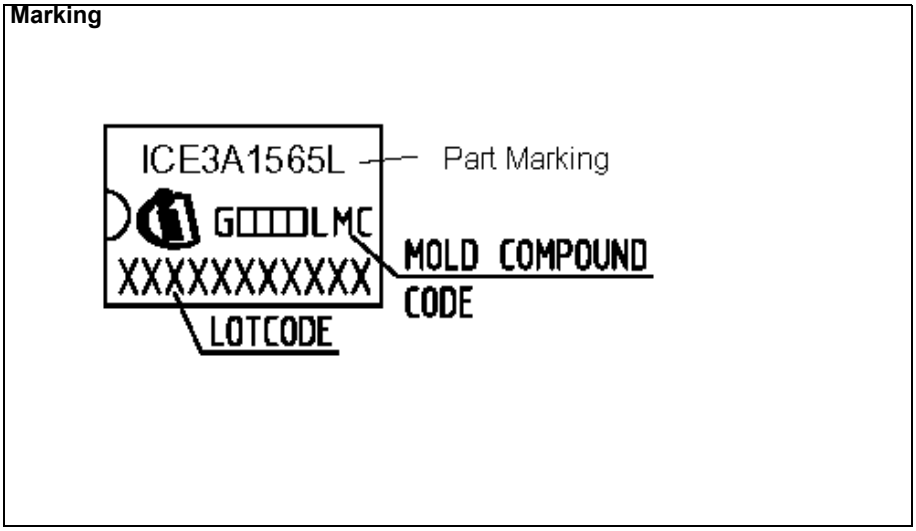

Figure 27 Marking for ICE3A1565L

8 Schematic for recommended PCB layout

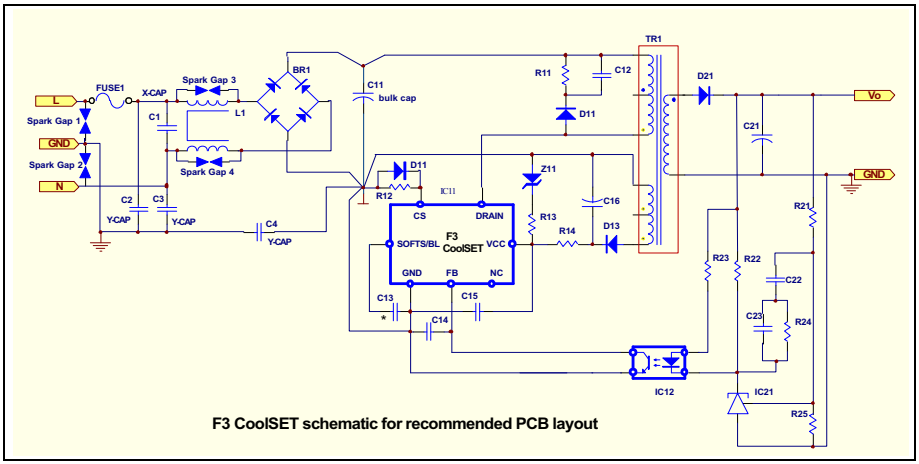

Figure 28 Schematic for recommended PCB layout

General guideline for PCB layout design using F3 CoolSET (refer to Figure 28):

1. “Star Ground “at bulk capacitor ground, C11:

   “Star Ground “means all primary DC grounds should be connected to the ground of bulk capacitor C11 separately in one point. It can reduce the switching noise going into the sensitive pins of the CoolSET device effectively. The primary DC grounds include the followings.

   a. DC ground of the primary auxiliary winding in power transformer, TR1, and ground of C16 and Z11.

   b. DC ground of the current sense resistor, R12

   c. DC ground of the CoolSET device, GND pin of IC11; the signal grounds from C13, C14, C15 and collector of IC12 should be connected to the GND pin of IC11 and then “star “connect to the bulk capacitor ground.

   d. DC ground from bridge rectifier, BR1

   e. DC ground from the bridging Y-capacitor, C4

2. High voltage traces clearance:

   High voltage traces should keep enough spacing to the nearby traces. Otherwise, arcing would incur.

   a. 400V traces (positive rail of bulk capacitor C11) to nearby trace: > 2.0mm

   b. 600V traces (drain voltage of CoolSET IC11) to nearby trace: > 2.5mm

3. Filter capacitor close to the controller ground:

   Filter capacitors, C13, C14 and C15 should be placed as close to the controller ground and the controller pin as possible so as to reduce the switching noise coupled into the controller.

Guideline for PCB layout design when >3KV lightning surge test applied (refer to Figure 28):

1. Add spark gap

   Spark gap is a pair of saw-tooth like copper plate facing each other which can discharge the accumulated charge during surge test through the sharp point of the saw-tooth plate.

   a. Spark Gap 3 and Spark Gap 4, input common mode choke, L1:

   Gap separation is around 1.5mm (no safety concern)

b. Spark Gap 1 and Spark Gap 2, Live / Neutral to GROUND:

These 2 Spark Gaps can be used when the lightning surge requirement is >6KV.

230Vac input voltage application, the gap separation is around 5.5mm

115Vac input voltage application, the gap separation is around 3mm

2. Add Y-capacitor (C2 and C3) in the Live and Neutral to ground even though it is a 2-pin input
3. Add negative pulse clamping diode, D11 to the Current sense resistor, R12:

The negative pulse clamping diode can reduce the negative pulse going into the CS pin of the CoolSET and reduce the abnormal behavior of the CoolSET. The diode can be a fast speed diode such as IN4148.

The principle behind is to drain the high surge voltage from Live/Neutral to Ground without passing through the sensitive components such as the primary controller, IC11.

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