Smarc

User Manual

SM-C12

SMARC Rel. 2.1 compliant module with
NXP i.MX 8M Applications Processors

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REVISION HISTORY

Revision	Date	Note	Rif
1.0	14th May 2019	First official release	LG
1.1	11th November 2019	SDIO_PWR_EN logic level corrected	SB
1.2	25th September 2020	Aligned module to be compliant with SMARC Rel. 2.1 standard: - Added GPIO 12, GPIO 13 (par. 3.2.1.15) - Added pull up resistor on UART_RX and UART_CTS signals (par. 3.2.1.9). Removed Mipi-DSI interface on factory alternatives Configured LVDS interface as a factory option Block diagram and technical specifications updated	AR

Every effort has been made to ensure the accuracy of this manual. However, SECO S.p.A. accepts no responsibility for any inaccuracies, errors or omissions herein. SECO S.p.A. reserves the right to change precise specifications without prior notice to supply the best product possible.

For further information on this module or other SECO products, but also to get the required assistance for any and possible issues, please contact us using the dedicated web form available at http://www.seco.com (registration required).

Our team is ready to assist.

INDEX

Chapter 1.
INTRODUCTION

- Warranty
- Information and assistance
- RMA number request
- Safety
- Electrostatic Discharges
- RoHS compliance
- Terminology and definitions
- Reference specifications

1.1 Warranty

This product is subject to the Italian Law Decree 24/2002, acting European Directive 1999/44/CE on matters of sale and warranties to consumers.

The warranty on this product lasts for 1 year.

Under the warranty period, the Supplier guarantees the buyer assistance and service for repairing, replacing or credit of the item, at the Supplier's own discretion.

Shipping costs that apply to non-conforming items or items that need replacement are to be paid by the customer.

Items cannot be returned unless previously authorised by the supplier.

The authorisation is released after completing the specific form available on the web-site https://www.seco.com/us/support/online-rma.html (RMA Online). The RMA authorisation number must be put both on the packaging and on the documents shipped with the items, which must include all the accessories in their original packaging, with no signs of damage to, or tampering with, any returned item.

The error analysis form identifying the fault type must be completed by the customer and has must accompany the returned item.

If any of the above-mentioned requirements for RMA is not satisfied, the item will be shipped back and the customer will have to pay any and all shipping costs.

Following a technical analysis, the supplier will verify if all the requirements, for which a warranty service applies, are met. If the warranty cannot be applied, the Supplier will calculate the minimum cost of this initial analysis on the item and the repair costs. Costs for replaced components will be calculated separately.

Warning!
All changes or modifications to the equipment not explicitly approved by SECO S.p.A. could impair the equipment's functionality and could void the warranty

1.2 Information and assistance

What do I have to do if the product is faulty?

SECO S.p.A. offers the following services:

- SECO website: visit http://www.seco.com to receive the latest information on the product. In most of the cases it is possible to find useful information to solve the problem.
- SECO Sales Representative: the Sales Rep can help to determine the exact cause of the problem and search for the best solution.
- SECO Help-Desk: contact SECO Technical Assistance. A technician is at disposal to understand the exact origin of the problem and suggest the correct solution.

  E-mail: technical.service@seco.com

  Fax (+39) 0575 350210

- Repair center: it is possible to send the faulty product to the SECO Repair Centre. In this case, follow this procedure:
  - Returned items must be accompanied by a RMA Number. Items sent without the RMA number will be not accepted.
  - Returned items must be shipped in an appropriate package. SECO is not responsible for damages caused by accidental drop, improper usage, or customer neglect.

Note: Please have the following information before asking for technical assistance:

- Name and serial number of the product;
- Description of Customer's peripheral connections;
- Description of Customer's software (operating system, version, application software, etc.);
- A complete description of the problem;
- The exact words of every kind of error message encountered.

1.3 RMA number request

To request an RMA number, please visit SECO's web-site. On the home page, please select "RMA Online" and follow the procedure described.

An RMA Number will be sent within 1 working day (only for on-line RMA requests).

1.4 Safety

The SM-C12 module uses only extremely low voltages.

While handling the board, please use extreme caution to avoid any kind of risk or damages to electronic components.

Always switch the power off, and unplug the power supply unit, before handling the board and/or connecting cables or other boards.

Avoid using metallic components - like paper clips, screws and similar - near the board when connected to a power supply, to avoid short circuits due to unwanted contacts with other board components.

If the board has become wet, never connect it to any external power supply unit or battery.

Check carefully that all cables are correctly connected and that they are not damaged.

1.5 Electrostatic Discharges

The SM-C12 module, like any other electronic product, is an electrostatic sensitive device: high voltages caused by static electricity could damage some or all the devices and/or components on-board.

Whenever handling a SM-C12 module, ground yourself through an anti-static wrist strap. Placement of the board on an anti-static surface is also highly recommended.

1.6 RoHS compliance

The SM-C12 module is designed using RoHS compliant components and is manufactured on a lead-free production line. It is therefore fully RoHS compliant.

1.7 Terminology and definitions

API	Application Program Interface, a set of commands and functions that can be used by programmers for writing software for specific Operating Systems
CAN Bus	Controller Area network, a protocol designed for in-vehicle communication
CSI2	MIPI Camera Serial Interface, 2nd generation standard regulating communication between a peripheral device (camera) and a host processor
DDC	Display Data Channel, a kind of I2C interface for digital communication between displays and graphics processing units (GPU)
DDR	Double Data Rate, a typology of memory devices which transfer data both on the rising and on the falling edge of the clock.
DVI	Digital Visual interface, a type of display video interface
FFC/FPC	Flexible Flat Cable / Flat Panel Cable
GBE	Gigabit Ethernet
Gbps	Gigabits per second
GND	Ground
GPI/O	General purpose Input/Output
HDMI	High Definition Multimedia Interface, a digital audio and video interface
I2C Bus	Inter-Integrated Circuit Bus, a simple serial bus consisting only of data and clock line, with multi-master capability
I2S	Inter-Integrated Circuit Sound, an audio serial bus protocol interface developed by Philips (now NXP) in 1986
LPDDR4	Low-Power Double Data Rate Synchronous Dynamic Random Access Memory, 4th generation
LVDS	Low Voltage Differential Signalling, a standard for transferring data at very high speed using inexpensive twisted pair copper cables, usually used for video applications
Mbps	Megabits per second
MIPI	Mobile Industry Processor Interface alliance
MMC/eMMC	MultiMedia Card / embedded MMC, a type of memory card, having the same interface as the SD card. The eMMC is the embedded version of the MMC. They are devices that incorporate the flash memories on a single BGA chip.
N.A.	Not Applicable
N.C.	Not Connected
OpenGL	Open Graphics Library, an Open Source API dedicated to 2D and 3D graphics
OpenVG	Open Vector Graphics, an Open Source API dedicated to hardware accelerated 2D vector graphics
OTG	On-the-Go, a specification that allows to USB devices to act indifferently as Host or as a Client, depending on the device connected to the port.
PCI-e	Peripheral Component Interface Express

PWM	Pulse Width Modulation
PWR	Power
RGMII	Reduced Gigabit Reduced Media Independent Interface, a standard interface between the Ethernet Media Access Control (MAC) and the Physical Layer (PHY)
SD	Secure Digital, a memory card type
SDIO	Secure Digital Input/Output, an evolution of the SD standard that allows the use of the same SD interface to drive different Input/Output devices, like cameras, GPS, Tuners and so on.
SM Bus	System Management Bus, a subset of the I2C bus dedicated to communication with devices for system management, like a smart battery and other power supply-related devices.
SPI	Serial Peripheral Interface, a 4-Wire synchronous full-duplex serial interface which is composed of a master and one or more slaves, individually enabled through a Chip Select line.
TBM	To be measured
TMDS	Transition-Minimized Differential Signalling, a method for transmitting high speed serial data, normally used on DVI and HDMI interfaces
TTL	Transistor-transistor Logic
USB	Universal Serial Bus
uSDHC	Ultra Secure Digital Host Controller

1.8 Reference specifications

Here below it is a list of applicable industry specifications and reference documents.

Reference	Link
CAN Bus	http://www.bosch-semiconductors.de/en/ubk_semiconductors/safe/ip_modules/can_literature/can_literature.html
CSI	http://www.mipi.org/specifications/camera-interface
DDC	http://www.vesa.org
FasEthernet	http://standards.ieee.org/about/get/802/802.3.html
HDMI	http://www.hdmi.org/index.aspx
I2C	http://www.nxp.com/documents/other/UM10204_v5.pdf
I2S	https://www.sparkfun.com/datasheets/BreakoutBoards/I2SBUS.pdf
LVDS	http://www.ti.com/ww/en/analog/interface/lvds.shtml and http://www.ti.com/lit/ml/snla187/snla187.pdf
MIPI	http://www.mipi.org
MMC/eMMC	http://www.jedec.org/committees/jc-649
NXP i.MX 8M processor	https://www.nxp.com/products/processors-and-microcontrollers/arm-based-processors-and-mcus/i.mx-applications-processors/i.mx-8-processors/i.mx-8m-family-armcortex-a53-cortex-m4-audio-voice-video:i.MX8M
OpenGL	http://www.opengl.org
OpenVG	http://www.khronos.org/openvg
PCI Express	http://www.pcisig.com/specifications/pciexpress
SMARC Design Guide 2.0	https://www.sget.org/fileadmin/user_upload/SMARC_DG_V2.pdf
SMARC Hardware Specification 2.1.1	https://sget.org/wp-content/uploads/2020/05/SMARC_V211.pdf
SD Card Association	https://www.sdcard.org/home
SDIO	https://www.sdcard.org/developers/overview/sdio
SM Bus	http://www.smbus.org/specs
TMDS	http://www.siliconimage.com/technologies/tmds
USB 2.0 and USB OTG	http://www.usb.org/developers/docs/usb_20_070113.zip

Chapter 2.
OVERVIEW

- Introduction
- Technical Specifications
- Electrical Specifications
- Mechanical Specifications
- Supported Operating Systems
- Block Diagram

2.1 Introduction

The SM-C12 is a SMARC Rel. 2.1 compliant module with NXP i.MX 8M Applications Processors. Featuring multicore processing (Dual or Quad ARM Cortex®-A53 cores + general purpose Cortex®-M4 processor) and 4Kp60 HEVC decoding with HDR, it is a scalable solution designed by SECO for home automation, transportation, digital signage and vending machines, and applicable to scenarios requiring advanced security, connectivity, multimedia and real-time response.

The module offers a very high level of integration, both for all most common used peripherals in the ARM domain and for bus interfaces typically used in the x86 domain, like PCI-Express

Presented in the SMARC ("Smart Mobility ARChitecture") form factor, offering the computing abilities of a standard board, with the possibilities of combining with a ready-to-use carrier board like the SECO CSM-B79 or customised carrier board.

For external interfacing to standard devices, a carrier board with a 314-pin MXM connector is needed. This board will implement all the routing of the interface signals to external standard connectors, as well as the integration of other peripherals/devices not already included in SM-C12 module.

2.2 Technical Specifications

Processors

NXP i.MX 8M Family based on ARM Cortex®-A53 cores + general purpose Cortex®-M4 processor:

- i.MX 8M Quad - 4x Cortex®-A53 cores up to 1.5GHz
- i.MX 8M Dual - 2x Cortex®-A53 cores up to 1.5GHz
- i.MX 8M QuadLite - 4x Cortex®-A53 cores up to 1.5GHz, no VPU

Memory

Soldered Down LPDDR4-3200 memory, 32-bit interface, up to 4GB

Graphics

Integrated Graphics Processing Unit, supports 2 independent displays.
Embedded VPU (not available on QuadLite), supports H/W decoding of HEVC, H.264, H.263, MPEG-4, MPEG-2, AVC, VC-1, RV, DivX, VP6, VP8, VP9, JPEG
Supports OpenGL ES 3.1, Open CL 1.2, OpenGL 2.X, Vulkan, DirectX, Open VG 1.1

Video Interfaces

1 x HDMI 2.0a interface, supporting HDCP 2.2 and HDCP 1.4
1 x LVDS 18/24-bit Dual Channel (factory option)

Video Resolution

HDMI, resolution up to 4096x2160 @60Hz
LVDS, resolution up to 1920x1080 @60Hz

Mass Storage

eMMC 5.0 Drive soldered on-board
Optional SD 4-bit interface
8MB QuadSPI Flash

PCI Express

2 x PCI-e x1 Gen2 ports

Networking

1 x Gigabit Ethernet interface
Optional WiFi + BT LE module onboard

USB

1 x USB 2.0 OTG port
USB 3.0 Hub onboard, makes available

- 2 x USB 2.0 ports
- 2 x USB 3.0 Superspeed ports

Audio

I2S Audio interface

Serial ports

Up to 2x UART Tx/Rx/RTS/CTS
2x UART Tx/Rx
1x CAN Bus

Other Interfaces

1x 4-lanes + 1x 2-lanes CSI camera interfaces
I2C Bus
SM Bus
2x SPI interfaces
QuadSPI interface
14 x GPI/Os
Boot select signals
Power Management Signals

Power supply voltage: +5V_{DC}

RTC voltage: 3.3V

Operating temperature:

Commercial version 0°C ÷ +60°C **.
Industrial version -40°C ÷ +85°C **.

Dimensions: 50 x82 mm (1.97" x 3.23")

! *** Measured at any point of SECO standard heatspreader for this product, during any and all times (including start-up). Actual temperature will widely depend on application, enclosure and/or environment. Upon customer to consider application-specific cooling solutions for the final system to keep the heatspreader temperature in the range indicated.*
Please also check paragraph 4.1

2.3 Electrical Specifications

According to SMARC specifications, the SM-C12 module needs to be supplied only with an external +5V_{DC} power supply.

For Real Time Clock working and CMOS memory data retention, it is also needed a backup battery voltage. All these voltages are supplied directly through card edge fingers (see connector's pinout).

All remaining voltages needed for board's working are generated internally from +5V_{DC} power rail.

2.3.1 Power Consumption

SM-C12 module, like all SMARC modules, needs a carrier board for its normal working. All connections with the external world come through this carrier board, which provide also the required voltage to the board, deriving it from its power supply source.

Anyway, it has been possible to measure power consumption directly on VDD_IN power rail (5V_{DC})that supplies the board.

Status	Processor		
	i.MX8M Quad 2GB LPDDR4 8GB eMMC	i.MX8M QuadLite 1GB LPDDR4 8GB eMMC	i.MX8M Dual
Idle	3.2W	3.4W	TBM
GPU working at full load, video output on LVDS	4.5W	5W	TBM
VPU working, video reproduction of a 1080p 60fps video on HDMI	3.7W	N.A.	TBM
RTC Power consumption on VDD_RTC (when VDD_IN off)	270nA		

Please consider that power consumption is strongly dependent on the board's configuration, on number of processor cores active and from the interfaces that are SW enabled.

2.3.2 Power Rails meanings

In all the tables contained in this manual, Power rails are named with the following meaning:

VDD_IN: Module power input voltage. +5V voltage directly coming from the card edge connector.

VDD_RTC: Low current RTC circuit backup power. 3V coin cell voltage coming from the edge card for supplying the RTC clock on the I.MX 8M

_RUN: Switched voltages, i.e. power rails that are active only when the board is in ACPI's S0 (Working) state. Examples: +1.8V_RUN,+3.3V_RUN, +5V_RUN.

_ALW: Always-on voltages, i.e. power rails that are active both in ACPI's S0 (Working), S3 (Standby) and S5 (Soft Off) state. Examples: +5V_ALW, +3.3V_ALW.

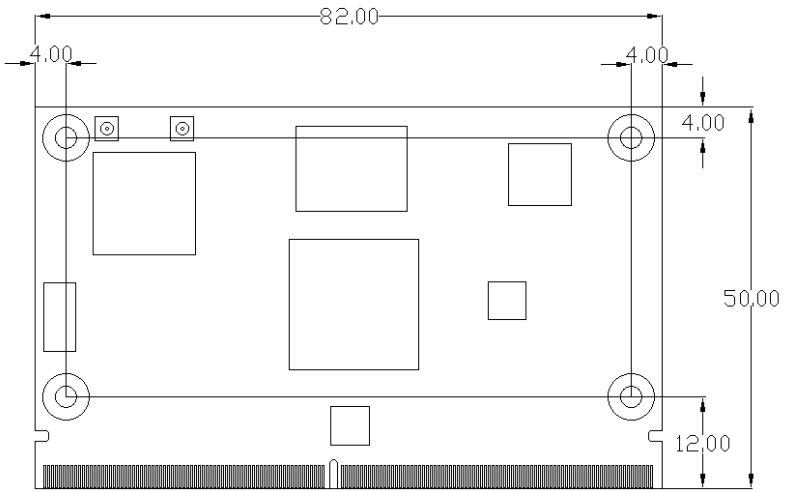
2.4 Mechanical Specifications

According to SMARC® specifications, the board dimensions are: 50 x 82 mm (1.97” x 3.23”) including the pin numbering and edge finger pattern.

Printed circuit of the board is made of ten layers, some of them are ground planes, for disturbance rejection.

The MXM connector accommodates various connector heights for different carrier board applications needs.

When using different connector heights, please consider that, according to SMARC specifications, components placed on bottom side of SM-C12 will have a maximum height of 1.3mm. Keep this value in mind when choosing the MXM connector’s height, if there is the need to place components on the carrier board in the zone below the SMARC module.



2.5 Supported Operating Systems

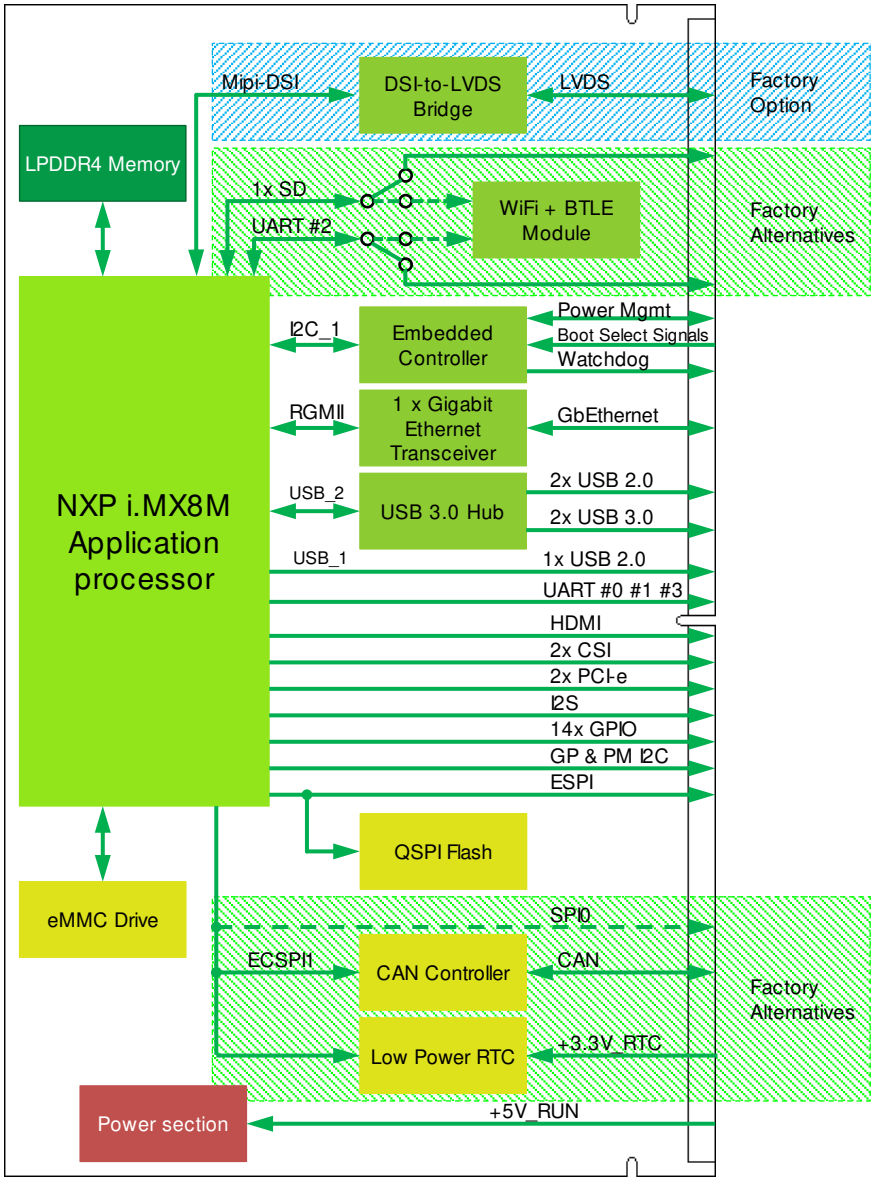
SM-C12 module supports the following operating systems:

- Linux
- Android

SECO will offer the BSP (Board Support Package) for these O.Ss, to reduce at minimum SW development of the board, supplying all the drivers and libraries needed for use both with the SMARC board and the Carrier Board, assuming that the Carrier Board is designed following SECO SMARC Design Guide, with the same IC’s.

For further details, please visit https://www.seco.com.

2.6 Block Diagram



Chapter 3.
CONNECTORS

- Introduction
- Connectors description

3.1 Introduction

According to SMARC specifications, all interfaces to the board are available through a single card edge connector.

TOP SIDE

Card edge golden finger, pin P1

Card edge golden finger, pin P156

BOTTOM SIDE

Card edge golden finger, pin S158

Card edge golden finger, pin S1

3.2 Connectors description

3.2.1 SMARC Connector

According to SMARC Rel 2.1 specification, all interface signals are reported on the card edge connector, which is a 314-pin Card Edge that can be inserted into standard low profile 314 pin 0.5mm right pitch angle connector that was originally defined for use with MXM3 graphics cards.

Not all signals contemplated in the SMARC Rel 2.1 are implemented on card edge connector, therefore, please refer to the following table for a list of effective signals reported on the card edge connector.

For accurate signals description, please consult the following paragraphs.

SMARC Golden Finger Connector - CN4							
TOP SIDE				BOTTOM SIDE			
SIGNAL GROUP	Type	Pin name	Pin nr.	Pin nr.	Pin name	Type	SIGNAL GROUP
				S1	I2C_CAM1_CK	I/O	CAMERA
MANAGEMENT	I	SMB_ALERT_1V8#	P1	S2	I2C_CAM1_DAT	I/O	CAMERA
		GND	P2	S3	GND		
CAMERA	I	CSI1_CK+	P3	S4	RSVD		
CAMERA	I	CSI1_CK-	P4	S5	I2C_CAM0_CK	I/O	CAMERA
		N.C.	P5	S6	CAM_MCK	O	CAMERA
		N.C	P6	S7	I2C_CAM0_DAT	I/O	CAMERA
CAMERA	I	CSI1_RX0+	P7	S8	CSI0_CK+	I	CAMERA
CAMERA	I	CSI1_RX0-	P8	S9	CSI0_CK-	I	CAMERA
		GND	P9	S10	GND		
CAMERA	I	CSI1_RX1+	P10	S11	CSI0_RX0+	I	CAMERA
CAMERA	I	CSI1_RX1-	P11	S12	CSI0_RX0-	I	CAMERA
		GND	P12	S13	GND		
CAMERA	I	CSI1_RX2+	P13	S14	CSI0_RX1+	I	CAMERA
CAMERA	I	CSI1_RX2-	P14	S15	CSI0_RX1-	I	CAMERA
		GND	P15	S16	GND		
CAMERA	I	CSI1_RX3+	P16	S17	N.C.		

CAMERA	I	CSI1_RX3-	P17	S18	N.C.		
		GND	P18	S19	N.C.		
GBE	I/O	GBE0_MDI3-	P19	S20	N.C.		
GBE	I/O	GBE0_MDI3+	P20	S21	N.C.		
GBE	O	GBE0_LINK100#	P21	S22	N.C.		
GBE	O	GBE0_LINK1000#	P22	S23	N.C.		
GBE	I/O	GBE0_MDI2-	P23	S24	N.C.		
GBE	I/O	GBE0_MDI2+	P24	S25	GND		
GBE	O	GBE0_LINK_ACT#	P25	S26	N.C.		
GBE	I/O	GBE0_MDI1-	P26	S27	N.C.		
GBE	I/O	GBE0_MDI1+	P27	S28	N.C.		
		N.C.	P28	S29	N.C.		
GBE	I/O	GBE0_MDI0-	P29	S30	N.C.		
GBE	I/O	GBE0_MDI0+	P30	S31	N.C.		
SPI_INTERFACE	O	SPI0_CS1#	P31	S32	N.C.		
		GND	P32	S33	N.C.		
SDIO_CARD	I	SDIO_WP	P33	S34	GND		
SDIO_CARD	I/O	SDIO_CMD	P34	S35	USB4+	I/O	USB
SDIO_CARD	I	SDIO_CD#	P35	S36	USB4-	I/O	USB
SDIO_CARD	O	SDIO_CK	P36	S37	N.C.		
SDIO_CARD	O	SDIO_PWR_EN	P37	S38	AUDIO_MCK	O	AUDIO
		GND	P38	S39	I2S0_LRCK	I/O	AUDIO
SDIO_CARD	I/O	SDIO_D0	P39	S40	I2S0_SDOUT	O	AUDIO
SDIO_CARD	I/O	SDIO_D1	P40	S41	I2S0_SDIN	I	AUDIO
SDIO_CARD	I/O	SDIO_D2	P41	S42	I2S0_CK	I/O	AUDIO
SDIO_CARD	I/O	SDIO_D3	P42	S43	ESPI_ALERT0#	I	SPI_INTERFACE
SPI_INTERFACE	O	SPI0_CS0#	P43	S44	N.C.		
SPI_INTERFACE	O	SPI0_CK	P44	S45	RSVD		
SPI_INTERFACE	I	SPI0_DIN	P45	S46	RSVD		
SPI_INTERFACE	O	SPI0_DO	P46	S47	GND		

		GND	P47	S48	I2C_GP_CK	I/O	I2C
		N.C.	P48	S49	I2C_GP_DAT	I/O	I2C
		N.C.	P49	S50	N.C.		
		GND	P50	S51	N.C.		
		N.C.	P51	S52	N.C.		
		N.C.	P52	S53	N.C.		
		GND	P53	S54	N.C.		
SPI_INTERFACE	O	ESPI_CS0#	P54	S55	USB5_EN_OC#	I/O	USB
		N.C.	P55	S56	ESPI_IO_2	I/O	SPI_INTERFACE
SPI_INTERFACE	O	ESPI_CK	P56	S57	ESPI_IO_3	I/O	SPI_INTERFACE
SPI_INTERFACE	I/O	ESPI_IO_0	P57	S58	ESPI_RESET#	O	SPI_INTERFACE
SPI_INTERFACE	I/O	ESPI_IO_1	P58	S59	N.C.		
		GND	P59	S60	N.C.		
USB	I/O	USB0+	P60	S61	GND		
USB	I/O	USB0-	P61	S62	USB3_SSTX+	O	USB
USB	I/O	USB0_EN_OC#	P62	S63	USB3_SSTX-	O	USB
		N.C.	P63	S64	GND		
USB	I	USB0_OTG_ID	P64	S65	USB3_SSRX+	I	USB
USB	I/O	USB1+	P65	S66	USB3_SSRX-	I	USB
USB	I/O	USB1-	P66	S67	GND		
USB	I/O	USB1_EN_OC#	P67	S68	USB3+	I/O	USB
		GND	P68	S69	USB3-	I/O	USB
USB	I/O	USB2+	P69	S70	GND		
USB	I/O	USB2-	P70	S71	USB2_SSTX+	O	USB
USB	I/O	USB2_EN_OC#	P71	S72	USB2_SSTX-	O	USB
		RSVD	P72	S73	GND		
		RSVD	P73	S74	USB2_SSRX+	I	USB
USB	I/O	USB3_EN_OC#	P74	S75	USB2_SSRX-	I	USB
PCI_e	O	PCIE_A_RST#	P75	S76	PCIE_B_RST#	O	PCI_e
USB	I/O	USB4_EN_OC#	P76	S77	N.C.		

		RSVD	P77	S78	N.C.		
		RSVD	P78	S79	N.C.		
		GND	P79	S80	GND		
		N.C.	P80	S81	N.C.		
		N.C.	P81	S82	N.C.		
		GND	P82	S83	GND		
PCI_e	O	PCIE_A_REFCK+	P83	S84	PCIE_B_REFCK+	O	PCI_e
PCI_e	O	PCIE_A_REFCK-	P84	S85	PCIE_B_REFCK-	O	PCI_e
		GND	P85	S86	GND		
PCI_e	I	PCIE_A_RX+	P86	S87	PCIE_B_RX+	I	PCI_e
PCI_e	I	PCIE_A_RX-	P87	S88	PCIE_B_RX-	I	PCI_e
		GND	P88	S89	GND		
PCI_e	O	PCIE_A_TX+	P89	S90	PCIE_B_TX+	O	PCI_e
PCI_e	O	PCIE_A_TX-	P90	S91	PCIE_B_TX-	O	PCI_e
		GND	P91	S92	GND		
SECONDARY_DISPLAY	O	HDMI_D2+	P92	S93	N.C.		
SECONDARY_DISPLAY	O	HDMI_D2-	P93	S94	N.C.		
		GND	P94	S95	N.C.		
SECONDARY_DISPLAY	O	HDMI_D1+	P95	S96	N.C.		
SECONDARY_DISPLAY	O	HDMI_D1-	P96	S97	N.C.		
		GND	P97	S98	N.C.		
SECONDARY_DISPLAY	O	HDMI_D0+	P98	S99	N.C.		
SECONDARY_DISPLAY	O	HDMI_D0-	P99	S100	N.C.		
		GND	P100	S101	GND		
SECONDARY_DISPLAY	O	HDMI_CK+	P101	S102	N.C.		
SECONDARY_DISPLAY	O	HDMI_CK-	P102	S103	N.C.		
		GND	P103	S104	N.C.		
SECONDARY_DISPLAY	I	HDMI_HPD	P104	S105	N.C.		
SECONDARY_DISPLAY	I/O	HDMI_CTRL_CK	P105	S106	N.C.		
SECONDARY_DISPLAY	I/O	HDMI_CTRL_DAT	P106	S107	LCD1_BKLT_EN	O	LCD_SUPPORT

		N.C.	P107	S108	LVDS1_CK+	O	PRIMARY_DISPLAY
GPIO	I/O	GPIO0 / CAM0_PWR#	P108	S109	LVDS1_CK-	O	PRIMARY_DISPLAY
GPIO	I/O	GPIO1 / CAM1_PWR#	P109	S110	GND		
GPIO	I/O	GPIO2 / CAM0_RST#	P110	S111	LVDS1_0+	O	PRIMARY_DISPLAY
GPIO	I/O	GPIO3 / CAM1_RST#	P111	S112	LVDS1_0-	O	PRIMARY_DISPLAY
GPIO	I/O	GPIO4 / HDA_RST#	P112	S113	N.C.		
GPIO	I/O	GPIO5 / PWM_OUT	P113	S114	LVDS1_1+	O	PRIMARY_DISPLAY
GPIO	I/O	GPIO6 / TACHIN	P114	S115	LVDS1_1-	O	PRIMARY_DISPLAY
GPIO	I/O	GPIO7	P115	S116	LCD1_VDD_EN	O	LCD_SUPPORT
GPIO	I/O	GPIO8	P116	S117	LVDS1_2+	O	PRIMARY_DISPLAY
GPIO	I/O	GPIO9	P117	S118	LVDS1_2-	O	PRIMARY_DISPLAY
GPIO	I/O	GPIO10	P118	S119	GND		
GPIO	I/O	GPIO11	P119	S120	LVDS1_3+	O	PRIMARY_DISPLAY
		GND	P120	S121	LVDS1_3-	O	PRIMARY_DISPLAY
MANAGEMENT	I/O	I2C_PM_CK	P121	S122	LCD1_BKLT_PWM	O	LCD_SUPPORT
MANAGEMENT	I/O	I2C_PM_DAT	P122	S123	GPIO12	I/O	GPIO
BOOT_SEL	I	BOOT_SEL0#	P123	S124	GND		
BOOT_SEL	I	BOOT_SEL1#	P124	S125	LVDS0_0+	O	PRIMARY_DISPLAY
BOOT_SEL	I	BOOT_SEL2#	P125	S126	LVDS0_0-	O	PRIMARY_DISPLAY
MANAGEMENT	O	RESET_OUT#	P126	S127	LCD0_BKLT_EN	O	LCD_SUPPORT
MANAGEMENT	I	RESET_IN#	P127	S128	LVDS0_1+	O	PRIMARY_DISPLAY
MANAGEMENT	I	POWER_BTN#	P128	S129	LVDS0_1-	O	PRIMARY_DISPLAY
ASYNC_SERIAL	O	SER0_TX	P129	S130	GND		
ASYNC_SERIAL	I	SER0_RX	P130	S131	LVDS0_2+	O	PRIMARY_DISPLAY
ASYNC_SERIAL	O	SER0_RTS#	P131	S132	LVDS0_2-	O	PRIMARY_DISPLAY
ASYNC_SERIAL	I	SER0_CTS#	P132	S133	LCD0_VDD_EN	O	LCD_SUPPORT
		GND	P133	S134	LVDS0_CK+	O	
ASYNC_SERIAL	O	SER1_TX	P134	S135	LVDS0_CK-	O	
ASYNC_SERIAL	I	SER1_RX	P135	S136	GND		
ASYNC_SERIAL	O	SER2_TX	P136	S137	LVDS0_3+	O	PRIMARY_DISPLAY

ASYNC_SERIAL	I	SER2_RX	P137	S138	LVDS0_3-	O	PRIMARY_DISPLAY
ASYNC_SERIAL	O	SER2_RTS#	P138	S139	I2C_LCD_CK	O	LCD_SUPPORT
ASYNC_SERIAL	I	SER2_CTS#	P139	S140	I2C_LCD_DAT	I/O	LCD_SUPPORT
ASYNC_SERIAL	O	SER3_TX	P140	S141	LCD0_BKLT_PWM	O	LCD_SUPPORT
ASYNC_SERIAL	I	SER3_RX	P141	S142	GPIO12	I/O	GPIO
		GND	P142	S143	GND		
CAN	O	CAN0_TX	P143	S144	N.C.		
CAN	I	CAN0_RX	P144	S145	WDT_TIME_OUT#	O	WATCHDOG
		N.C.	P145	S146	PCIE_WAKE#	I	PCI_e
		N.C.	P146	S147	VDD_RTC		
		VDD_IN	P147	S148	LID#	I	MANAGEMENT
		VDD_IN	P148	S149	SLEEP#	I	MANAGEMENT
		VDD_IN	P149	S150	VIN_PWR_BAD#	I	MANAGEMENT
		VDD_IN	P150	S151	CHARGING#	I	MANAGEMENT
		VDD_IN	P151	S152	CHARGER_PRSNT#	I	MANAGEMENT
		VDD_IN	P152	S153	CARRIER_STBY#	O	MANAGEMENT
		VDD_IN	P153	S154	CARRIER_PWR_ON	O	MANAGEMENT
		VDD_IN	P154	S155	FORCE_RECOV#	I	BOOT_SEL
		VDD_IN	P155	S156	BATLOW#	I	MANAGEMENT
		VDD_IN	P156	S157	TEST#	I	MANAGEMENT
				S158	GND		

3.2.1.1 LCD Display Support Signals

The panel control signals are:

LCD0_VDD_EN: Panel #0 VDD enable signal. Set high to enable. +1.8V_RUN electrical level Output.

LCD0_BKLT_EN: Panel #0 Backlight Enable signal. It can be used to turn On/Off the backlight's lamps of a connected LVDS display. +1.8V_RUN electrical level Output

LCD0_BKLT_PWM: This signal can be used to adjust the Panel #0 backlight brightness in displays supporting Pulse Width Modulated (PWM) regulations. +1.8V_RUN electrical level Output

LCD1_VDD_EN: Panel #1 VDD enable signal. Set high to enable. +1.8V_RUN electrical level Output

LCD1_BKLT_EN: Panel #1 Backlight Enable signal. It can be used to turn On/Off the backlight's lamps of a connected LVDS display. +1.8V_RUN electrical level Output.

LCD1_BKLT_PWM: This signal can be used to adjust the Panel #1 backlight brightness in displays supporting Pulse Width Modulated (PWM) regulations. +1.8V_RUN electrical level Output.

I2C_LCD_DAT: LCD I2C Data. This signal is used to read the LCD display EDID EEPROM. +1.8V_RUN electrical level Bidirectional

I2C_LCD_CLK: LCD I2C Clock: This signal is used to read the LCD display EDID EEPROM. +1.8V_RUN electrical level Output

3.2.1.2 Primary Display (LVDS Flat Panel) signals

The module has, as a factory option, a Texas Instruments SN65DSI84 DSI to FlatLink™ bridge, connected from one channel of the MIPI-DSI of the processor to the LVDS0 and LVDS1 interfaces of the edge connector. Supports resolution up to1920x1080p60.

Here follows the signals related to LVDS Channel #0 and #1 management:

LVDS0_0+ / LVDS0_0- : LVDS Channel #0 differential data pair #0

LVDS0_1+/ LVDS0_1-: LVDS Channel #0 differential data pair #1

LVDS0_2+/LVDS0_2-: LVDS Channel #0 differential data pair #2

LVDS0_3+/ LVDS0_3-: LVDS Channel #0 differential data pair #3

LVDS0_CK+/ LVDS0_CK-: LVDS Channel #0 differential Clock

LVDS1_0+/LVDS1_0-: LVDS Channel #1 differential data pair #0.

LVDS1_1+/LVDS1_1-: LVDS Channel #1 differential data pair #1.

LVDS1_2+/LVDS1_2-: LVDS Channel #1 differential data pair #2.

LVDS1_3+/LVDS1_3-: LVDS Channel #1 differential data pair #3.

LVDS1_CK+/LVDS1_CK-: LVDS Channel #1 differential Clock.

3.2.1.3 Secondary Display (HDMI interface) signals

The NXP i.MX 8M processor has an HD Display Transmitter Controller (HDMI TX), which provides a HDMI standard interface for HDMI 2.0a compliant displays. Supports HDCP 2.2 and HDCP 1.4

The signals are:

HDMI_D0+/HDMI_D0-: HDMI Output Differential Pair #0

HDMI_D1+/HDMI_D1-: HDMI Output Differential Pair #1

HDMI_D2+/HDMI_D2-: HDMI Output Differential Pair #2

HDMI_CK+/HDMI_CK-: HDMI Differential Clock

HDMI_HPD: Hot Plug Detect Input signal. +1.8V_RUN electrical level signal

HDMI_CTRL_CK: DDC Clock line for HDMI panel. Bidirectional signal, +1.8V_RUN electrical level with a 100kΩ pull-up resistor

HDMI_CTRL_DAT: DDC Data line for HDMI panel. Bidirectional signal, +1.8V_RUN electrical level with a 100kΩ pull-up resistor

Since HDMI Tx module is embedded in the i.MX 8 processors it is not necessary to implement voltage level shifter for TMDS differential pairs on the Carrier board. It is still necessary, however, to implement voltage level shifters on Control data/Clock signals, as well as for Hot Plug Detect signal.

3.2.1.4 Serial Cameras

There are two MIPI-CSI2 interfaces available. The CSI0 interface supports two lanes, the CSI1 interface supports 4 lanes.

CSI0_CK+/CSI0_CK-: 2-lane CSI Input Clock Differential Pair

CSI0_RX0+/CSI0_RX0-: 2-lane CSI Input Differential Pair 0

CSI0_RX1+/CSI0_RX1-: 2-lane CSI Input Differential Pair 1

CSI1_CK+/CSI1_CK-: 4-lane CSI Input Clock Differential Pair

CSI1_RX0+/CSI1_RX0- 4-lane CSI Input Differential Pair 0

CSI1_RX1+/CSI1_RX1-: 4-lane CSI Input Differential Pair 1

CSI1_RX2+/CSI1_RX2-: 4-lane CSI Input Differential Pair 2

CSI1_RX3+/CSI1_RX3-: 4-lane CSI Input Differential Pair 3

3.2.1.5 SDI/O interface signals

The NXP i.MX 8M processors offer many different SDIO interfaces, that can be used independently one from the other to implement different mass storages (internal eMMC, internal SD Card, external SDI/O interface).

The SDIO1 signals of the processor are used for the onboard eMMC storage of the SM-C12 module.

When the SM C12 module is without an onboard wireless module, the SDIO2 interface of the processor is externally accessible through the edge connector of the

module. Supporting 4-bit mode as per the SMARC specification.

The uSDHC controller complies with:

- SD Host Controller Standard Specification version 3.0 with 50 MHZ SDR signaling to support up to 25MB/sec (High Speed Mode)
- MMC System Specification version 5.0

The edge accessible SDIO2 signals are as follows:

SDIO_WP: Write Protect bidirectional signal, electrical level +3.3V_RUN. It is used to communicate the status of Write Protect switch on external SD/MMC card.

SDIO_CMD: Command/Response line. Bidirectional signal, electrical level +3.3V_RUN, used to send command from Host (i.MX 8M processor) to the connected card, and to send the response from the card to the Host.

SDIO_CD#: Card Detect Input. Active Low Signal, electrical level +3.3V_RUN with 10kΩ pull-up resistor. This signal must be externally pulled low to signal that a SDIO/MMC Card is present.

SDIO_CK: Clock Line (output), 52MHz maximum frequency for MMC High Speed Mode, 50 MHz maximum frequency for SD/SDIO High Speed Mode.

SDIO_PWR_EN: SDIO Power Enable output, active high signal, electrical level +3.3V_RUN. It is used to enable the power line supplying SD/SDIO/MMC devices.

SDIO_[D0÷D3]: SDIO data bus. Signals for 4-bit SD/SDIO/MMC communication mode. The 8-bit MMC communication mode is unsupported.

As a factory alternative, the above set of signals are instead routed to an onboard WiFi/BT controller.

3.2.1.6 SPI interface signals

The signals related to SPI0 are as follows:

SPI0_CS0#: SPI primary Chip select, active low output signal. Electrical level +1.8V_RUN

SPI0_CS1#: SPI secondary Chip select, active low output signal. Electrical level +1.8V_RUN. This signal must be used only in case there are two SPI devices on the carrier board, and the first chip select signal (SPI_CS0#) has already been used. It must not be used in case there is only one SPI device

SPI0_CK: SPI Clock Output to carrier board's SPI embedded devices. Electrical level +1.8V_RUN

SPI0_DIN: SPI0 Master Data Input, electrical level +1.8V_RUN. Input to i.MX 8M from SPI devices embedded on the Carrier Board

SPI0_DO: SPI0 Master Data Output, electrical level +1.8V_RUN. Output from i.MX 8M to SPI devices embedded on the Carrier Board

The signals related to QuadSPI are as follows:

ESPI_CK: QuadSPI Master Clock Output. Electrical level +1.8V_RUN. The reference timing signal for all the serial input and output operations

ESPI_CS0#: QuadSPI Master Chip Select Output. Electrical level +1.8V_RUN. Driven low by the processor to select the QuadSPI slave device on the carrier board. On the same bus there is a second QuadSPI slave device (flash storage), mounted on the module, connected to a dedicated chip select signal

ESPI_IO_[0:3]: QuadSPI Master Data Bidirectional . Electrical level +1.8V_RUN. Data transfer between the master and slaves. In Single I/O mode, ESPI_IO_0 is the eSPI master output/eSPI slave input (MOSI) whereas ESPI_IO_1 is the eSPI master input/eSPI slave output (MISO).

ESPI_RESET#: QuadSPI Reset. Output. Electrical level +1.8V_RUN. Reset the QuadSPI interface for both master and slaves.

ESPI_ALERT0#: Alert signal driven by the slave QuadSPI slave device. Input. Electrical level +1.8V_RUN

SPI interface can support speed up to 20MHz.

3.2.1.7 Audio interface signals

Here are following the signals related to I2S Audio interface:

AUDIO_MCK: Master clock output to Audio codec. Output from the module to the Carrier board, electrical level +1.8V_RUN

I2S0_LRCK: Left& Right audio synchronization clock. Bi-Directional between the module to the Carrier board, electrical level +1.8V_RUN

I2S0_SDOUT: Digital audio Output. Output from the module to the Carrier board, electrical level +1.8V_RUN

I2S0_SDIN: Digital audio Input. Input from the module to the Carrier board, electrical level +1.8V_RUN

I2S0_CK: Digital audio clock. Bi-Directional between the module to the Carrier board, electrical level +1.8V_RUN

All these signals have to be connected, on the Carrier Board, to an I2S Audio Codec. Please refer to the chosen Codec's Reference Design Guide for correct implementation of audio section on the carrier board.

3.2.1.8 IC2 Interface

I2C_GP_CK: I2C General Purpose clock signal. Bi-Directional between the module to the Carrier board, electrical level +1.8V_RUN

I2C_GP_DAT: I2C General Purpose data signal. Bi-Directional between the module to the Carrier board, electrical level +1.8V_RUN

3.2.1.9 Asynchronous Serial Ports (UART) interface signals

All UART interface signals are directly managed by the i.MX 8M processor. In all versions, the edge connector offers the three following UART interfaces.

SER0_TX: UART #2 Interface, Serial data Transmit (output) line, +1.8V_RUN electrical level

SER0_RX: UART #2 Interface, Serial data Receive (input) line, +1.8V_RUN electrical level with a 100kΩ pull-up resistor

SER0_RTS#: UART #2 Interface, Handshake signal, Request to Send (output) line, +1.8V_RUN electrical level

SER0_CTS#: UART #2 Interface, Handshake signal, Clear to Send (Input) line, +1.8V_RUN electrical level with a 100kΩ pull-up resistor

SER1_TX: UART #1 Interface, Serial data Transmit (output) line, +1.8V_RUN electrical level

SER1_RX: UART #1 Interface, Serial data Receive (input) line, +1.8V_RUN electrical level with a 100kΩ pull-up resistor

SER3_RX: UART #3 Interface, Serial data Receive (input) line, +1.8V_RUN electrical level with a 100kΩ pull-up resistor

SER3_TX: UART #3 Interface, Serial data Transmit (output) line, +1.8V_RUN electrical level

A fourth UART interface is present only when the module is without the optional onboard WLAN combo module:

SER2_TX: UART #4 Interface, Serial data Transmit (output) line, +1.8V_RUN electrical level

SER2_RX: UART #4 Interface, Serial data Receive (input) line, +1.8V_RUN electrical level with a 100kΩ pull-up resistor

SER2_RTS#: UART #4 Interface, Handshake signal, Request to Send (output) line, +1.8V_RUN electrical level

SER2_CTS#: UART #4 Interface, Handshake signal, Clear to Send (Input) line, +1.8V_RUN electrical level with a 100kΩ pull-up resistor.

Please consider that interface is at +1.8V_RUN electrical level; therefore, please evaluate well the typical scenario of application. If there isn't any explicit need of interfacing directly at +1.8V_RUN level, for connection to standard serial ports commonly available (like those offered by common PCs, for example) it is mandatory to include an RS-232 transceiver on the carrier board.

3.2.1.10 CAN interface signals

CAN0_TX: CAN Transmit Output for CAN Bus Channel 0. +1.8V_RUN electrical voltage level signal.

CAN0_RX: CAN Receive Input for CAN Bus Channel 0. +1.8V_RUN electrical voltage level signal.

The CAN interface is managed by an onboard Microchip Technology MCP2517FDT-H/JHA CANbus Controller.

Please consider that it is not possible to connect the SMARC CAN interface to any CAN Bus directly, it is necessary to integrate a CAN Bus Transceiver in the Carrier board.

3.2.1.11 USB interface signals

The module has 5x USB ports consisting of 1x USB 2.0 OTG port from the NXP i.MX 8M processor USB 2.0 controller. 2x USB 3.0 Superspeed and 2x USB 2.0 from a Cypress USB3304-68LTXC USB 3.0 hub controller.

USB 2.0 controller Core #1 is capable of OTG (On-The-Go) capabilities, capable to work in High Speed (HS), Full Speed (FS) and Low Speed (LS) in Host mode, and HS/FS in peripheral mode. It is carried out directly to the golden finger connector

To allow OTG functionality, the following signal must be driven as an open collector signal by external circuitry placed on the carrier board:

USB0_OTG_ID: USB OTG Input, electrical level +3.3V_RUN. When USB Port #0 is set to work in Client mode, then this signal shall be used to inform the USB controller when an external USB Host is connected (signal High) or disconnected (Signal Low). It must be tied to GND when USB Port #0 has to be set to work in Host mode. When not driven, USB Port#0 will work in Client mode.

Please take note that this USB0, directly managed by i.MX 8M USB Host Controller core #1, on SM-C12 during normal condition does work as USB 2.0 Host Port. Client mode is supported only during serial download when signal FORCE_RECOV# is driven low. With Software customization if needed, this port can be configured to work always in Client mode.

Here following the signals related to USB interfaces.

USB0+/ USB0-: Universal Serial Bus Port #0 differential pair (directly managed by i.MX 8M USB Host Controller core #1).

USB0_EN_OC#: Power Enable and over current monitoring function. Active Low Output signal, +3.3V_RUN electrical level with a 10kΩ pull-up resistor. Refer to SMARC 2.1 Specification for over current operation information.

USB1+/ USB1-: Universal Serial Bus Port #1 differential pair

USB1_EN_OC#: Power Enable and over current monitoring function. Active Low Output signal, +3.3V_RUN electrical level with a 10kΩ pull-up resistor. Refer to SMARC 2.1 Specification for OC operation information.

USB2+/USB2-: Universal Serial Bus Port #2 differential pair.

USB2_SSTX+/ USB2_SSTX-: USB Port #2 Superspeed Transmit differential pair.

USB2_SSRX+/ USB2_SSRX-: USB Port #2 Superspeed Receive differential pair.

USB2_EN_OC#: Power Enable and over current monitoring function. Active Low Output signal, +3.3V_RUN electrical level with a 10kΩ pull-up resistor. Refer to SMARC 2.1 Specification for OC operation information.

USB3+/USB3-: Universal Serial Bus Port #3 differential pair.

USB3_SSTX+/ USB3_SSTX-: USB Port #3 Superspeed Transmit differential pair.

USB3_SSRX+/ USB3_SSRX-: USB Port #3 Superspeed Receive differential pair.

USB3_EN_OC#: Power Enable and over current monitoring function. Active Low Output signal, +3.3V_RUN electrical level with a 10kΩ pull-up resistor. Refer to SMARC 2.1 Specification for OC operation information.

USB4+/ USB4-: Universal Serial Bus Port #4 differential pair

USB4_EN_OC#: Power Enable and over current monitoring function. Active Low Output signal, +3.3V_RUN electrical level with a 10kΩ pull-up resistor. Refer to SMARC 2.1 Specification for OC operation information.

For EMI/ESD protection, common mode chokes on USB data lines, and clamping diodes on USB data and voltage lines, are also needed.

3.2.1.12 PCI Express interface signals

The SM-C12 module can offer two PCI Express x1 lanes, which is directly managed by i.MX8 processor (all versions).

PCI express Gen 2.0 (5Gbps) is supported.

Here following the signals involved in PCI express management

PCIE_A_RX+/ PCIE_A_RX-: PCI Express lane #0, Transmitting Output Differential pair

PCIE_A_TX+/PCIE_A_TX-: PCI Express lane #0, Receiving Input Differential pair

PCIE_A_REFCK+/ PCIE_A_REFCK-: PCI Express Reference Clock for lane #0, Differential Pair

PCIE_A_RST#: Reset Signal that is sent from SMARC Module to a PCI-e device available on the carrier board. Active Low, +3.3V_RUN electrical level. Controlled by a STM32 MCU soldered onboard the SMARC module.

PCIE_B_RX+/ PCIE_B_RX-: PCI Express lane #1, Transmitting Output Differential pair

PCIE_B_TX+/PCIE_B_TX-: PCI Express lane #1, Receiving Input Differential pair

PCIE_B_REFCK+/ PCIE_B_REFCK-: PCI Express Reference Clock for lane #1, Differential Pair

PCIE_B_RST#: Reset Signal that is sent from SMARC Module to a PCI-e device available on the carrier board. Active Low, +3.3V_RUN electrical level. Controlled by a STM32 MCU soldered onboard the SMARC module.

3.2.1.13 Gigabit Ethernet signals

Gigabit Ethernet interface is realized on SM-C12 module by using a Texas Instruments DP83867CRRGZR Gigabit Ethernet transceiver, which is interfaced to NXP i.MX 8M processor through an RGMII interface.

Here following the signals involved in Fast Ethernet management

GBE0_MDI0+/GBE0_MDI0-: Media Dependent Interface (MDI) Transmit/Receive differential pair

GBE0_MDI1+/GBE0_MDI1-: Media Dependent Interface (MDI) Transmit/Receive differential pair

GBE0_MDI2+/GBE0_MDI2-: Media Dependent Interface (MDI) Transmit/Receive differential pair

GBE0_MDI3+/GBE0_MDI3-: Media Dependent Interface (MDI) Transmit/Receive differential pair

GBE0_LINK_ACT#: Ethernet controller activity indicator. Active Low Output signal, +3.3V_RUN electrical level

GBE0_LINK100#: Ethernet controller 100Mbps link indicator. Active Low Output signal, +3.3V_RUN electrical level

GBE0_LINK1000#: Ethernet controller 1Gbps link indicator. Active Low Output signal, +3.3V_RUN electrical level

3.2.1.14 Watchdog

WDT_TIME_OU: Watchdog timer Output. +1.8V_RUN electrical level

3.2.1.15 Miscellaneous signals

GPIO0 / CAM0_PWR#: General Purpose I/O #0, +1.8V_RUN electrical level
GPIO1 / CAM1_PWR#: General Purpose I/O #1, +1.8V_RUN electrical level
GPIO2 / CAM0_RST#: General Purpose I/O #2, +1.8V_RUN electrical level
GPIO3 / CAM1_RST#: General Purpose I/O #3, +1.8V_RUN electrical level
GPIO4 / HDA_RST#: General Purpose I/O #4, +1.8V_RUN electrical level
GPIO5 / PWM_OUT: General Purpose I/O #5, +1.8V_RUN electrical level
GPIO6 / TACHIN: General Purpose I/O #6, +1.8V_RUN electrical level
GPIO7: General Purpose I/O #7, +1.8V_RUN electrical level
GPIO8: General Purpose I/O #8, +1.8V_RUN electrical level
GPIO9: General Purpose I/O #9, +1.8V_RUN electrical level
GPIO10: General Purpose I/O #10, +1.8V_RUN electrical level
GPIO11: General Purpose I/O #11, +1.8V_RUN electrical level
GPIO12: General Purpose I/O #12, +1.8V_RUN electrical level
GPIO13: General Purpose I/O #13, +1.8V_RUN electrical level

3.2.1.16 Management pins

According to the SMARC specifications, the input pins listed below are all Active Low, meant to be driven by open drain devices on the carrier board:

VIN_PWR_BAD#: Power Bad indication signal from the Carrier Board
CARRIER_PWR_ON: Power On. Command to the Carrier Board. Output, +1.8V_RUN electrical level
CARRIER_STBY#: Stand By command to the Carrier Board. Output, +1.8V_RUN electrical level
RESET_OUT#: General Purpose Reset. Output, +1.8V_RUN electrical level
RESET_IN#: General Purpose Reset. Input, +1.8V_RUN electrical level
POWER_BTN#: Power Button. Input, +1.8V_RUN electrical level
SLEEP#: Sleep indicator from Carrier board. Input, +1.8V_RUN electrical level
LID#: LID Switch. Input, +1.8V_RUN electrical level
BATLOW#: Battery Low indication signal from the Carrier Board. Input, +1.8V_RUN electrical level
I2C_PM_CK: Power Management I2C Clock

I2C_PM_DAT: Power Management I2C Data
CHARGING#: Battery Charging Input Signal from the Carrier Board. Input, +1.8V_RUN electrical level
CHARGER_PRSNT#: Battery Charger Present input from the Carrier Board. Input, +1.8V_RUN electrical level
TEST#: Held low by Carrier to invoke Module vendor specific test function(s). Input. +1.8V_RUN electrical level
SMB_ALERT_1V8#: SM Bus Alert# (interrupt) signal. Input, +1.8V_RUN electrical level

3.2.1.17 Boot Select

The following signals are active low and driven by open drain circuitry on the carrier board.

BOOT_SEL0#: Boot Device Selection #0. Input, +1.8V_RUN electrical level with a 10kΩ pull-up resistor
BOOT_SEL1#: Boot Device Selection #1. Input, +1.8V_RUN electrical level with a 10kΩ pull-up resistor
BOOT_SEL2#: Boot Device Selection #2. Input, +1.8V_RUN electrical level with a 10kΩ pull-up resistor
FORCE_RECOV#: Force recovery Mode. Input, +1.8V_RUN electrical level with a 10kΩ pull-up resistor

Chapter 4.
Appendices

- Thermal Design

4.1 Thermal Design

Highly integrated modules like SM-C12 offer very high performance within small dimensions. On the other hand, the miniaturization of ICs and the high operating frequencies of the processors lead to high heat generation that must be dissipated in order to maintain the CPU within its allowed temperature range.

The operating temperature specified in the Technical Features of SM-C12 indicates the temperature range in which any and all parts of the heat spreader / heat sink must remain, in order for SECO to guarantee functionality. Hence, these numbers do not necessarily indicate the suitable environmental temperature.

The heat spreader is not intended to be a guaranteed standalone cooling system, but should be used only as a supplemental means of transferring heat to another dissipation system (i.e. heat sinks, fans, heat pipes etc).

It is the customer's responsibility to design and apply an application-dependent cooling system, capable of ensuring that the heat spreader / heat sink temperature remain within the indicated range of the module.

It is an absolute requirement that the customer, after thorough evaluation of the processor's workload in the actual system application, the system enclosure and consequent air flow/Thermal analysis, accurately study and develop a suitable cooling solution for the assembled system.

SECO can provide SM C12 specific heatspreaders and heatsinks, but please remember that their use must be evaluated accurately inside the final system, and that they should be used only as a part of a more comprehensive ad-hoc cooling solutions.

Ordering Code	Description
RC12-DISS-1-PK	SMARC HEAT SPREADER: SM-C12 Heat Spreader (PASSIVE) - Packaged
RC12-DISS-2-PK	SMARC HEAT SINK: SM-C12 Heat Sink (PASSIVE) - Packaged

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