SY89610L

77.75MHz to 694MHz Jitter Attenuator and Low Phase Noise Frequency Synthesizer

General Description

The SY89610L is a 3.3V, fully differential jitter attenuator and frequency synthesizer that accepts a noise clock between 19.44MHz and 694MHz, depending on I/O frequency selection. The output provides an ultra-low jitter clock frequency between 77.75MHz and 694MHz covering SONET/SDH, Gigabit Ethernet, Fibre Channel, SAS, SATA, and many other communication standards.

The output jitter of the SY89610L is typically $1ps_{RMS}$. It has a 1kHz to 10kHz programmable loop bandwidth to accommodate different jitter attenuation applications and PLL requirements. The auto-tune circuit enables precision frequency calibration.

The differential input includes Micrel's unique, 3-pin input termination architecture that interfaces to LVPECL, LVDS or CML differential signals, (AC- or DC-coupled) as small as 100mV without any level-shifting or termination resistor networks in the signal path. For AC-coupled input interface applications, an on-board output reference voltage (V_{REF-AC}) is provided to bias the V_T pin. The outputs are compatible with 400mV typical swing into 50Ω loads, with rise/fall times guaranteed to be less than 250ps.

The SY89610L operates at 3.3V ±10% supply and the output can accommodate 1.8V to 3.3V operation with the dedicated output supply. The part is guaranteed to operate over the full industrial temperature range (–40°C to +85°C). The SY89610L is part of Micrel's Precision Edge® product line.

Datasheets and support documentation can be found on Micrel's web site at: www.micrel.com.

Precision Edge®

Features

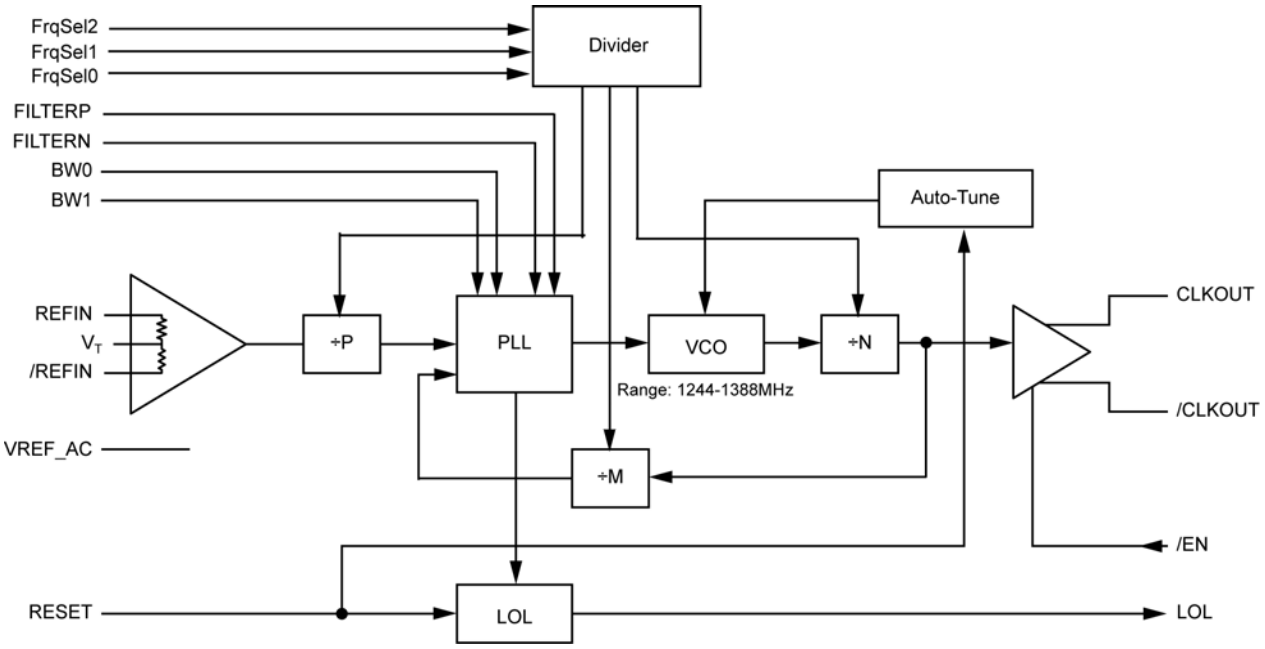
- Accepts high jitter input clock signal and attenuates it to provide Ultra-Low Jitter and Phase Noise clock signal at the output
- Output Frequency Range: 77.75MHz – 694MHz
- Input Frequency Range: 19.44MHz – 694MHz
- Phase Noise and Jitter performance:
  – $<2ps_{RMS}$ Output Jitter Gen (12kHz-20MHz)
  – Low Phase Noise: -80dBc/Hz at 1kHz offset
- CML compatible output signal
- 3-pin input accepts an AC- or DC-coupled differential input (LVDS, LVPECL, and CML)
- Unique, Auto-Tune circuitry enables precision frequency calibration
- Internal source termination to minimize round-trip reflections
- Programmable Loop Bandwidth: 1kHz-10kHz
- Output Enable/disable function
- Only one external component needed for LC VCO (a filter capacitor)
- Includes Loss of Lock (LOL) output pin
- Includes Auto-tune Circuit for precision frequency calibration
- 1.8V ±5% to 3.3V ±10% output power supply
- 3.3V ±10% power supply operation
- Industrial temperature range: –40°C to +85°C
- Available in 32-pin (5mm x 5mm) QFN package

Applications

Covers telecom/datacom/storage standards:

- SONET/SDH
- GbE and 10GbE LAN PHY (w/FEC)
- 1/2/4/8G Fibre Channel
- High-end routers and switches
- Telecom transmission equipment
- High speed optical modules
- Long haul transport

Functional Block Diagram



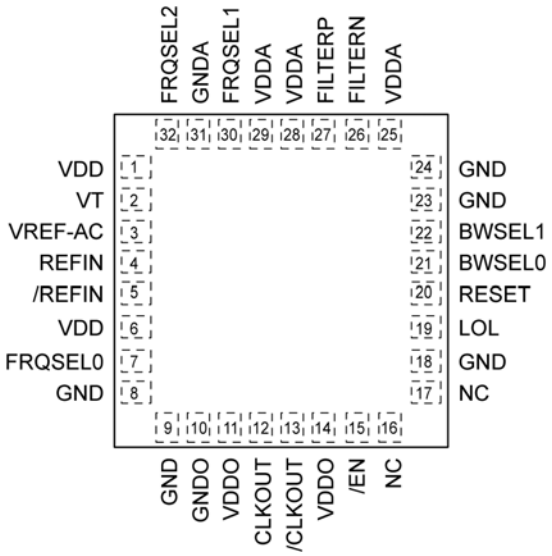
Ordering Information[1]

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY89610LMG	QFN-32	Industrial	SY89610L with Pb-Free bar-line indicator	NiPdAu Pb-Free
SY89610LMGTR[2]	QFN-32	Industrial	SY89610L with Pb-Free bar-line indicator	NiPdAu Pb-Free

Notes:

1. Contact factory for die availability. Dice are guaranteed at T_A = 25°C, DC Electricals only.
2. Tape and Reel.

Pin Configuration



32-Pin QFN

Pin Description

Pin Number	Pin Name	Pin Function
2	VT	Input Termination Center-Tap: Each side of the differential input pair terminates to VT pin. This pin provides a center-tap to a termination network for maximum interface flexibility. See “Input Interface Applications” subsection.
3	VREF-AC	Reference Output Voltage: This output biases to V_{DD}-1.4V. It is used when AC-coupling the inputs (IN, /IN). Connect V_{REF}-AC directly to the V_T pin. Bypass with 0.01µF low ESR capacitors to V_{DD}. Maximum current source or sink is ±0.5mA. See “Input Interface Applications” subsection.
4, 5	REFIN, /REFIN	Differential Input Pair: This input pair is the differential signal input to the device. Input accepts AC- or DC-coupled differential signals as small as 100mV (200mV_{PP}). Each pin of this pair internally terminates with 50Ω to the V_T pin. See Figure 1a.
15	/EN	Single-ended Input: This TTL/CMOS input disables and enables the output. It has an internal pull-down and will default to a logic LOW state if left open. When HIGH, the output is forced into the disable state (Q = LOW and /Q = HIGH). The pull-down current is typically 0.5µA.
8, 9, 18, 23, 24	GND, Exposed Pad	Ground: These are the ground pins for core and input stage. Exposed pad must be connected to a ground plane that is the same potential as the ground pin.
12, 13	CLKOUT, /CLKOUT	CML Differential Output Pair: Differential buffered output copy of the input signal with very low jitter. The output swing is typically 400mV. The output pair is referenced to V_{DDO}. Output pair can be terminated 100Ω across or 50Ω to V_{BIAS}. See “CML Output Termination” subsection.
10	GNDO	Ground: This is the ground pin for output stage. GNDO and GND must be connected together on the PCB.
11, 14	VDDO	CML Output Driver Power Pins: VDDO enables the output stage to operate from a lower supply voltage than the core synthesizer voltage. These outputs can be powered from 1.8V ±5% to 3.3V ±10% power supply. For applications that only require 3.3V reference output operation, VDDO and VDD pins may be connected to a common power supply. Connect both VDDO pins to same power supply. Bypass with 0.1µF//0.01µF low ESR capacitors as close to the V_{DD} pins as possible.
20	RESET	Single-ended Input: Reset is active on the Low-to-High edge of the input pulse. It has an internal pull-down and will default to a logic LOW state if left open. Resetting the part starts an auto-tune sequence to provide output frequency closest to input frequency. Calibration setting is lost on power down. The pull-down current is typically 0.5µA.
19	LOL	Single-ended Output: This LVTTL/CMOS output asserts HIGH when the PLL is out of phase lock. LOL is asserted if the PLL frequency deviates more than ±1000ppm for more than 5ms. This prevents false triggering. The Loss of Lock pin can be directly connected to /EN.
27, 26	FILTERP, FILTERN	Analog Input: These pins provide reference for PLL loop filter. Connect a LOW ESR capacitor across these pins as close to the device as possible, clear from any supply lines or adjacent signal lines. See “External Loop Filter Considerations” for loop filter values. Loop filter capacitor value depends on I/O frequency selection. Loop filter capacitor layout should include a quiet ground plane under the loop filter capacitor and loop filter (FILTP, FILTN) pins. Recommend 1206, X5R, 6.3V ceramic type, ±30%. See “PLL Loop Filter Capacitor Table”.
31	GNDA	Ground: This is an analog ground pin for the PLL. Connect to “quiet” ground. It is internally referenced to the VCO. GNDA and Ground must be shorted on the PCB.
25, 28, 29	VDDA	Analog Power: Connect to “quiet” 3.3V ±10% power supply. These pins are not internally connected and must be shorted on the PCB. VDDA internally connects to the VCO. Bypass with 0.1µF//0.01µF low ESR capacitors as close to the pin as possible
21, 22	BW0, BW1	Single-ended Input: These LVTTL/CMOS inputs determine the loop bandwidth of the jitter reducing PLL. BWSEL0 and BWSEL1 will default to a logic HIGH state if left open with a typical pull-up current of 1.3µA. See “Loop Bandwidth Table.”

Pin Description

Pin Number	Pin Name	Pin Function
7, 30, 32	FRQSEL0 FRQSEL1 FRQSEL2	Single-ended Input: These LVTTL/CMOS inputs program internal pre- and post-dividers to determine the I/O synthesis multiplication factor. Each FrqSel has three logic states, HIGH, LOW, and Float. These pins will default to a mid-rail (float) state (VDD/2) if left open. These inputs have a pull-up resistor of 180kΩ-to-VDD and a pull-down resistor of 180kΩ-to-GND. See “I/O Frequency Table” for more details.
16, 17	NC	No Connect. Solder pins to floating pads.
1, 6	VDDC	Positive Power Supply: VDDC pins are connected to core and input stage that connects to a 3.3V ±10% power supply. Bypass with 0.1uF//0.01uF low ESR capacitors as close to the V_{CC} pins as possible.

BW1	BW0	Nominal Loop Bandwidth (Hz)
0	0	1k
0	1	2k
1	0	5k
1	1	10k

Table 1. Loop Bandwidth Table

Input Frequency (MHz)	Output Frequency (MHz)	FRQSEL2	FRQSEL1	FRQSEL0	P	N	M	Input Min.	Input Max.	Output Min.	Output Max.	Mult.
78	78	0	0	0	1	16	1	77.75	86.75	77.75	86.75	1
78	155	0	0	Float	1	8	2	77.75	86.75	155.5	173.5	2
78	311	0	0	1	1	4	4	77.75	86.75	311	347	4
78	622	0	Float	0	1	2	8	77.75	86.75	622	694	8
155	155	0	Float	1	2	8	2	155.5	173.5	155.5	173.5	1
155	311	0	1	0	2	4	4	155.5	173.5	311	347	2
155	622	0	1	Float	2	2	8	155.5	173.5	622	694	4
311	311	Float	0	1	4	4	4	311	347	311	347	1
311	622	Float	Float	0	4	2	8	311	347	622	694	2
622	622	Float	1	Float	8	2	8	622	694	622	694	1
19	78	1	0	0	1	16	4	19.44	21.69	77.75	86.75	4
19	155	1	0	Float	1	8	8	19.44	21.69	155.5	173.5	8
19	311	1	0	1	1	4	16	19.44	21.69	311	347	16
19	622	1	Float	0	1	2	32	19.44	21.69	622	694	32

Table 2. I/O Frequency Table

Input Frequency = 78MHz, 155MHz, 311MHz, 622MHz				
BW Code	00	01	10	11
BW (kHz)	1	2	5	10
Cext (uF)	4.7	1	0.22	0.15

Input Frequency = 19MHz				
BW Code	00	01	10	11
BW (kHz)	1	2	5	10
Cext (uF)	1	0.33	0.15	0.033

Table 3. PLL Loop Filter Capacitor Tables

Offset/loop BW	1kHz	2kHz	5kHz	10kHz	
100Hz offset	-50	-55	-70	-75	dBc/Hz
1kHz offset	-65	-65	-75	-80	dBc/Hz
10kHz offset	-90	-90	-90	-90	dBc/Hz
100kHz offset	-115	-110	-110	-115	dBc/Hz

Table 4. Typical Phase Noise Performance (622MHz Input, 622MHz Output)

Absolute Maximum Ratings[1]

Supply Voltage ($V_{DDA,}$ $V_{DD,}$ V_{DDO})..... –0.5V to +4.0V
Input Voltage (V_{IN})..... –0.5V to V_{DDC} + 0.4V
CML Output Voltage (V_{OUT}).....-0.5V to V_{DDO} + 0.4V
CML Output Current (I_{OUT})
Continuous.....50mA
Surge 100mA
Current (V_T)
Source or sink on VT pin .....±100mA
Input Current
Source or sink Current on (Ref-IN, /Ref-IN) ..±50mA
Current (V_{REF})
Source or sink current on V_{REF-AC}[2] .....±1.5mA
Maximum Junction Temperature..... 125°C
Lead Temperature (soldering, 20sec.)..... 260°C
Storage Temperature (T_s) .....–65°C to +150°C
ESD (Human Body Model).....2000V

Operating Ratings[3]

Supply Voltage ($V_{DDA,}$ V_{DD}) .....+3.0V to +3.60V
Output Supply Voltage (V_{DDO}).....+1.71V to +3.60V
Ambient Temperature (T_A) .....–40°C to +85°C
Package Thermal Resistance[4]
QFN
Still-air (θ_{JA}) .....35°C/W
Junction-to-board (ψ_{JB}).....20°C/W

DC Electrical Characteristics[5]

V_{DD} = 3.3V ± 10%, GND = 0V; T_A = –40°C to +85°C, R_L is 100Ω across the output pair, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{DD}	Power Supply Voltage Range		3.0	3.3	3.6	V
V_{DDO}	Output Voltage Range		1.71		3.6	V
I_{DDT}	Total Supply Current	No load Max. V_{DD}, V_{DDO}, V_{DDA} Max. Frequency		85	120	mA
R_{DIFF_IN}	Differential Input Resistance (Ref-IN-to-/Ref-IN)		85	100	115	Ω
V_{IH}	Input HIGH Voltage (Ref-IN-to-/Ref-IN)	Ref-IN, /Ref-IN	1.2		V_{CC}	V
V_{IL}	Input LOW Voltage (Ref-IN, /Ref-IN)	Ref-IN, /Ref-IN	0		V_{IH}–0.1	V
V_{IN}	Input Voltage Swing (Ref-IN, /Ref-IN)	Note 6	0.1		1.7	V
V_{DIFF_IN}	Differential Input Voltage Swing (|Ref-IN – /Ref-IN|)		0.2			V
V_{REF-AC}	Output Reference Voltage		V_{DD}–1.5	V_{DD}–1.4	V_{DD}–1.3	V
V_{T_IN}	Voltage from Input to V_T				1.28	V

Notes:

1. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.
2. Due to the limited drive capability, use for input of the same package only.
3. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
4. Package thermal resistance assumes exposed pad is soldered (or equivalent) to the device's most negative potential on the PCB. ψ_{JB} and θ_{JA} values are determined for a 4-layer board in still-air number, unless otherwise stated.
5. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.
6. V_{IN} (max) is specified when V_T is floating.

CML Output DC Electrical Characteristics[7]

V_{DDA}, V_{DD} =+3.3V ±10%, V_{DDO} = +1.71V to 3.6V, GND and GNDO = 0V, R_L = 100Ω across the outputs; T_A = –40°C to +85°C, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OH}	Output HIGH Voltage	R_L = 50Ω to V_{DDO}	V_{DDO}-0.13	V_{DDO}-0.085	V_{DDO}-0.04	V
V_{OL}	Output LOW Voltage	R_L = 50Ω to V_{DDO}	V_{DDO}-0.63	V_{DDO}-0.485	V_{DDO}-0.34	V
V_{OUT}	Output Voltage Swing	See Figure 3a	300	400	500	mV
V_{DIFF_OUT}	Differential Output Voltage Swing	See Figure 3b	600	800	1000	mV
R_{OUT}	Output Source Impedance		40	50	60	Ω

LVTTL/CMOS DC Electrical Characteristics[7]

V_{DDC} = 3.3V ±10%, GND = 0V, T_A = –40°C to + 85°C, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input HIGH Voltage		2.5			V
V_{IL}	Input LOW Voltage				0.8	V
V_{OH}	Output High Voltage	$I_{OH}/I_{OL} \leq 4$ mA	2.7			V
V_{OL}	Output Low Voltage	$I_{OH}/I_{OL} \leq 4$ mA			0.2	V
I_{IH}	Input HIGH Current		-1		3	µA
I_{IL}	Input LOW Current		-5		1	µA

FREQSEL DC Electrical Characteristics[7]

V_{DDC} = 3.3V ±10%, GND = 0V, T_A = –40°C to + 85°C, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input HIGH Voltage		2.5			V
V_{IL}	Input LOW Voltage				0.8	V
V_{OH}	Output High Voltage	$I_{OH}/I_{OL} \leq 4$ mA	2.7			V
V_{OL}	Output Low Voltage	$I_{OH}/I_{OL} \leq 4$ mA			0.2	V
V_{IM}	Input MID Voltage		Vdd/2 – 0.1	Vdd/2	Vdd/2 + 0.1	V
I_{IH}	Input HIGH Current		5		50	µA
I_{IL}	Input LOW Current		-50		-5	µA

Notes:

7. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

AC Electrical Characteristics

V_{DDA}, V_{DDC} =+3.3V ±10%, GND and GNDO = 0V, R_L = 100Ω across the outputs; Input $t_r/t_f \leq$ 400ps; T_A = –40°C to +85°C, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{IN}	Input Frequency Range	V_{IN} > 100mV Clock	19.44		694	MHz
f_{OUT}	Output Frequency Range	V_{OUT} > 200mV Clock	77.75		694	MHz
f_{VCO}	Internal VCO frequency		1244		1388	MHz
LOL	Maximum I/O frequency	PLL out of Lock, ~4ms sustained I/O difference	-1000		1000	ppm
T_{LOCK}	Acquisition Lock Time[8]	I/O frequency = 155MHz			450	ms
		Max VCO frequency			550	ms
REFIN t_r, t_f	Input Rise/Fall Times	20% to 80%			400	ps
CLKOUT t_r, t_f	Output Rise/Fall Times	20% to 80%	110	160	250	ps
RefIn C_{Duty}	Input Duty Cycle		40		60	%
CLKOut C_{Duty}	Output Duty Cycle		48	50	52	%
BW	Loop Bandwidth, locked	BW1 = 0, BW0 = 0	750	1000	1250	Hz
		BW1 = 0, BW0 = 1	1500	2000	2500	Hz
		BW1 = 1, BW0 = 0	3750	5000	6250	Hz
		BW1 = 1, BW0 = 1	7500	10000	12500	Hz

Notes:

8. Reset Low-to-High to LOL High-to-Low.

Jitter Characteristics[9]

V_{DDA}, V_{DD} =+3.3V ±10%, GND= 0V, R_L = 100Ω across the outputs; Input t_r/t_f < 400ps; T_A = –40°C to +85°C, unless otherwise stated. Contact factory for 1kHz and 2kHz Loop Bandwidth Transfer Characteristics.

BW Setting: 1kHz, BW1:0 = 00

Symbol	Parameter	Condition	Min	Typ	Max	Units
J_{Gen}	CLKOUT **RMS** Jitter Generation	12kHz to 20MHz (Ideal ref input and supply)		1	2	ps_{RMS}
		50kHz to 80MHz (Ideal ref input and supply)		1	2	
J_{TOL}	Jitter Tolerance			10		ns
F_{BW}	Jitter Transfer Bandwidth	LBW = 1kHz		1000		Hz
J_P	Jitter Peaking	<1kHz			0.1	dB

BW Setting: 2kHz, BW1:0 = 01

Symbol	Parameter	Condition	Min	Typ	Max	Units
JGen	CLKOUT **RMS** Jitter Generation	12kHz to 20MHz (Ideal ref input and supply)		1	2	psRMS
		50kHz to 80MHz (Ideal ref input and supply)		1	2	
JTOL	Jitter Tolerance			10		ns
FBW	Jitter Transfer Bandwidth	LBW = 2kHz		2000		Hz
JP	Jitter Peaking	<1kHz			0.1	dB

BW Setting: 5kHz, BW1:0 = 10

Symbol	Parameter	Condition	Min	Typ	Max	Units
JGen	CLKOUT RMS Jitter Generation	12kHz to 20MHz (Ideal ref input and supply)		1	2	psRMS
		50kHz to 80MHz (Ideal ref input and supply)		1	2	
JTOL	Jitter Tolerance			10		ns
FBW	Jitter Transfer Bandwidth	LBW = 5kHz		5000		Hz
JP	Jitter Peaking	<1kHz			0.1	dB

BW Setting: 10kHz, BW1:0 = 11

Symbol	Parameter	Condition	Min	Typ	Max	Units
JGen	CLKOUT RMS Jitter Generation	12kHz to 20MHz (Ideal ref input and supply)		1	2	psRMS
		50kHz to 80MHz (Ideal ref input and supply)		1	2	
JTOL	Jitter Tolerance			10		ns
FBW	Jitter Transfer Bandwidth	LBW = 10kHz		10,000		Hz
JP	Jitter Peaking	<1kHz			0.1	dB

Note:

9. 5k and 10k loop bandwidth settings are recommended due to better jitter performance with jitter bandwidth below 12K Hz. The use of 1k and 2k bandwidth settings may be acceptable in certain applications where jitter bandwidth is limited to above 12K Hz. Please contact the factory for additional information.

Functional Description

Overall Function

The SY89610L is designed to accept a high-jitter signal and provide an ultra-low jitter and ultra-low phase noise CML compatible clock signal. Unlike normal buffers, the SY89610L is a jitter attenuator since it does not transfer jitter across from input to output. This makes this product an ideal solution for precision clock applications.

LC Voltage Control Oscillator (VCO)

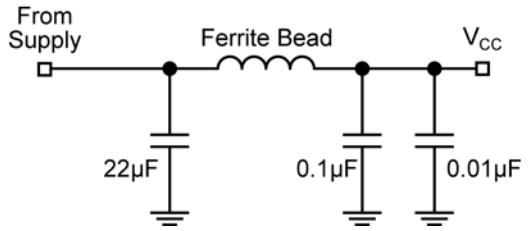
The SY89610L uses an extremely low phase noise VCO to prevent jitter at the output. At low frequencies, the PLL produces more phase noise. To offset the noise, the LC VCO provides an extremely low phase noise signal that feeds to the output circuit. Unlike many competitive VCOs, this VCO only requires a single external component, which is a filter capacitor.

External Loop Filter Considerations

The SY89610L features an external PLL loop filter that allows the user to tailor the PLLs behavior. It is recommended that ceramic capacitors with NOP or X7R dielectric be used because they have very low effective series resistance. All other filter components are on-chip. Internally, the filter has a resistor in series with the external capacitor and a much smaller capacitor in parallel with the series combination of the internal resistor and external capacitor. The selectable PLL bandwidths from 1kHz-to-10kHz allows the user to select between different loop filter values. The external capacitor must be placed as close to the device pins as possible. While laying out the board, keep any supply or signal traces lines away from the capacitor. Loop filter capacitor layout should include a quiet ground plane under the loop filter capacitor and loop filter pins.

Power Supply Filtering Techniques

As with any high-speed integrated circuit, power supply filtering is very important. At a minimum, VDDA, VDD, and all VDDO pins should be individually connected using via to the power supply plane, and separate bypass capacitors should be used for each pin. To achieve optimal jitter performance, each power supply pin should use separate instances of the circuit shown in Power Supply Scheme below.



Power Supply Scheme

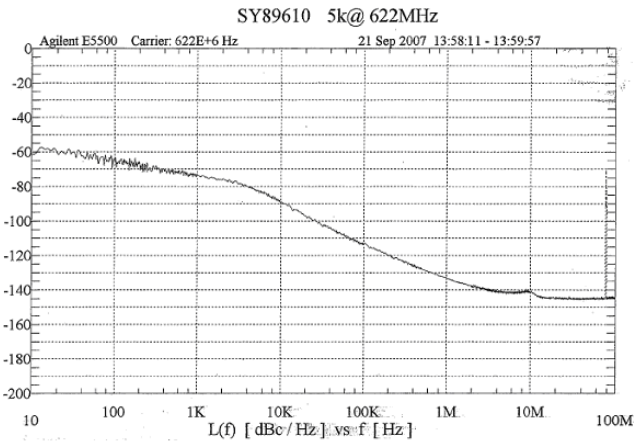
Jitter Generation

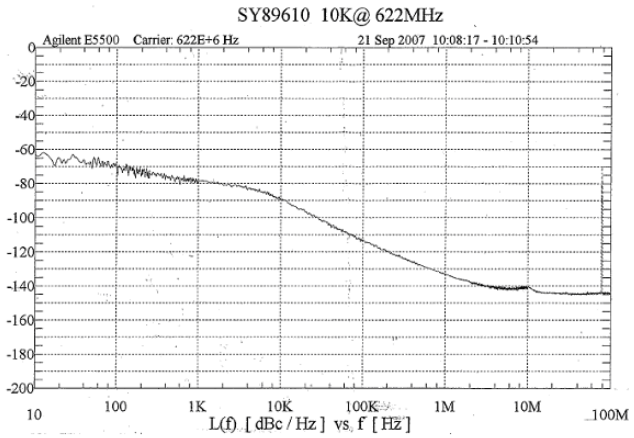
Jitter generation is the amount of jitter generated by the part at the output when there is no jitter present at the input clock. While the VCO and PLL are sources of jitter in a synthesizer, the different loop bandwidth options aid in reducing jitter. The SY89610L guarantees less than $2ps_{RMS}$. See Jitter characteristics subsection.

Phase Noise

The SY89610L has very low phase noise at 1kHz offset from the center frequency. Phase noise is measured at the output with a jitter-free signal injected at the input. The loop bandwidth settings have a minor impact on the phase noise values. For 10kHz loop bandwidth, we guarantee the phase noise less than -80dBc/Hz. See Phase Noise curve.

Phase Noise Characteristics





Input and Output Stage

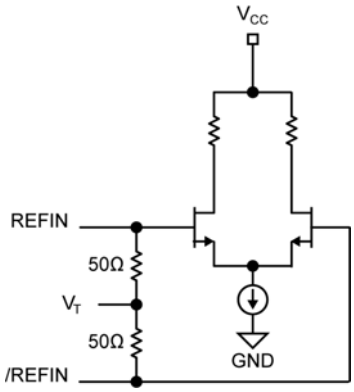


Figure 1a. Simplified Differential Input Buffer

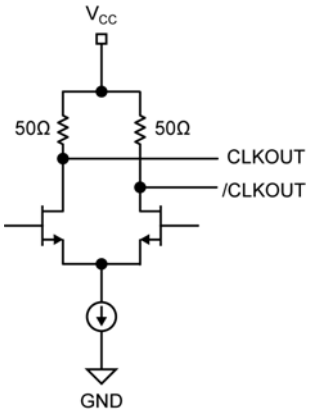


Figure 1b. Simplified CML Output Buffer

Single-Ended and Differential Swings

Figure 2a. Single-Ended Swing

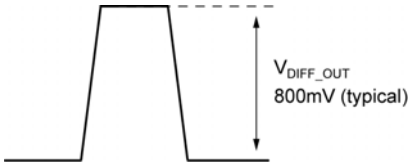


Figure 2b. Differential Swing

Input Interface Applications

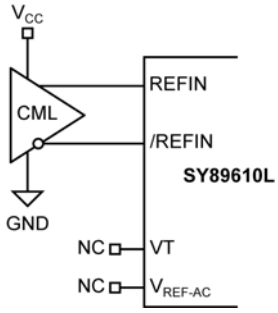


Figure 3a. CML Interface (DC-Coupled)

Option: May connect V_T to V_{CC}

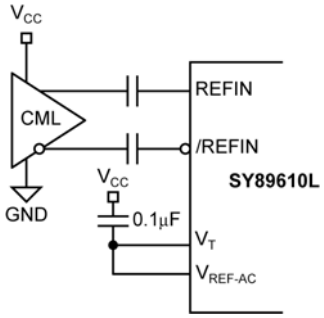


Figure 3b. CML Interface (AC-Coupled)

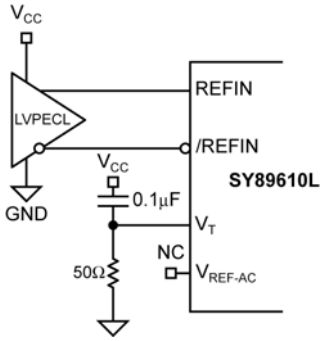


Figure 3c. LVPECL Interface (DC-Coupled)

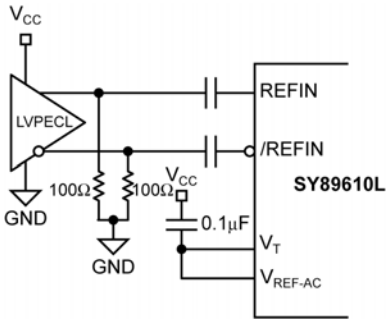


Figure 3d. LVPECL Interface (AC-Coupled)

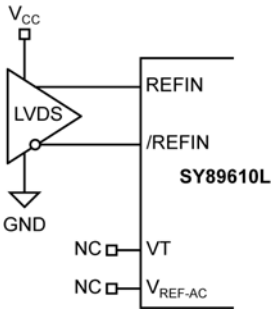


Figure 3e. LVDS Interface

CML Output Termination

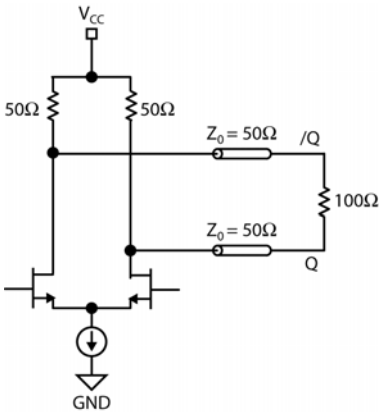


Figure 4a. CML DC-Coupled Termination

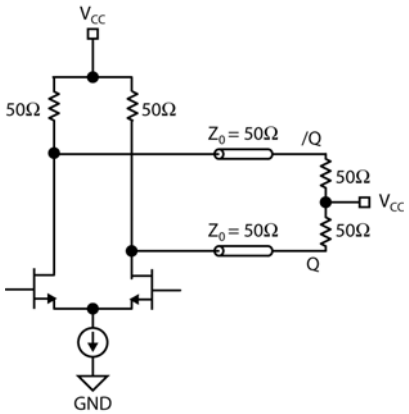


Figure 4b. CML DC-Coupled Termination

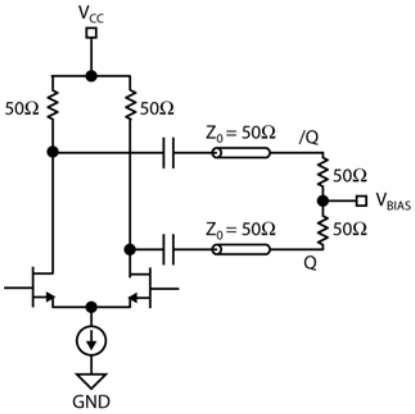
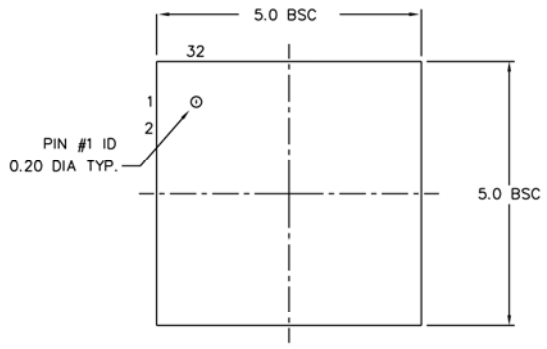
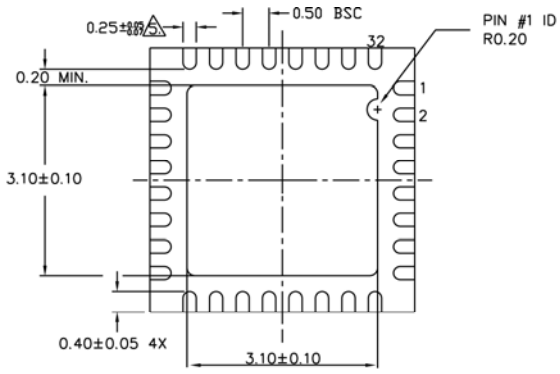


Figure 4c. CML AC-Coupled Termination

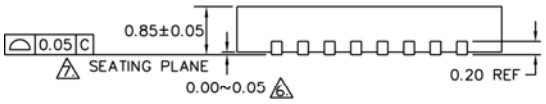
Package Information



TOP VIEW



BOTTOM VIEW



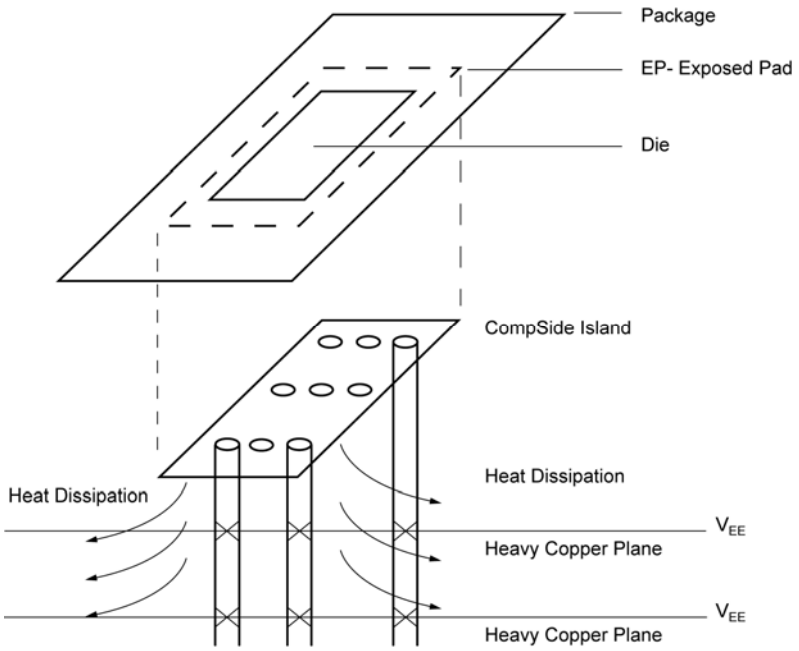
SIDE VIEW

NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. MAX. PACKAGE WARPAGE IS 0.05 mm.
3. MAXIMUM ALLOWABE BURRS IS 0.076 mm IN ALL DIRECTIONS.
4. PIN #1 ID ON TOP WILL BE LASER/INK MARKED.
5. DIMENSION APPLIES TO METALIZED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25 mm FROM TERMINAL TIP.
6. APPLIED ONLY FOR TERMINALS.
7. APPLIED FOR EXPOSED PAD AND TERMINALS.

32-Pin (5mm x 5mm) QFN

Packages Notes:

1. Package meets Level 2 Moisture Sensitivity Classification.
2. All parts are dry-packed before shipment.
3. Exposed pad must be soldered to ground for proper thermal management



PCB Thermal Consideration for 32-pin QFN Package

(Always solder, or equivalent, the exposed pad to the PCB)

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