TPS7A49 36-V, 150-mA, Ultralow-Noise, Positive Linear Regulator

1 Features

- Input Voltage Range: 3 V to 36 V
- Noise:
  - 12.7 μV_{RMS} (20 Hz to 20 kHz)
  - 15.4 μV_{RMS} (10 Hz to 100 kHz)
- Power-Supply Ripple Rejection:
  - 72 dB (120 Hz)
  - ≥ 52 dB (10 Hz to 400 kHz)
- Adjustable Output: 1.194 V to 33 V
- Output Current: 150 mA
- Dropout Voltage: 260 mV at 100 mA
- Stable with Ceramic Capacitors ≥ 2.2 μF
- CMOS Logic-Level-Compatible Enable Pin
- Fixed Current-Limit and Thermal Shutdown Protection
- Packages: 8-Pin HVSSOP PowerPAD™ and 3-mm × 3-mm VSON
- Operating Temperature Range: –40°C to 125°C

2 Applications

- Supply Rails for Op Amps, DACs, ADCs, and Other High-Precision Analog Circuitry
- Audio
- Post DC-DC Converter Regulation and Ripple Filtering
- Test and Measurement
- Rx, Tx, and PA Circuitry
- Industrial Instrumentation
- Base Stations and Telecom Infrastructure

3 Description

The TPS7A49 series of devices are positive, high-voltage (36 V), ultralow-noise (15.4 μV_{RMS}, 72-dB PSRR) linear regulators that can source a 150-mA load.

These linear regulators include a CMOS logic-level-compatible enable pin and capacitor-programmable soft-start function that allows for customized power-management schemes. Other available features include built-in current limit and thermal shutdown protection to safeguard the device and system during fault conditions.

The TPS7A49 family is designed using bipolar technology, and is ideal for high-accuracy, high-precision instrumentation applications where clean voltage rails are critical to maximize system performance. This design makes the device an excellent choice to power operational amplifiers, analog-to-digital converters (ADCs), digital-to-analog converters (DACs), and other high-performance analog circuitry.

In addition, the TPS7A49 family of linear regulators is suitable for post dc-dc converter regulation. By filtering out the output voltage ripple inherent to dc-dc switching conversion, maximum system performance is provided in sensitive instrumentation, test and measurement, audio, and RF applications.

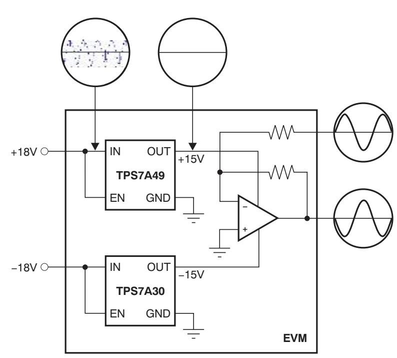
For applications where positive and negative high-performance rails are required, consider TI's TPS7A30xx family of negative high-voltage, ultralow-noise linear regulators as well.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS7A49	HVSSOP PowerPAD (8)	3.00 mm × 3.00 mm
	VSON (8)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Post DC-DC Converter Regulation for High-Performance Analog Circuitry



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (March 2015) to Revision E	Page
• Added DRB package to document	1
• Added TI Design	1
• Changed Shutdown Protection *Features* bullet: removed *Integrated*	1
• Changed *Packages* Features bullet	1
• Added VSON row to *Device Information* table	1
• Added DRB package to *Pin Configuration and Functions* section	4
• Changed *Pin Functions* table: changed EN (changed $V_{EN} \leq V_{EN(low)}$) and FB (deleted *control-loop* from first sentence) pin descriptions	4
• Added DRB column to *Thermal Information* table	6
• Changed 35°C to 45°C in *Thermal Protection* section	13
• Changed T_J value for disabled mode in Table 1 to match *Electrical Characteristics* table	13
• Changed first sentence of *Application Information* section	14
• Changed first sentence of *Post DC-DC Converter Filtering* section	15
• Changed Equation 3	17
• Changed *1.27 kΩ* to *100 kΩ* in description of R_2 setting in the *Detailed Design Procedure* section	17
• Added third paragraph and Figure 36 to *Power Dissipation* section	20
• Changed capacitor size value in footnote of Figure 37	21

Changes from Revision C (December 2013) to Revision D	Page
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1
• Changed 9th bullet in *Features* list	1
• Removed pin drawing from front page of data sheet	1
• Revised *Thermal Information* table values	6

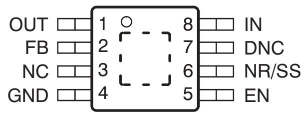
Changes from Revision B (January 2010) to Revision C — **Page**

Changes from Revision A (September 2010) to Revision B — **Page**

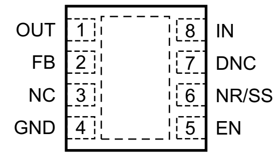
Changes from Original (August 2010) to Revision A — **Page**

5 Pin Configuration and Functions

DGN Package
8-Pin HVSSOP PowerPAD
Top View



DRB Package
VSON-8
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
DNC	7	—	Do not connect. Do not route this pin to any electrical net, not even GND or IN.
EN	5	I	This pin turns the regulator on or off. If $V_{EN} \geq V_{EN(high)}$, the regulator is enabled. If $V_{EN} \leq V_{EN(low)}$, the regulator is disabled. The EN pin can be connected to IN, if not used. $V_{EN} \leq V_{IN}$.
FB	2	I	This pin is the input to the error amplifier. FB is used to set the output voltage of the device.
GND	4	—	Ground
IN	8	I	Input supply
NC	3	—	Not internally connected. This pin can either be left open or tied to GND.
NR/SS	6	—	Noise-reduction pin. Connecting an external capacitor to this pin bypasses noise generated by the internal band gap. This capacitor allows RMS noise to be reduced to very low levels and also controls the soft-start function.
OUT	1	O	Regulator output. A capacitor ≥ 2.2 µF must be tied from this pin to ground to ensure stability.
PowerPAD		—	Must either be left open or tied to ground. Solder to the printed-circuit-board (PCB) plane to enhance thermal performance.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	IN pin to GND pin	–0.3	36	V
	OUT pin to GND pin	–0.3	33	V
	OUT pin to IN pin	–36	0.3	V
	FB pin to GND pin	–0.3	2	V
	FB pin to IN pin	–36	0.3	V
	EN pin to IN pin	–36	0.3	V
	EN pin to GND pin	–0.3	36	V
	NR/SS pin to IN pin	–36	0.3	V
	NR/SS pin to GND pin	–0.3	2	V
Current	Peak output	Internally limited		
Temperature	Operating virtual junction, T_J	–40	125	°C
	Storage, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±1500	V
		Charged device model (CDM), per JEDEC specification JESD22-C101 (2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input supply voltage	3		35	V
V_{EN}	Enable supply voltage	0		V_{IN}	V
V_{OUT}	Output voltage	V_{FB}		33	V
I_{OUT}	Output current	0		150	mA
T_J	Operating junction temperature	–40		125	°C
C_{IN}	Input capacitor	2.2	10		µF
C_{OUT}	Output capacitor	2.2	10		µF
C_{NR}	Noise reduction capacitor	0	10		nF
C_{FF}	Feed-forward capacitor	0	10		nF
R_2	Lower feedback resistor			237	kΩ

6.4 Thermal Information

THERMAL METRIC(1)		TPS7A49 DGN (HVSSOP PowerPAD) 8 PINS	TPS7A49 DRB (VSON) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	63.4	47.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	53	55.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	37.4	23.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	3.7	1.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	37.1	23.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	13.5	7.0	°C/W

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.

6.5 Electrical Characteristics

At T_J = –40°C to 125°C, $V_{IN} = V_{OUT(nom)}$ + 1 V or V_{IN} = 3 V (whichever is greater), $V_{EN} = V_{IN}$, I_{OUT} = 1 mA, C_{IN} = 2.2 µF, C_{OUT} = 2.2 µF, $C_{NR/SS}$ = 0 nF, and the FB pin tied to OUT, unless otherwise noted. Typical values are at T_A = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range		3		35	V
V_{REF}	Internal reference(1)	T_J = 25°C, $V_{NR/SS} = V_{REF}$	1.176	1.188	1.212	V
V_{FB}	Feedback voltage			1.185		V
V_{OUT}	Output voltage range(2)	$V_{IN} \geq V_{OUT(nom)}$ + 1 V	V_{REF}		33	V
	Nominal accuracy	T_J = 25°C, $V_{IN} = V_{OUT(nom)}$ + 0.5 V	–1.5		1.5	$\%V_{OUT}$
	Overall accuracy	$V_{OUT(nom)}$ + 1 V ≤ V_{IN} ≤ 35 V, 1 mA ≤ I_{OUT} ≤ 150 mA	–2.5		2.5	$\%V_{OUT}$
$\frac{\Delta V_{OUT}(\Delta V_{IN})}{V_{OUT(NOM)}}$	Line regulation	T_J = 25°C, $V_{OUT(nom)}$ + 1 V ≤ V_{IN} ≤ 35 V		0.086		$\%V_{OUT}$
$\frac{\Delta V_{OUT}(\Delta I_{OUT})}{V_{OUT(NOM)}}$	Load regulation	T_J = 25°C, 1 mA ≤ I_{OUT} ≤ 150 mA		0.04		$\%V_{OUT}$
V_{DO}	Dropout voltage	V_{IN} = 95% $V_{OUT(nom)}$, I_{OUT} = 100 mA		260		mV
		V_{IN} = 95% $V_{OUT(nom)}$, I_{OUT} = 150 mA		333	600	mV
I_{LIM}	Current limit	V_{OUT} = 90% $V_{OUT(nom)}$	220	309	500	mA
I_{GND}	Ground current	I_{OUT} = 0 mA		49	100	µA
		I_{OUT} = 100 mA		800		µA
I_{SHDN}	Shutdown supply current	V_{EN} = 0.4 V		0.8	3	µA
I_{FB}	Feedback current(3)			3	100	nA
I_{EN}	Enable current	$V_{EN} = V_{IN} = V_{OUT(nom)}$ + 1 V		0.02	1	µA
		$V_{EN} = V_{IN}$ = 35 V		0.2	1	µA
$V_{EN(high)}$	Enable high-level voltage		2.1		V_{IN}	V
$V_{EN(low)}$	Enable low-level voltage		0		0.4	V
V_n	Output noise voltage	V_{IN} = 3 V, $V_{OUT(nom)} = V_{REF}$, C_{OUT} = 10 µF, $C_{NR/SS}$ = 10 nF, BW = 10 Hz to 100 kHz		15.4		μV_{RMS}
		V_{IN} = 6.2 V, $V_{OUT(nom)}$ = 5 V, C_{OUT} = 10 µF, $C_{NR/SS}$ = C_{FF}(4) = 10 nF, BW = 10 Hz to 100 kHz		21.15		μV_{RMS}
PSRR	Power-supply rejection ratio	V_{IN} = 6.2 V, $V_{OUT(nom)}$ = 5 V, C_{OUT} = 10 µF, $C_{NR/SS}$ = C_{FF}(4) = 10 nF, f = 120 Hz		72		dB
T_{sd}	Thermal shutdown temperature	Shutdown, temperature increasing		170		°C
		Reset, temperature decreasing		150		°C
T_J	Operating junction temperature		–40		125	°C

(1) V_{REF} is measured at the NR/SS pin.
(2) To ensure stability at no load conditions, a current from the feedback resistive network equal to or greater than 5 µA is required.
(3) I_{FB} > 0 flows out of the device.
(4) C_{FF} refers to a feed-forward capacitor connected to the FB and OUT pins.

6.6 Typical Characteristics

At T_J = –40°C to 125°C, V_{IN} = $V_{OUT(nom)}$ + 1 V or V_{IN} = 3 V (whichever is greater), V_{EN} = V_{IN}, I_{OUT} = 1 mA, C_{IN} = 2.2 µF, C_{OUT} = 2.2 µF, $C_{NR/SS}$ = 0 nF, and the FB pin tied to OUT, unless otherwise noted. Typical values are at T_A = 25°C.

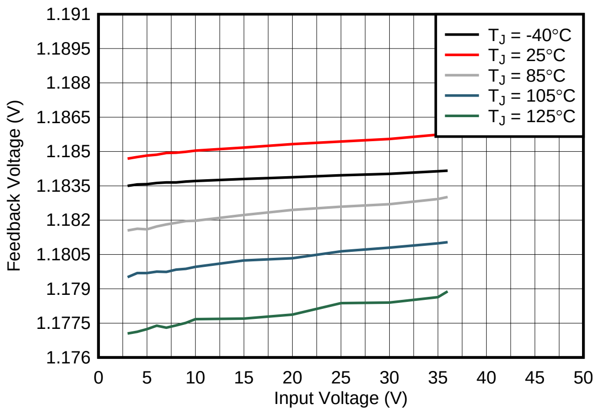


Figure 1. Feedback Voltage vs Input Voltage

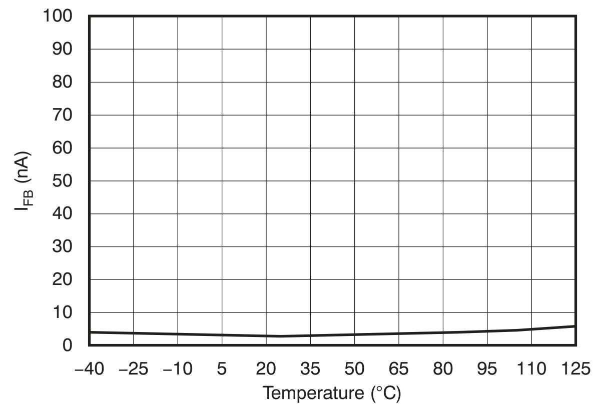


Figure 2. Feedback Current vs Temperature

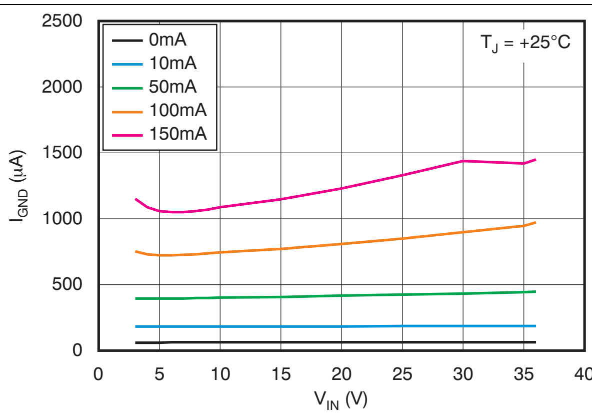


Figure 3. Ground Current vs Input Voltage

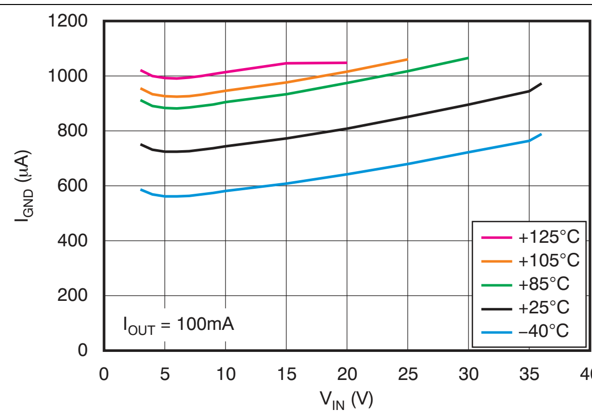


Figure 4. Ground Current vs Input Voltage

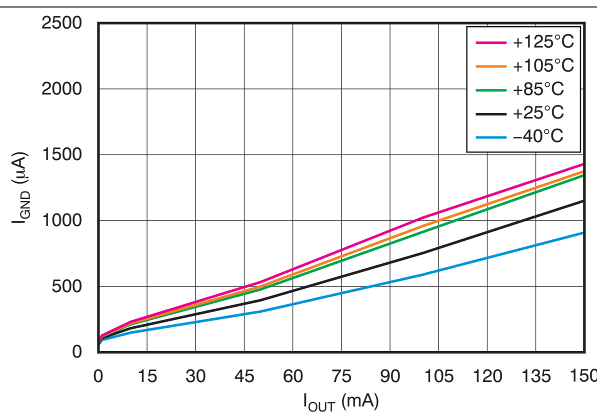


Figure 5. Ground Current vs Output Current

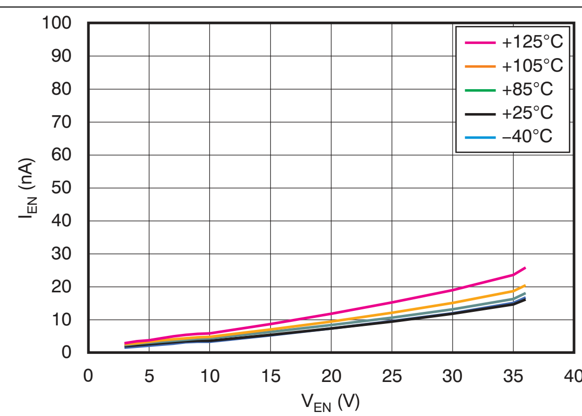


Figure 6. Enable Current vs Enable Voltage

Typical Characteristics (continued)

At T_J = –40°C to 125°C, $V_{IN} = V_{OUT(nom)}$ + 1 V or V_{IN} = 3 V (whichever is greater), $V_{EN} = V_{IN}$, I_{OUT} = 1 mA, C_{IN} = 2.2 µF, C_{OUT} = 2.2 µF, $C_{NR/SS}$ = 0 nF, and the FB pin tied to OUT, unless otherwise noted. Typical values are at T_A = 25°C.

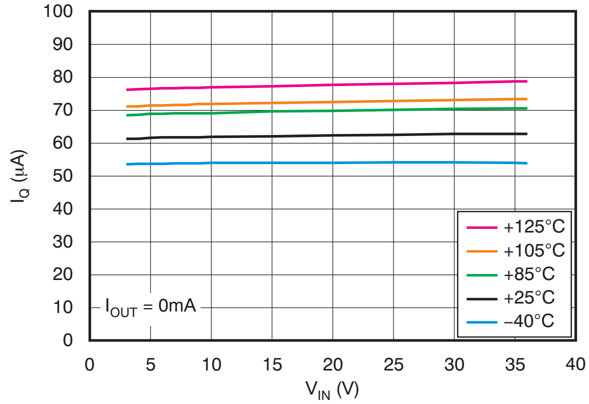


Figure 7. Quiescent Current vs Input Voltage

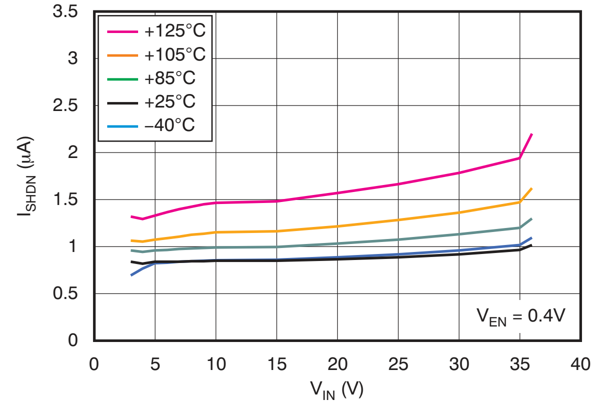


Figure 8. Shutdown Current vs Input Voltage

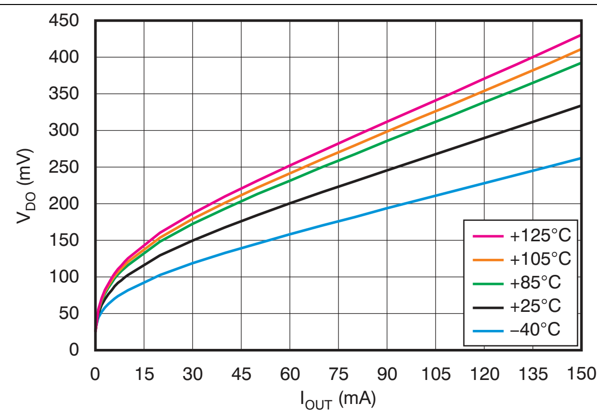


Figure 9. Dropout Voltage vs Output Current

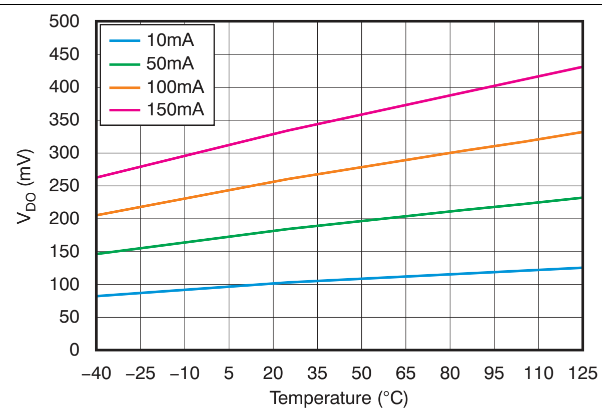


Figure 10. Dropout Voltage vs Temperature

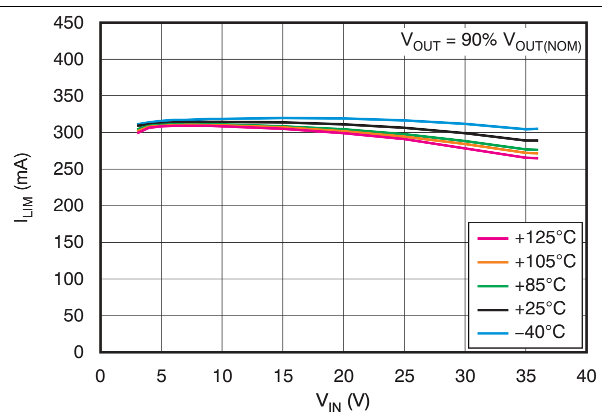


Figure 11. Current Limit vs Input Voltage

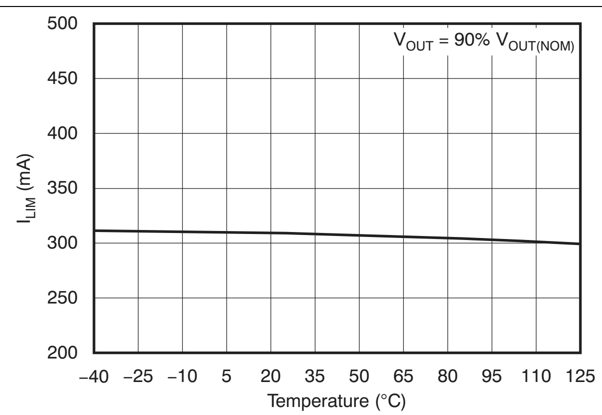


Figure 12. Current Limit vs Temperature

Typical Characteristics (continued)

At T_J = –40°C to 125°C, V_{IN} = $V_{OUT(nom)}$ + 1 V or V_{IN} = 3 V (whichever is greater), V_{EN} = V_{IN}, I_{OUT} = 1 mA, C_{IN} = 2.2 µF, C_{OUT} = 2.2 µF, $C_{NR/SS}$ = 0 nF, and the FB pin tied to OUT, unless otherwise noted. Typical values are at T_A = 25°C.

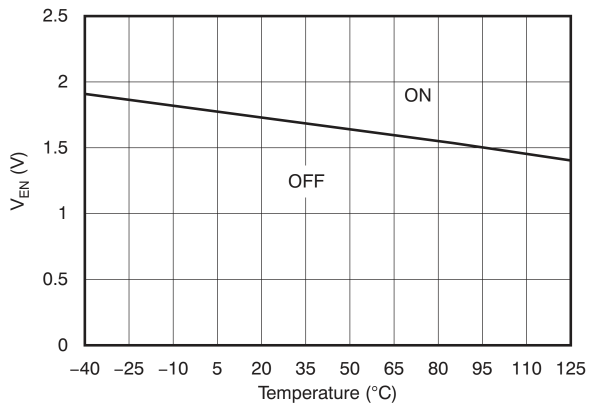


Figure 13. Enable Threshold Voltage vs Temperature

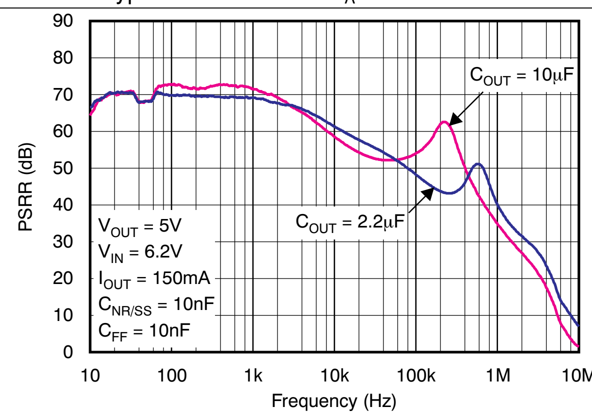


Figure 14. Power-Supply Rejection Ratio vs C_{OUT}

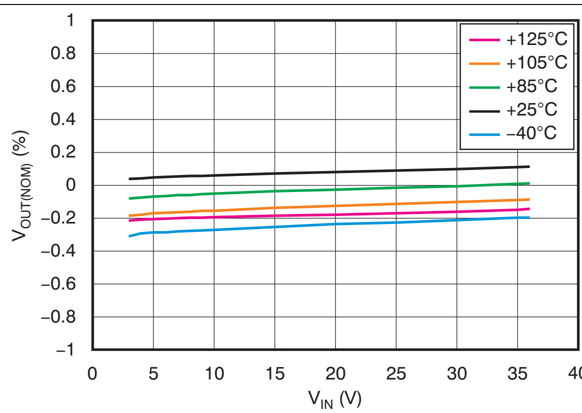


Figure 15. Line Regulation

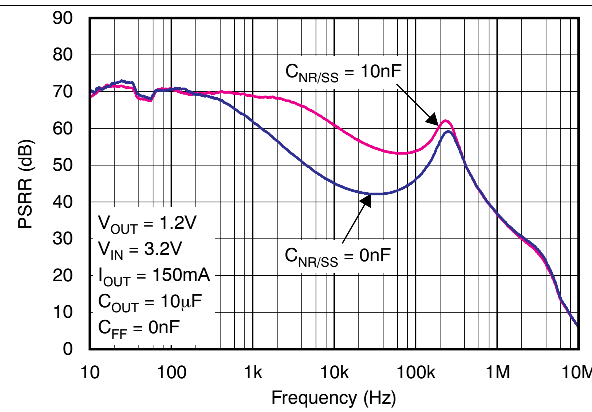


Figure 16. Power-Supply Rejection Ratio vs $C_{NR/SS}$

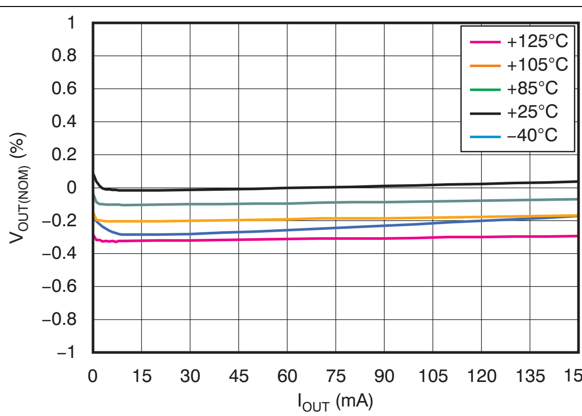


Figure 17. Load Regulation

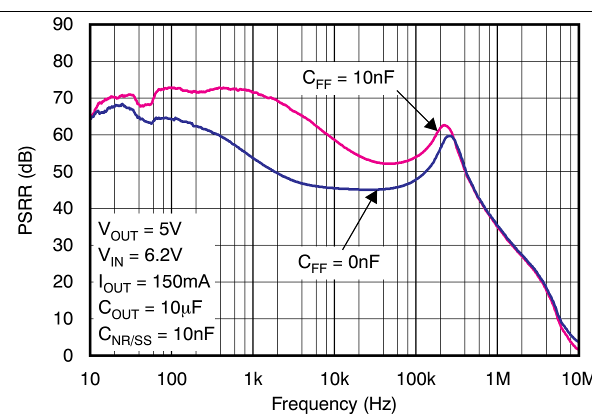


Figure 18. Power-Supply Rejection Ratio vs C_{FF}

Typical Characteristics (continued)

At T_J = –40°C to 125°C, V_{IN} = $V_{OUT(nom)}$ + 1 V or V_{IN} = 3 V (whichever is greater), V_{EN} = V_{IN}, I_{OUT} = 1 mA, C_{IN} = 2.2 µF, C_{OUT} = 2.2 µF, $C_{NR/SS}$ = 0 nF, and the FB pin tied to OUT, unless otherwise noted. Typical values are at T_A = 25°C.

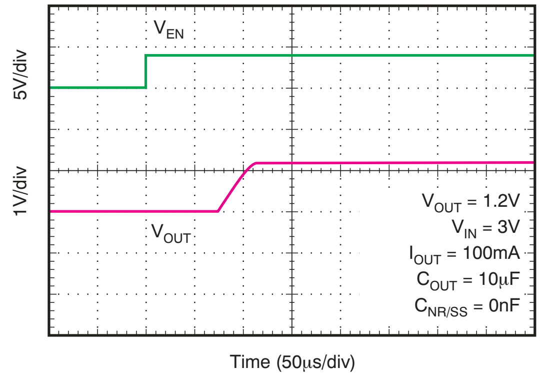


Figure 19. Capacitor-Programmable Soft-Start

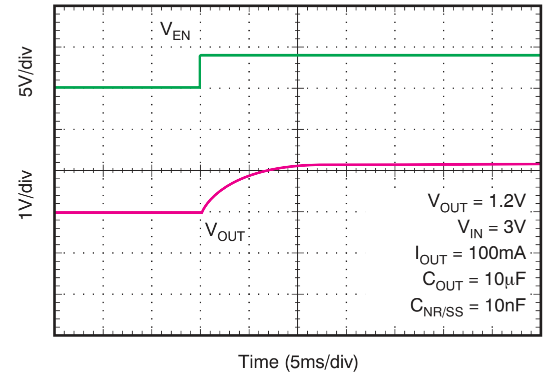


Figure 20. Capacitor-Programmable Soft-Start

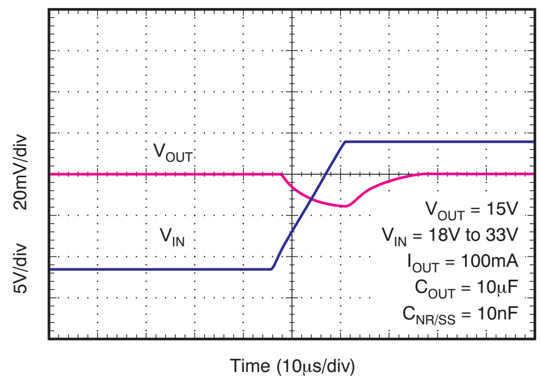


Figure 21. Line Transient Response

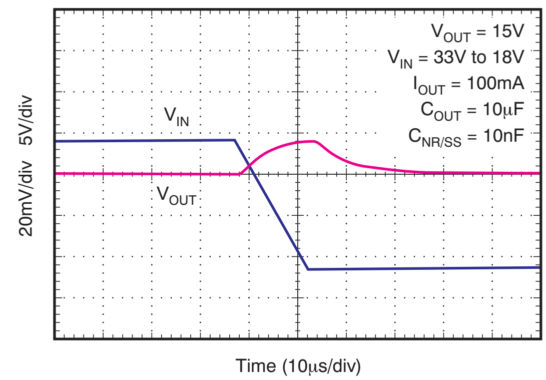


Figure 22. Line Transient Response

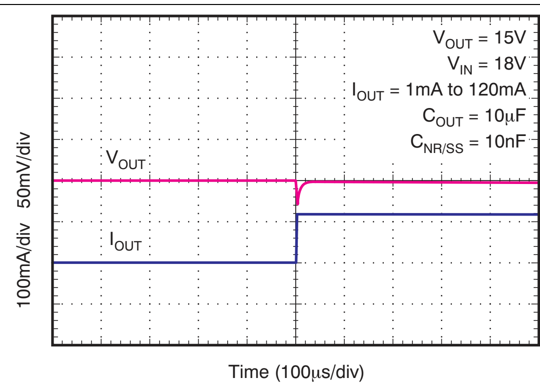


Figure 23. Load Transient Response

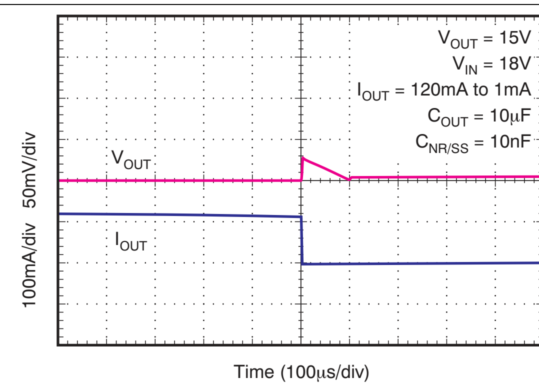
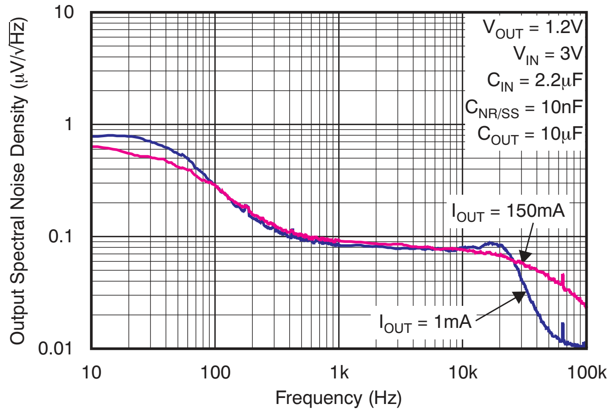


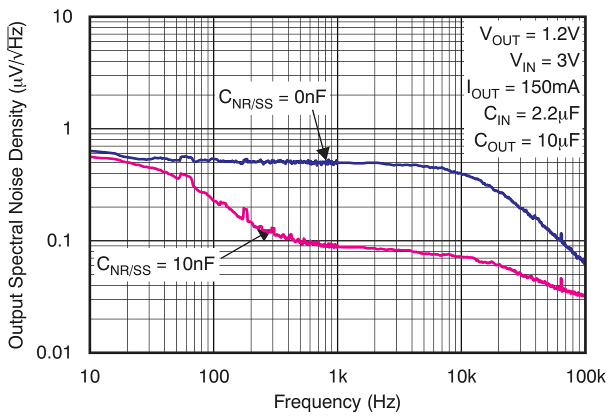
Figure 24. Load Transient Response

7 Parameter Measurement Information



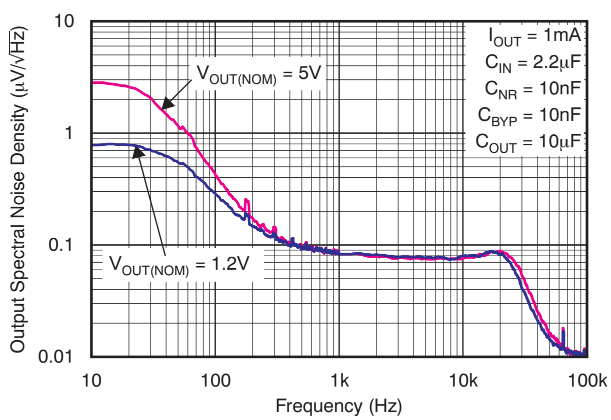
I_{OUT}	RMS NOISE	
	10Hz to 100kHz	100Hz to 100kHz
1mA	15.44	14.14
150mA	17.27	16.46

Figure 25. Output Spectral Noise Density vs Output Current



$C_{NR/SS}$	RMS NOISE	
	10Hz to 100kHz	100Hz to 100kHz
0nF	69.04	67.87
10nF	16.58	15.86

Figure 26. Output Spectral Noise Density vs $C_{NR/SS}$



$V_{OUT(NOM)}$	RMS NOISE	
	10Hz to 100kHz	100Hz to 100kHz
5V	21.15	14.74
1.2V	15.44	14.14

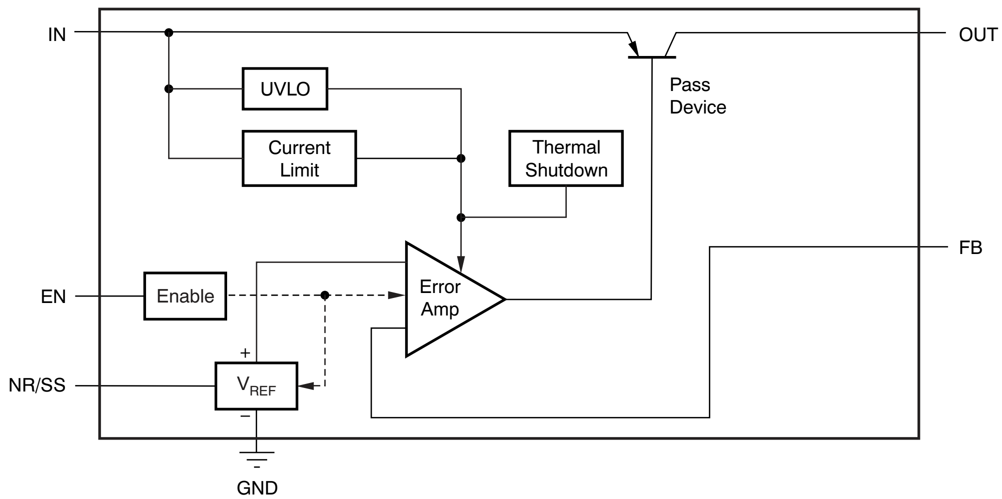
Figure 27. Output Spectral Noise Density vs $V_{OUT(NOM)}$

8 Detailed Description

8.1 Overview

The TPS7A49 family of devices are wide V_{IN}, low-noise, 150-mA linear regulators (LDOs). These devices feature an enable pin, programmable soft-start, current limiting, and thermal protection circuitry that allow the device to be used in a wide variety of applications. As bipolar-based devices, the TPS7A49 family are ideal for high-accuracy, high-precision applications at higher voltages.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Internal Current Limit

The fixed internal current limit of the TPS7A49 family helps protect the regulator during fault conditions. The maximum amount of current the device can source is the current limit (309 mA, typical), and is largely independent of output voltage. For reliable operation, the device does not operate in current limit for extended periods of time.

8.3.2 Programmable Soft-Start

The NR capacitor also functions as a soft-start capacitor to slow down the rise time of the output. The rise time of the output when using an NR capacitor is governed by Equation 1. In Equation 1, t_{SS} is the soft-start time in milliseconds, and $C_{NR/SS}$ is the capacitance at the NR pin in nanofarads.

$$t_{SS}\ (ms) = 1.4 \times C_{NR/SS}\ (nF) \quad (1)$$

8.3.3 Enable Pin Operation

The TPS7A49 provides an enable feature (EN) that turns on the regulator when $V_{EN} > V_{EN(high)}$ and disables the device when $V_{EN} < V_{EN(low)}$.

8.3.4 Thermal Protection

Thermal protection disables the output when the junction temperature rises to approximately 170°C, allowing the device to cool. When the junction temperature cools to approximately 150°C, the output circuitry is enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit can cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage as a result of overheating.

Feature Description (continued)

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, limit junction temperature to a maximum of 125°C. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, trigger thermal protection at least 45°C above the maximum expected ambient condition of a particular application. This configuration produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS7A49 is designed to protect against overload conditions. The protection circuitry is not intended to replace proper heatsinking. Continuously running the TPS7A49 into thermal shutdown degrades device reliability.

8.4 Device Functional Modes

8.4.1 Normal Operation

The device regulates to the nominal output voltage under the following conditions:

- The input voltage is at least as high as $V_{IN(min)}$.
- The input voltage is greater than the nominal output voltage added to the dropout voltage.
- The enable voltage has previously exceeded the enable rising threshold voltage and has not decreased below the enable falling threshold.
- The output current is less than the current limit.
- The device junction temperature is less than the maximum specified junction temperature.

8.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this mode of operation, the output voltage is the same as the input voltage minus the dropout voltage. The transient performance of the device is significantly degraded because the pass device (such as a bipolar junction transistor, or BJT) is in saturation and no longer controls the current through the LDO. Line or load transients in dropout can result in large output voltage deviations.

8.4.3 Disabled

The device is disabled under the following conditions:

- The enable voltage is less than the enable falling threshold voltage or has not yet exceeded the enable rising threshold.
- The device junction temperature is greater than the thermal shutdown temperature.

Table 1 lists the conditions that lead to the different modes of operation.

Table 1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER			
	V_{IN}	V_{EN}	I_{OUT}	T_J
Normal mode	$V_{IN} > V_{OUT(nom)} + V_{DO}$ and $V_{IN} > V_{IN(min)}$	$V_{EN} > V_{EN(high)}$	$I_{OUT} < I_{LIM}$	$T_J < 125°C$
Dropout mode	$V_{IN(min)} < V_{IN} < V_{OUT(nom)} + V_{DO}$	$V_{EN} > V_{EN(high)}$	—	$T_J < 125°C$
Disabled mode (any true condition disables the device)	—	$V_{EN} < V_{EN(low)}$	—	$T_J > 170°C$

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS7A49 devices belongs to a family of linear regulators that use an innovative bipolar process to achieve ultralow-noise and very high PSRR levels at a wide input voltage range. These features, combined with a high thermal-performance HVSSOP-8 with a PowerPAD package make this device ideal for high-performance analog applications.

9.1.1 Adjustable Operation

The TPS7A4901 device has an output voltage range of $V_{FB(nom)}$ to 33 V. The nominal output voltage of the device is set by two external resistors; see Figure 29.

R_1 and R_2 can be calculated for any output voltage range using the formula shown in Equation 2. To ensure stability under no-load conditions, this resistive network must provide a current greater than or equal to 5 μA.

$$R_1 = R_2\left(\frac{V_{OUT}}{V_{FB(nom)}} - 1\right), \quad \text{where } \frac{V_{FB(nom)}}{R_2} > 5\ \mu A \tag{2}$$

If greater voltage accuracy is required, take into account the output voltage offset contributions resulting from the feedback pin current and use 0.1% tolerance resistors.

9.1.2 Capacitor Recommendations

Use low-equivalent series resistance (ESR) capacitors for the input, output, noise reduction, and bypass capacitors. Ceramic capacitors with X7R and X5R dielectrics are preferred. These dielectrics offer more stable characteristics. Ceramic X7R capacitors offer improved overtemperature performance, whereas ceramic X5R capacitors are more cost-effective and are available in higher values.

High ESR capacitors can degrade PSRR. To ensure stability, maximum ESR must be less than 200 mΩ.

9.1.3 Input and Output Capacitor Requirements

The TPS7A49 family of positive, high-voltage linear regulators achieve stability with a minimum input and output capacitance of 2.2 μF; however, TI highly recommends using a 10-μF capacitor to maximize ac performance. Place the input and output capacitors as close to the pin as possible, on the same side as the device; do not use vias between the capacitor and the pin.

9.1.4 Noise-Reduction and Feed-Forward Capacitor Requirements

Although noise-reduction and feed-forward capacitors ($C_{NR/SS}$ and C_{FF}, respectively) are not needed to achieve stability, TI highly recommends using 10-nF capacitors to minimize noise and maximize ac performance. $C_{NR/SS}$ is a noise-reduction capacitor because it filters out noise from the band gap. For more information on C_{FF}, refer to application report, *Pros and Cons of Using a Feedforward Capacitor with a Low-Dropout Regulator* (SBVA042). This application report explains the advantages of using C_{FF} (also known as C_{BYP}), and the problems that can occur when using this capacitor.

9.1.5 Maximum AC Performance

To maximize noise and PSRR performance, TI recommends including 10 μF or higher input and output capacitors, and 10-nF noise-reduction and bypass capacitors; see Figure 29. The solution illustrated in Figure 29 delivers minimum noise levels of 15.4 μV_{RMS} and power-supply rejection levels above 52 dB from 10 Hz to 400 kHz; see Figure 18 and Figure 25.

Application Information (continued)

9.1.6 Output Noise

The TPS7A49 provides low output noise when a noise reduction capacitor ($C_{NR/SS}$) is used.

The noise-reduction capacitor serves as a filter for the internal reference. By using a 10-nF noise reduction capacitor, the output noise is reduced by approximately 75% (from 69 μV_{RMS} to 17 μV_{RMS}); see Figure 26.

The low output voltage noise of the TPS7A49 makes the device an ideal solution for powering noise-sensitive circuitry.

9.1.7 Post DC-DC Converter Filtering

Most of the time, the voltage rails available in a system do not match the voltage requirements for the system. These rails must be stepped up or down, depending on specific voltage requirements.

DC-DC converters are the preferred solution to step up or down a voltage rail when current consumption is not negligible. These converters offer high efficiency with minimum heat generation, but have one primary disadvantage: these converters introduce a high-frequency component (and the associated harmonics) in addition to the dc output signal.

If not filtered properly, this high-frequency component degrades analog circuitry performance, reducing overall system accuracy and precision.

The TPS7A49 offers a wide-bandwidth, very-high power-supply rejection ratio. This specification makes the device ideal for post dc-dc converter filtering, as shown in Figure 28. TI highly recommends using the maximum performance schematic illustrated in Figure 29. Also, verify that the fundamental frequency (and its first harmonic, if possible) is within the bandwidth of the regulator PSRR; see Figure 18.

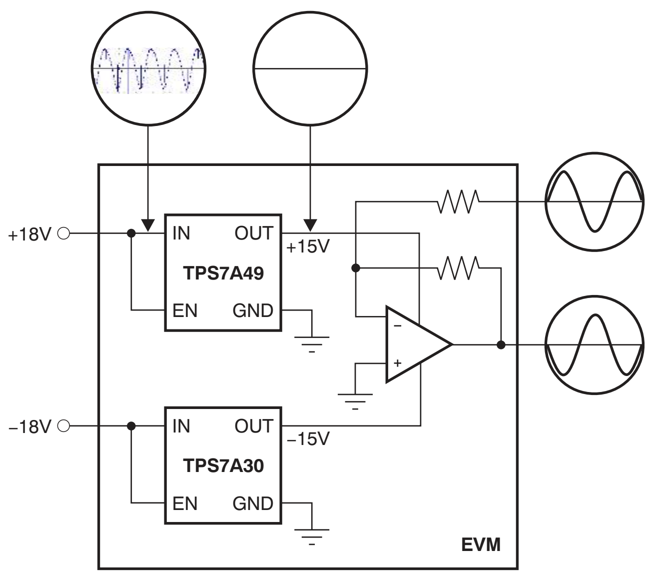


Figure 28. Post DC-DC Converter Regulation to High-Performance Analog Circuitry

9.1.8 Power-Supply Rejection

The 10-nF noise-reduction capacitor greatly improves the TPS7A49 power-supply rejection, achieving up to 15 dB of additional power-supply rejection for frequencies between 110 Hz and 200 kHz.

Additionally, ac performance can be maximized by adding a 10-nF bypass capacitor (C_{FF}) from the FB pin to the OUT pin. This capacitor greatly improves power-supply rejection at lower frequencies for the band from 10 Hz to 200 kHz; see Figure 18.

The very high power-supply rejection of the TPS7A49 makes the device a good choice for powering high-performance analog circuitry, such as operational amplifiers, ADCs, DACS, and audio amplifiers.

Application Information (continued)

9.1.9 Transient Response

As with any regulator, increasing the size of the output capacitor reduces over- and undershoot magnitude, but increases the duration of the transient response.

9.1.10 Audio Applications

Audio applications are extremely sensitive to any distortion and noise in the audio band from 20 Hz to 20 kHz. This stringent requirement demands clean voltage rails to power critical high-performance audio systems.

The very high power-supply rejection ratio (> 55 dB) and low noise at the audio band of the TPS7A49 maximize device performance for audio applications; see Figure 18.

9.1.11 Power for Precision Analog

One of the primary TPS7A49 applications is to provide ultralow-noise voltage rails to high-performance analog circuitry to maximize system accuracy and precision.

The TPS7A49 family of positive high-voltage linear regulators, in conjunction with its negative counterpart (the TPS7A30xx family of negative high-voltage linear regulators), provides ultralow noise, and positive and negative voltage rails for high-performance analog circuitry (such as operational amplifiers, ADCs, DACs, and audio amplifiers).

Because of the ultralow noise levels at high voltages, analog circuitry with high-voltage input supplies can be used. This characteristic allows for high-performance analog solutions to optimize the voltage range and maximize system accuracy.

9.2 Typical Application

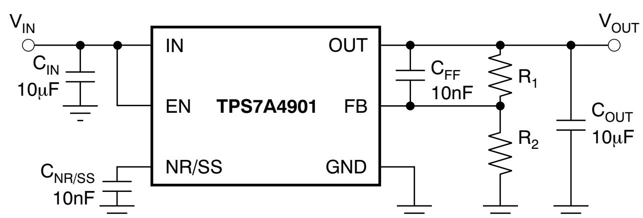


Figure 29. Adjustable Operation for Maximum AC Performance

9.2.1 Design Requirements

The maximum design goals are as follows:

- V_{IN} = 3 V
- V_{OUT} = 1.2 V
- I_{OUT} = 150 mA

The design optimizes transient response and meets a start-up time of 14 ms with a start-up dominated by the soft-start feature. The input supply comes from a supply on the same printed circuit board (PCB). The design circuit is shown in Figure 29.

The design space consists of C_{IN}, C_{OUT}, $C_{NR/SS}$, R_1, and R_2, at $T_{A(max)}$ = 75°C.

9.2.2 Detailed Design Procedure

The first step when designing with a linear regulator is to examine the maximum load current, along with the input and output voltage requirements, to determine if the device thermal and dropout voltage requirements can be met. At 150 mA, the input dropout voltage of the TPS7A49 family is a maximum of 600 mV over temperature; therefore, the dropout headroom of 1.8 V is sufficient for operation over both input and output voltage accuracy. Dropout headroom is calculated as $V_{IN} – V_{OUT} – V_{DO(max)}$, and for optimal performance must be at least 1 V. $V_{DO(max)}$ is the maximum dropout allowed, given worst-case load conditions.

Typical Application (continued)

The maximum power dissipated in the linear regulator is the maximum voltage dropped across the pass element from the input to the output, multiplied by the maximum load current. In this example, the maximum voltage drop across in the pass element is (3 V – 1.2 V), resulting in $V_{IN} – V_{OUT}$ = 1.8 V. The power dissipated in the pass element is calculated by taking this voltage drop multiplied by the maximum load current. For this example, the maximum power dissipated in the linear regulator is 0.2724 W, and is calculated as Equation 3:

$$P_D = (V_{IN} - V_{OUT})\,(I_{MAX}) + (V_{IN})\,(I_Q) \quad (3)$$

When the power dissipated in the linear regulator is known, the corresponding junction temperature rise can be calculated. To calculate the junction temperature rise above ambient, the power dissipated must be multiplied by the junction-to-ambient thermal resistance. This calculation gives the worst-case junction temperature; good thermal design can significantly reduce this number. For thermal resistance information, refer to the *Power Dissipation* section. For this example, using the DGN package, the maximum junction temperature rise is calculated to be 17.3°C. The maximum junction temperature rise is calculated by adding the junction temperature rise to the maximum ambient temperature, which is 75°C for this example. For this example, calculate the maximum junction temperature to be 103.8°C. Keep in mind that the maximum junction temperate must be below 92.3°C for reliable device operation. Additional ground planes, added thermal vias, and air flow all help to lower the maximum junction temperature.

Use the following guidelines to select the values for the remaining components:

To ensure stability under no-load conditions, the current through the resistor network must be greater than 5 µA, as shown in Equation 4:

$$\frac{V_{REF(max)}}{R_2} > 5\mu A \rightarrow R_2 < 242.4\ k\Omega \quad (4)$$

Next, set the value of R_2 to 100 kΩ for a standard 1% value resistor and use Equation 5 to calculate the value of R_1.

$$R_1 = R_2\left(\frac{V_{OUT}}{V_{FB(nom)}} - 1\right) = 100\ k\Omega\left(\frac{1.2\ V}{1.185\ V} - 1\right) = 1.265\ k\Omega \quad (5)$$

For R_1, select a standard, 1%, 68.1-kΩ resistor.

Use Equation 6 to calculate the start-up time, t_{SS}.

$$t_{SS}\ (ms) = 1.4 \times C_{NR/SS} = 14\ ms$$

$$C_{SS} = 10\ nF \quad (6)$$

For the soft-start to dominate the start-up conditions, place the start-up time as a result of the current limit at two decades below the soft-start time (at 140 µs). C_{OUT} must be at least 2.2 µF for stability, as shown in Equation 7 and Equation 8:

$$t_{SS(CL)} = V_{OUT}\left(\frac{C_{OUT}}{I_{CL(max)}}\right) \quad (7)$$

$$C_{OUT(max)} = t_{SS(CL)}\left(\frac{I_{CL(max)}}{V_{OUT}}\right) = 140\ \mu s \times \frac{500\ mA}{2\ V} = 35\ \mu F \quad (8)$$

For C_{IN}, assume that the 3-V supply has some inductance, and is placed several inches away from the PCB. For this case, select a 2.2-µF ceramic input capacitor to ensure that the input impedance is negligible to the LDO control loop and to keep the physical size and cost of the capacitor low; this component is a common-value capacitor.

For better PSRR for this design, use a 10-µF input and output capacitor. To reduce the peaks from transients but slow down the recovery time, increase the output capacitor size or add additional output capacitors.

Typical Application (continued)

9.2.3 Application Curves

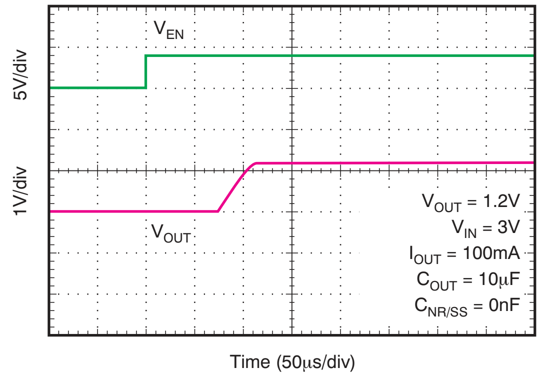


Figure 30. Capacitor-Programmable Soft-Start

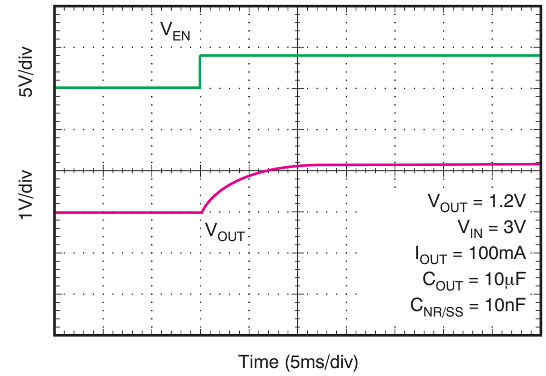


Figure 31. Capacitor-Programmable Soft-Start

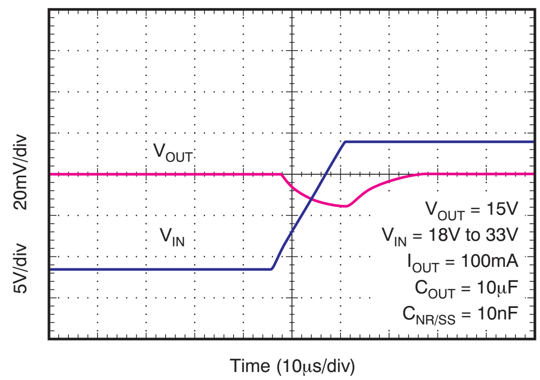


Figure 32. Line Transient Response

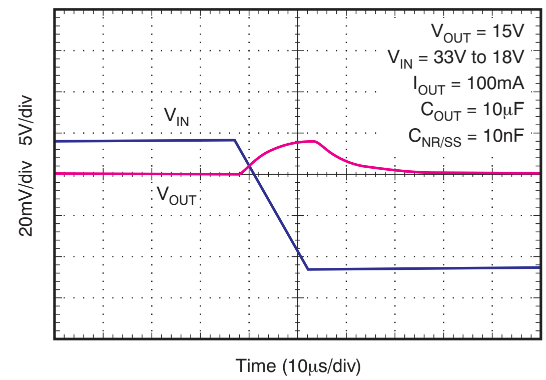


Figure 33. Line Transient Response

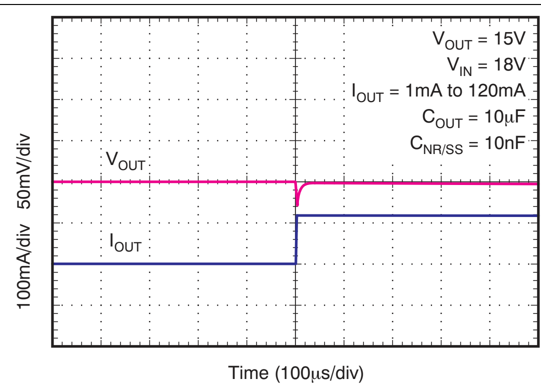


Figure 34. Load Transient Response

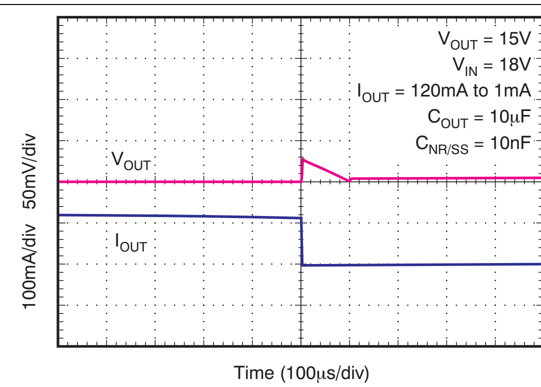


Figure 35. Load Transient Response

9.3 Do's and Don'ts

Place at least one low-ESR, 2.2-µF capacitor as close as possible to both the IN and OUT pins of the regulator to the GND pin.

Provide adequate thermal paths away from the device.

Do not place the input or output capacitor more than 10 mm away from the regulator.

Do not exceed the absolute maximum ratings.

Do not float the enable (EN) pin.

Do not resistively or inductively load the NR/SS pin.

10 Power Supply Recommendations

The input supply for the LDO must be within its recommended operating conditions (that is, between 3 V to 35 V). The input voltage must provide adequate headroom in order for the device to have a regulated output. If the input supply is noisy, additional input capacitors with low ESR can help improve the output noise performance.

The input and output supplies must also be bypassed with at least a 2.2-µF capacitor located near the input and output pins. No other components must be located between these capacitors and the pins.

11 Layout

11.1 Layout Guidelines

Layout is a critical part of good power-supply design. There are several signal paths that conduct fast-changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade the power-supply performance. To help eliminate these problems, bypass the IN pin to ground with a low-ESR ceramic bypass capacitor with an X5R or X7R dielectric.

The GND pin must be tied directly to the PowerPAD under the device. Connect the PowerPAD to any internal PCB ground planes using multiple vias directly under the device.

Equivalent series inductance (ESL) and equivalent series resistance (ESR) must be minimized to maximize performance and ensure stability. Every capacitor (C_{IN}, C_{OUT}, $C_{NR/SS}$, and C_{FF}) must be placed as close as possible to the device and on the same side of the PCB as the regulator itself.

Do not place any of the capacitors on the opposite side of the PCB from where the regulator is installed. The use of vias and long traces is strongly discouraged because these circuits can negatively affect system performance, and can even cause instability.

11.1.1 Board Layout Recommendations to Improve PSRR and Noise Performance

To improve ac performance (such as PSRR, output noise, and transient response), TI recommends that the board be designed with separate ground planes for V_{IN} and V_{OUT}, with each ground plane star-connected only at the GND pin of the device. In addition, the ground connection for the bypass capacitor must connect directly to the GND pin of the device.

11.1.2 Power Dissipation

The ability to remove heat from the die is different for each package type, presenting different considerations in the PCB layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. Performance data for JEDEC low- and high-K boards are given in *Thermal Information*. Using heavier copper increases the effectiveness in removing heat from the device. The addition of plated through-holes to heat-dissipating layers also improves the heatsink effectiveness.

Power dissipation depends on input voltage and load conditions. Power dissipation (P_D) can be approximated by the product of the output current times the voltage drop across the output pass element (V_{IN} to V_{OUT}), as shown in Equation 9:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (9)$$

Layout Guidelines (continued)

Figure 36 shows the maximum ambient temperature versus the power dissipation of the TPS7A49. Figure 36 assumes the device is soldered on a JEDEC standard, high-K layout with no airflow over the board. Actual board thermal impedances vary widely. If the application requires high power dissipation, having a thorough understanding of the board temperature and thermal impedances is helpful to ensure the TPS7A49 does not operate above a junction temperature of 125°C.

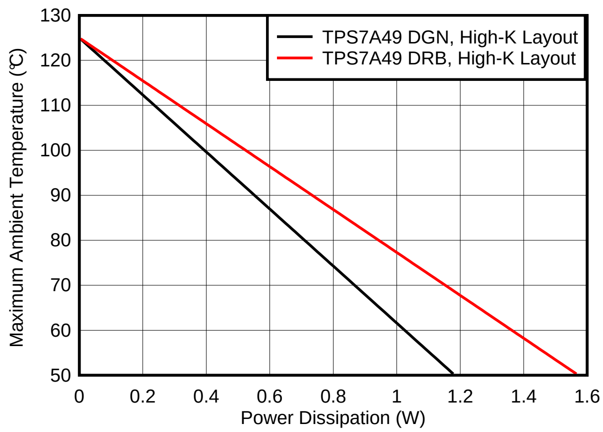


Figure 36. Maximum Ambient Temperature vs Device Power Dissipation

Estimating the junction temperature can be done by using the thermal metrics Ψ_{JT} and Ψ_{JB}; see the *Thermal Information* table. These metrics are a more accurate representation of the heat transfer characteristics of the die and the package than $R_{\theta JA}$. The junction temperature can be estimated with Equation 10.

$$\Psi_{JT}: \quad T_J = T_T + \Psi_{JT} \bullet P_D$$

$$\Psi_{JB}: \quad T_J = T_B + \Psi_{JB} \bullet P_D$$

where

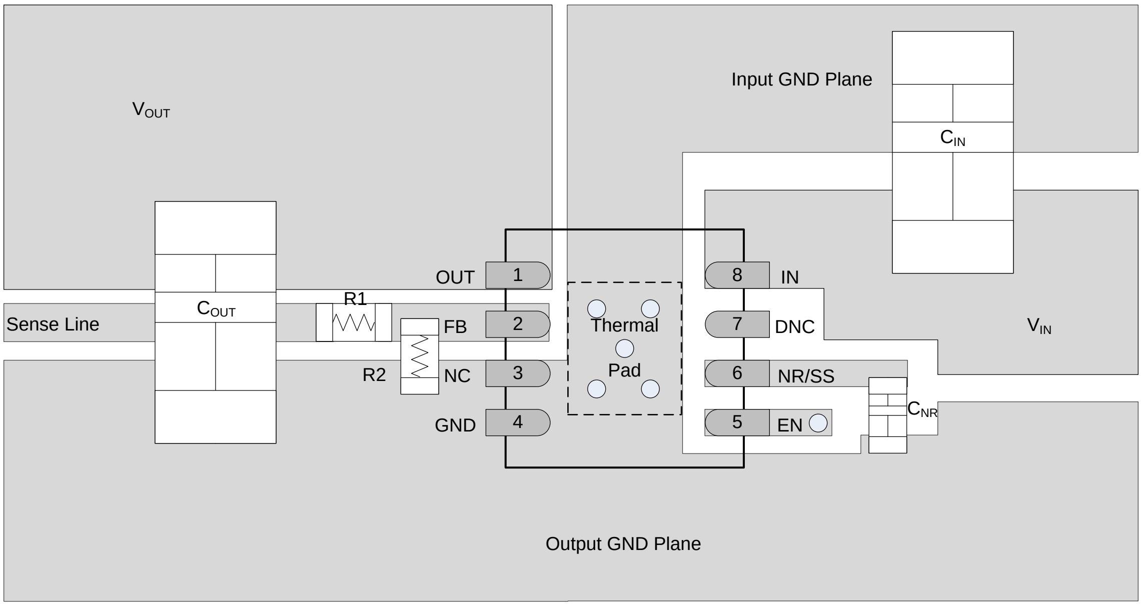
- P_D is the power dissipation given by Equation 9,
- T_T is the temperature at the center-top of the device package, and
- T_B is the PCB temperature measured 1 mm away from the device package on the PCB surface. (10)

NOTE

Both T_T and T_B can be measured on actual application boards using a thermo-gun (an infrared thermometer).

For more information about measuring T_T and T_B, see the application note *Using New Thermal Metrics* (SBVA025), available for download at www.ti.com.

11.2 Layout Example



NOTE: C_{IN} and C_{OUT} are size 1206 capacitors and C_{NR}, R1, and R2 are size 0402.

Figure 37. PCB Layout Example

11.3 Package Mounting

Solder pad footprint recommendations for the TPS7A49 are available at the end of this product data sheet and at www.ti.com.

12 Device and Documentation Support

12.1 Device Support

12.1.1 Development Support

12.1.1.1 Evaluation Modules

An evaluation module (EVM) is available to assist in the initial circuit performance evaluation using the TPS7A49. The TPS7A30-49EVM-567 evaluation module (and related user's guide) can be requested at the Texas Instruments website through the product folder or purchased directly from the TI eStore.

12.1.1.2 Spice Models

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. A SPICE model for the TPS7A49 is available through the product folder under *Tools & Software*.

12.1.2 Device Nomenclature

Table 2. Device Nomenclature(1)

PRODUCT	V_{OUT}
TPS7A49**xxyyyz**	**xx** is the nominal output voltage. An **01** denotes an adjustable voltage version. **yyy** is the package designator. **z** is the package quantity. R is for reel (3000 pieces), T is for tape (250 pieces).

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder on www.ti.com.

12.2 Documentation Support

12.2.1 Related Documentation

- *Pros and Cons of Using a Feedforward Capacitor with a Low-Dropout Regulator*, SBVA042
- *Using New Thermal Metrics*, SBVA025
- *TPS7A30-49EVM-567 User's Guide*, SLVU405

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS7A4901DGNR	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	PTJQ	Samples
TPS7A4901DGNT	ACTIVE	HVSSOP	DGN	8	250	RoHS & Green	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	PTJQ	Samples
TPS7A4901DRBR	ACTIVE	SON	DRB	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PTJQ	Samples
TPS7A4901DRBT	ACTIVE	SON	DRB	8	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PTJQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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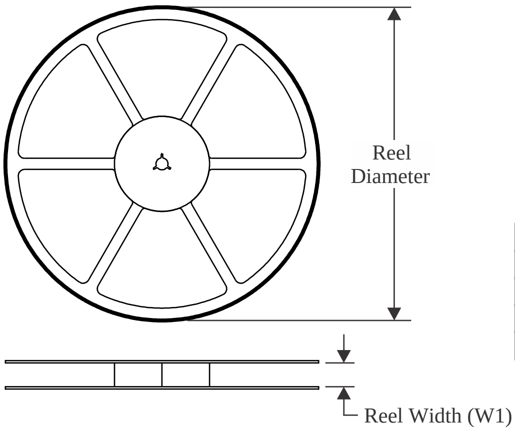
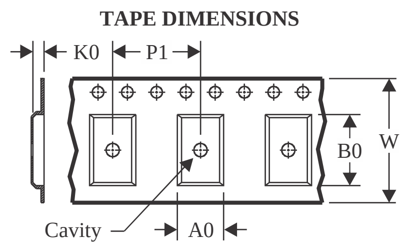
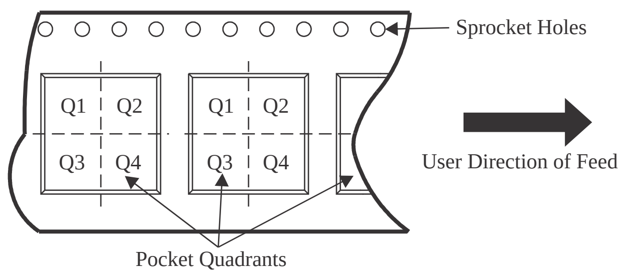
TAPE AND REEL INFORMATION





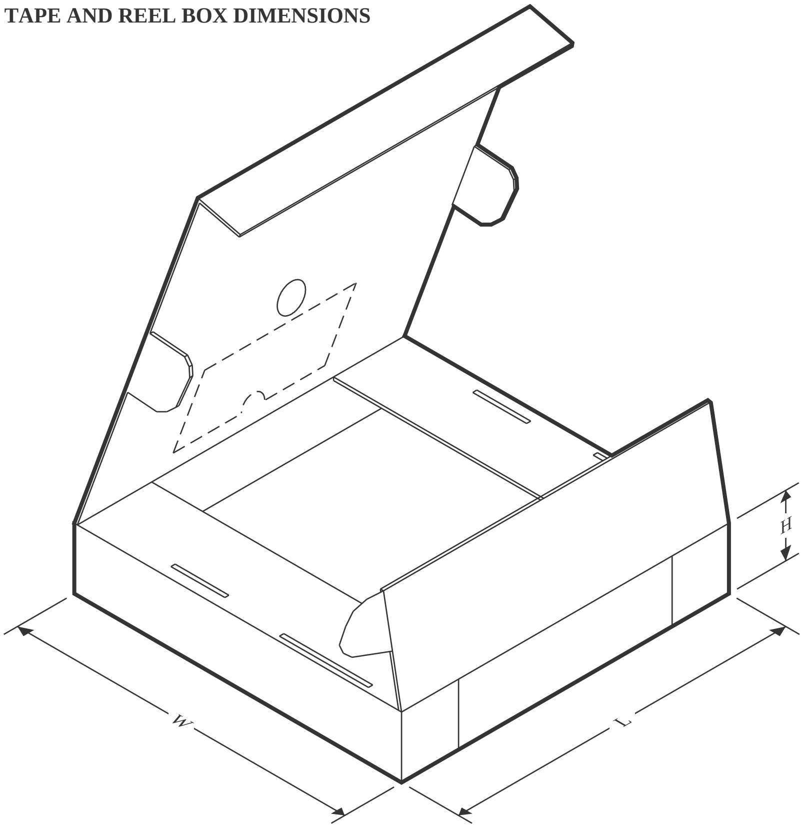
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7A4901DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS7A4901DRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

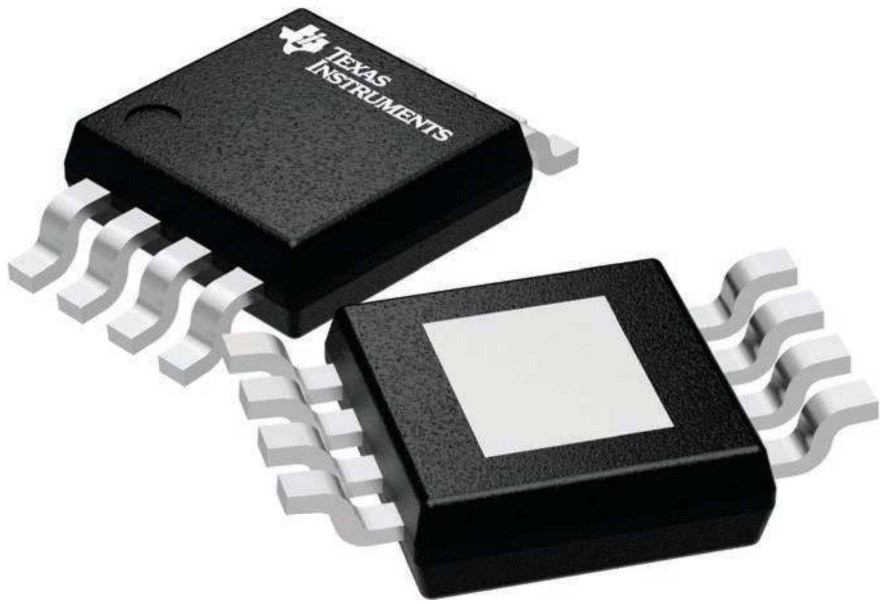
TAPE AND REEL BOX DIMENSIONS



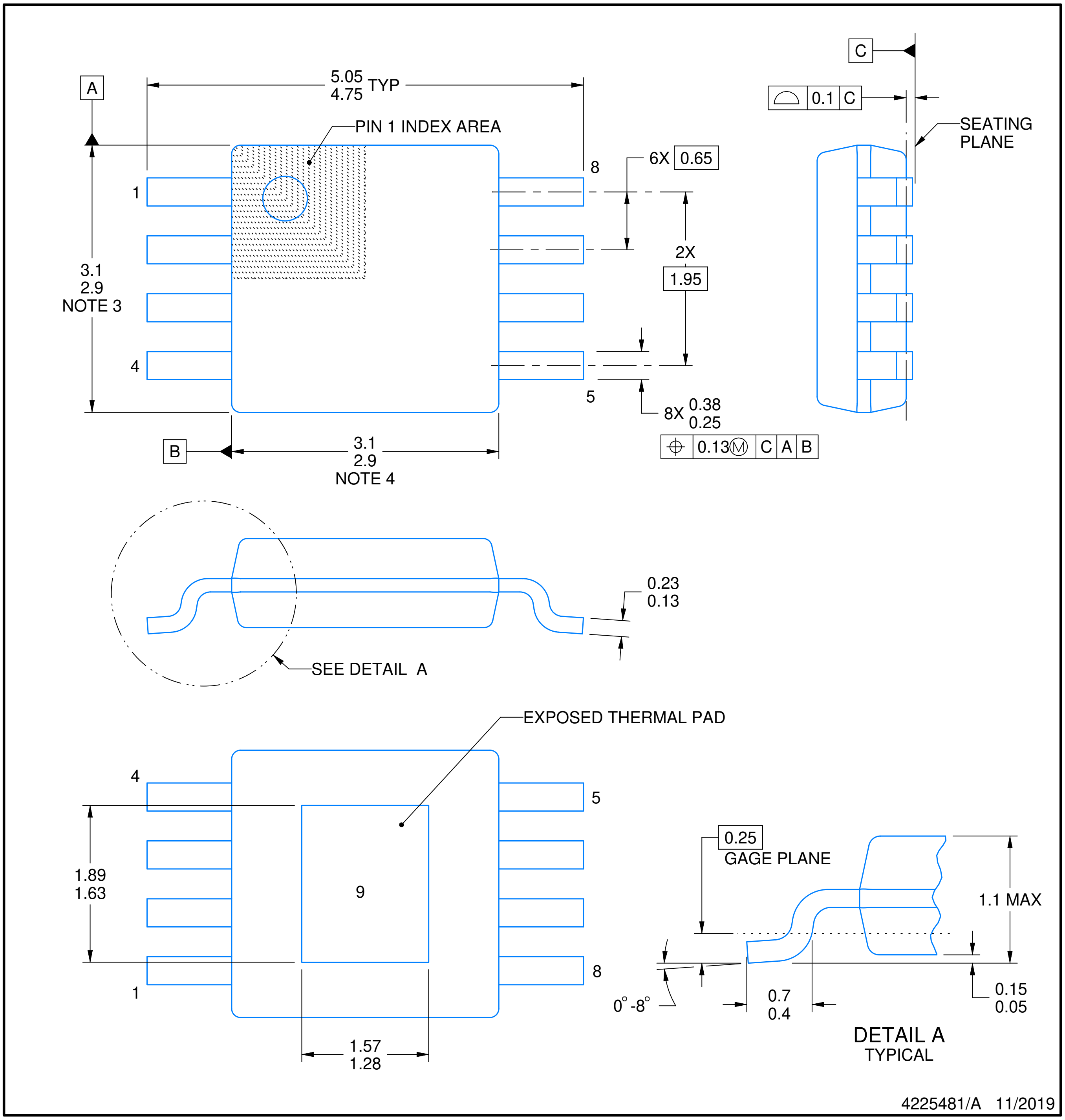
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7A4901DRBR	SON	DRB	8	3000	335.0	335.0	25.0
TPS7A4901DRBT	SON	DRB	8	250	182.0	182.0	20.0

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225482/A

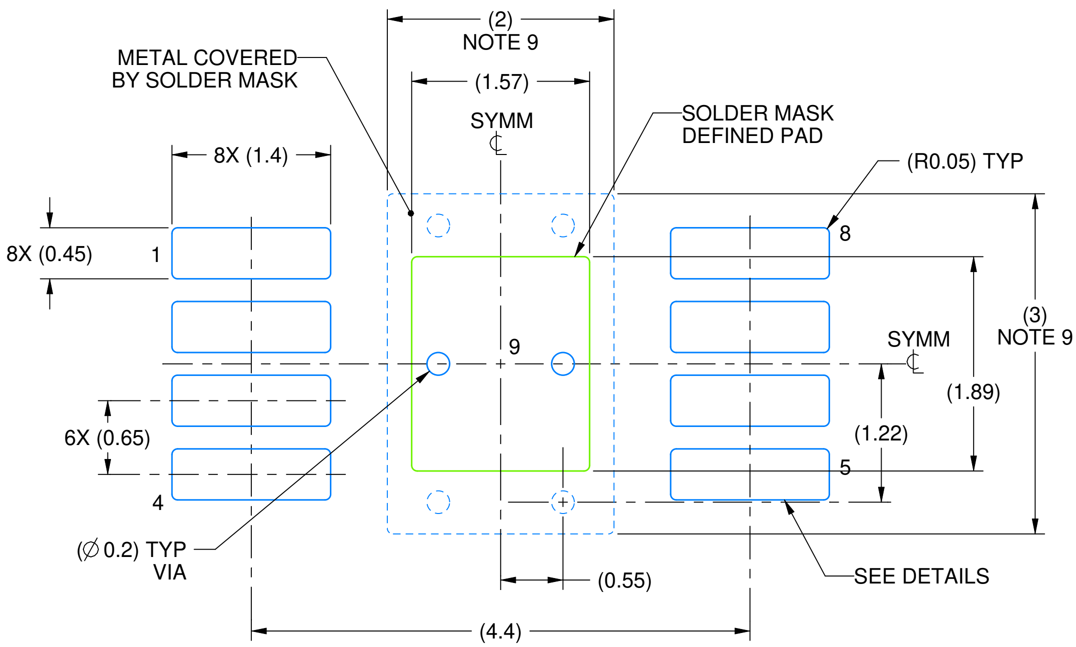


4225481/A 11/2019

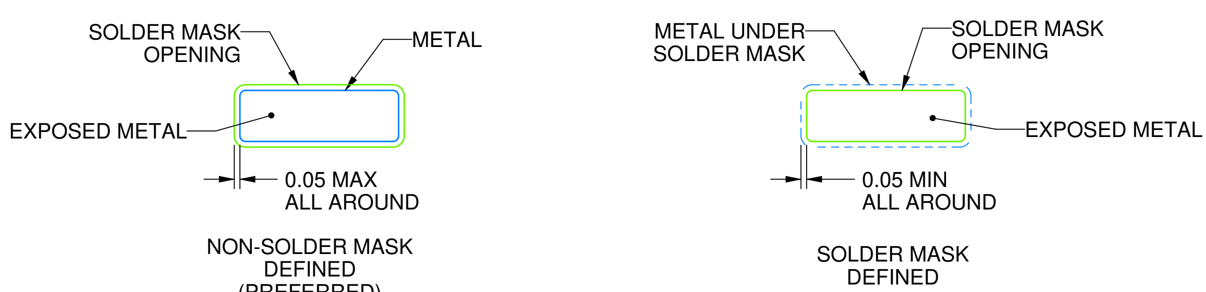
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

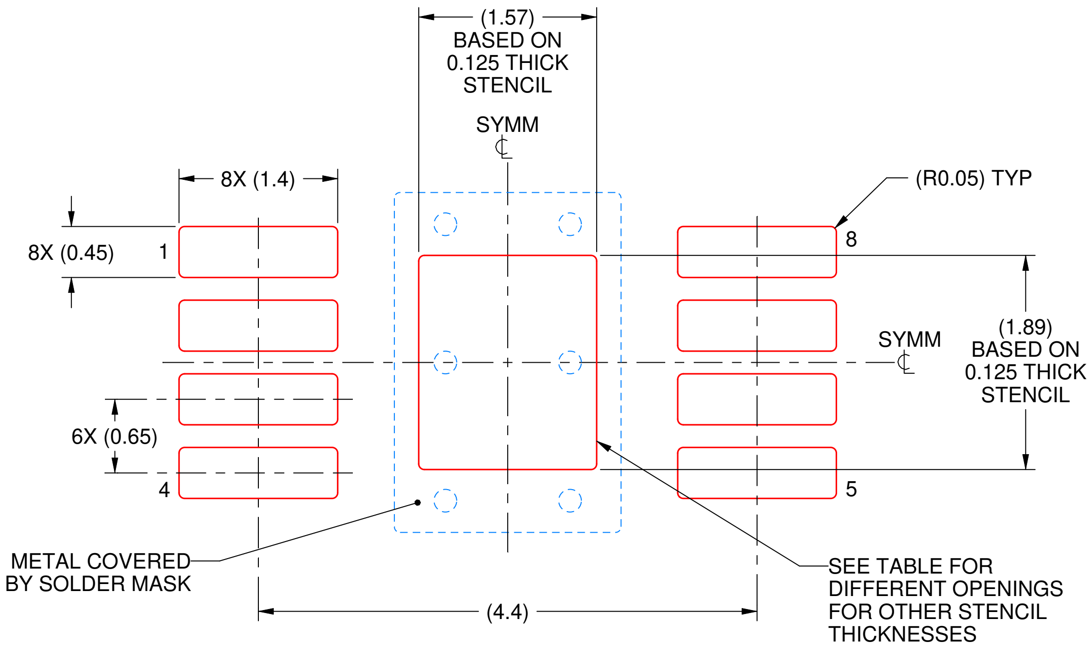


SOLDER MASK DETAILS

4225481/A 11/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



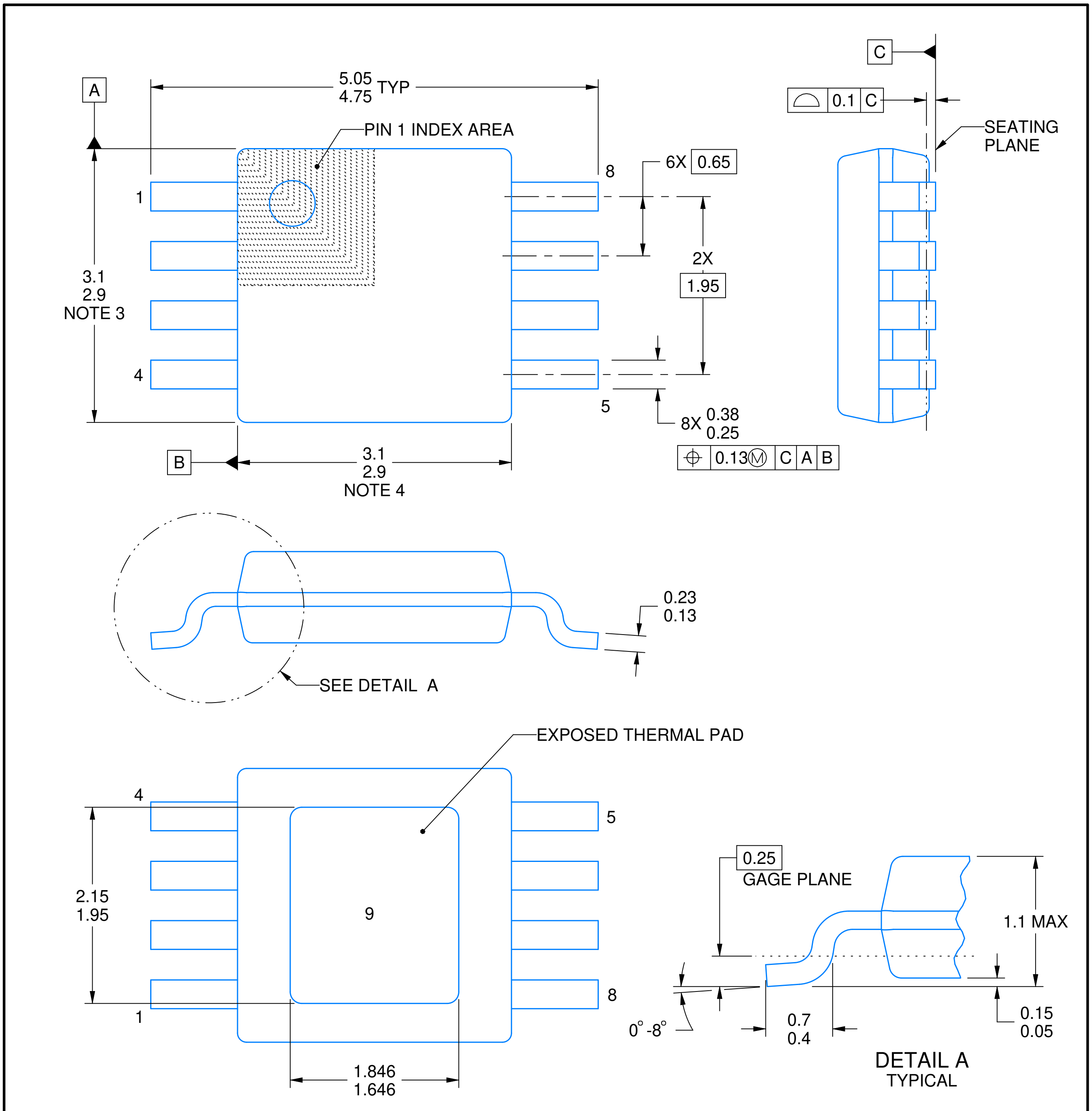
SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.76 X 2.11
0.125	1.57 X 1.89 (SHOWN)
0.15	1.43 X 1.73
0.175	1.33 X 1.60

4225481/A 11/2019

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

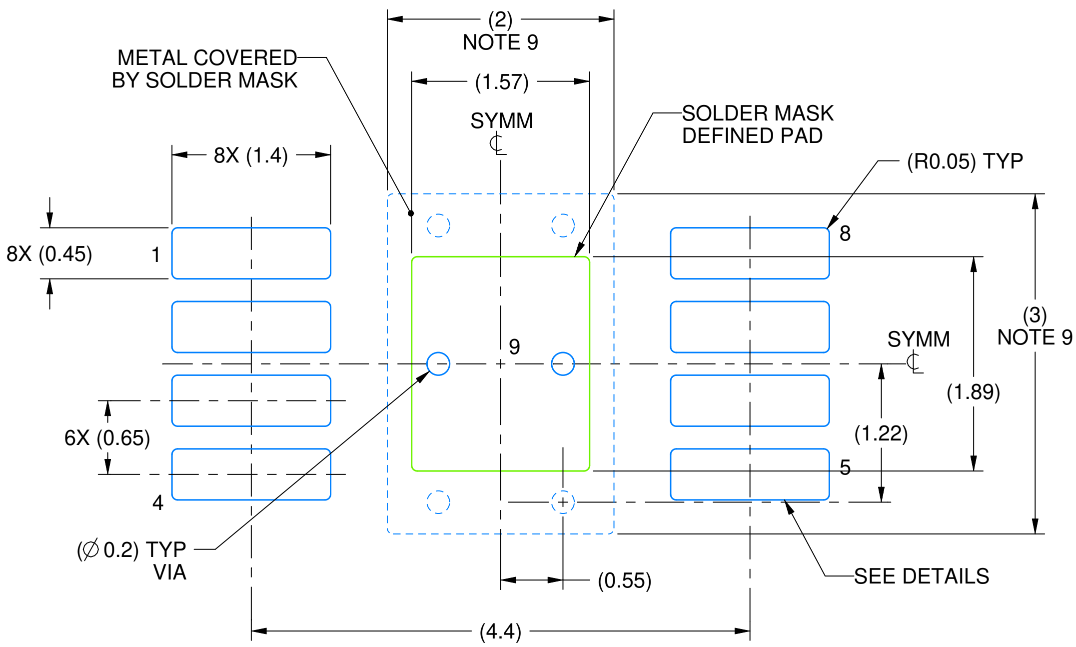


4225480/B 12/2022

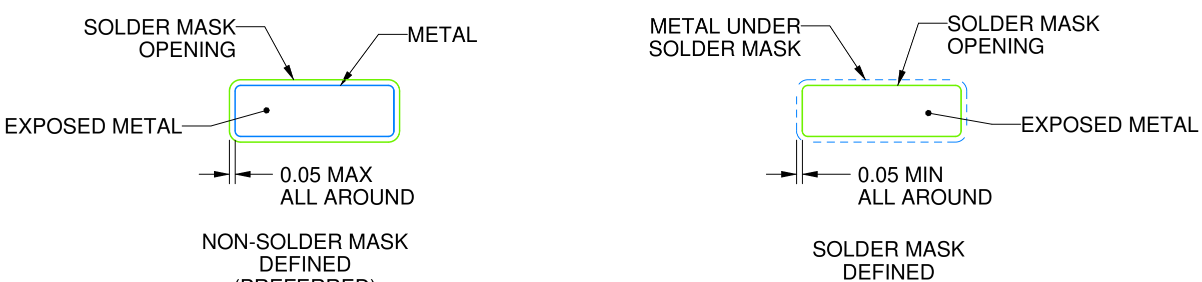
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

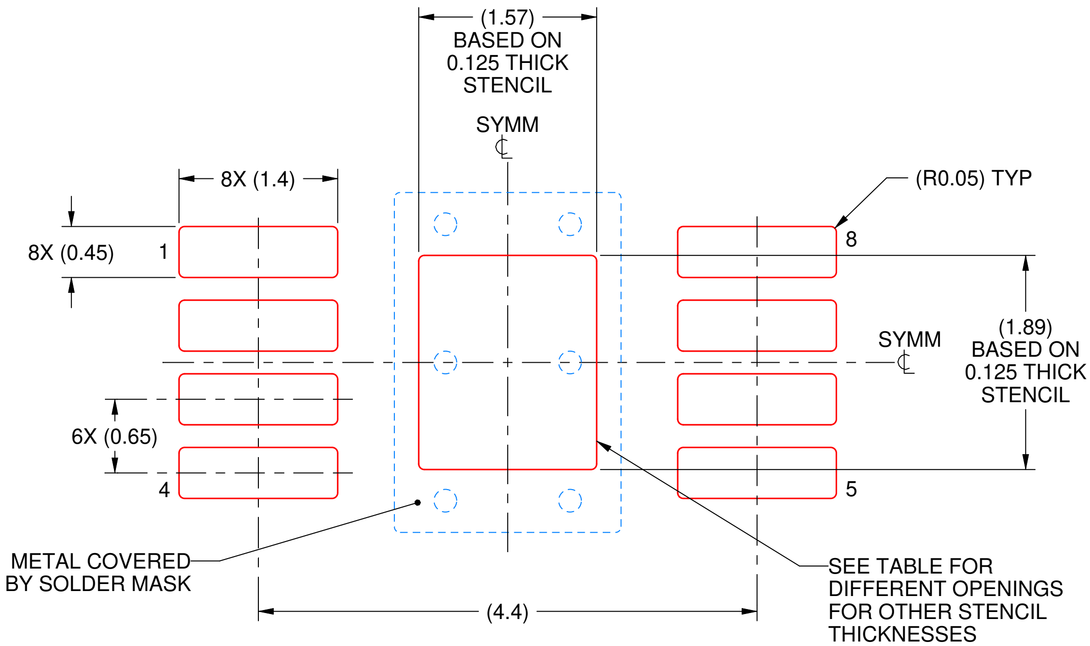


SOLDER MASK DETAILS

4225480/B 12/2022

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.76 X 2.11
0.125	1.57 X 1.89 (SHOWN)
0.15	1.43 X 1.73
0.175	1.33 X 1.60

4225480/B 12/2022

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

DRB 8 — VSON - 1 mm max height

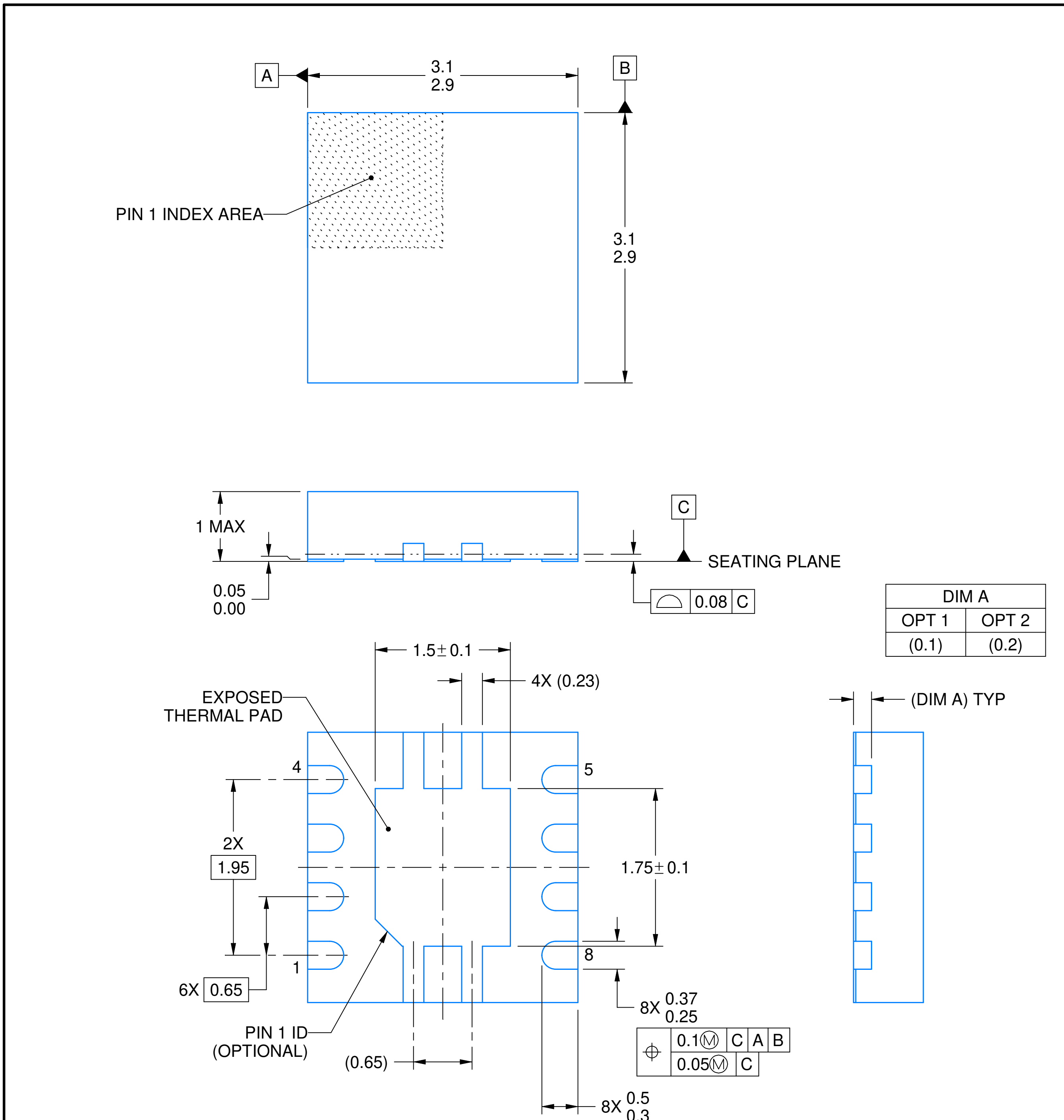
PLASTIC SMALL OUTLINE - NO LEAD

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

VSON - 1 mm max height

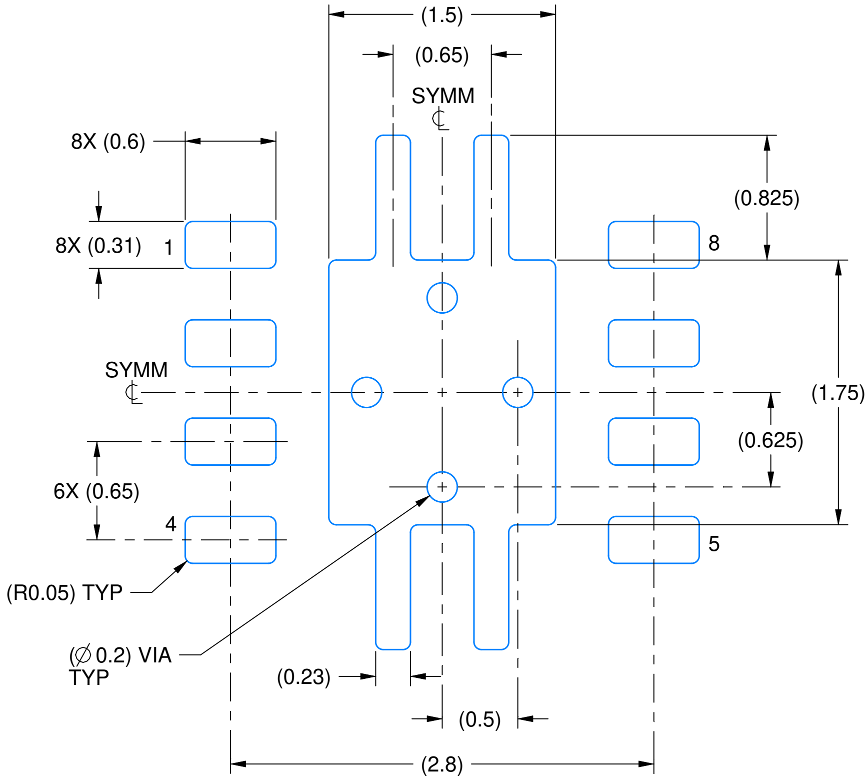
PLASTIC SMALL OUTLINE - NO LEAD



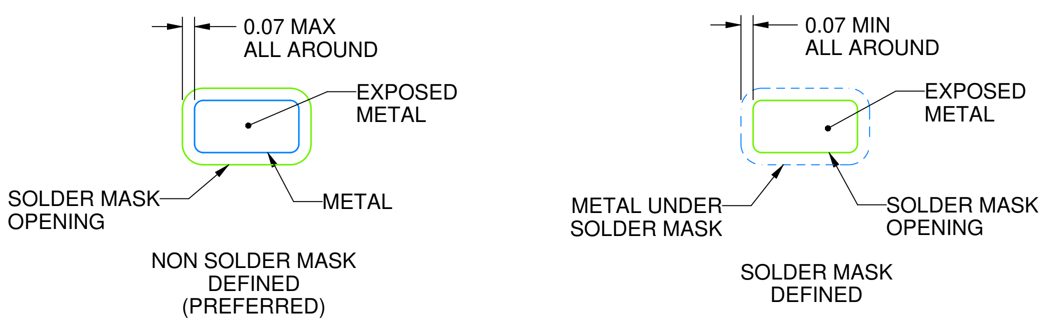
4218875/A 01/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

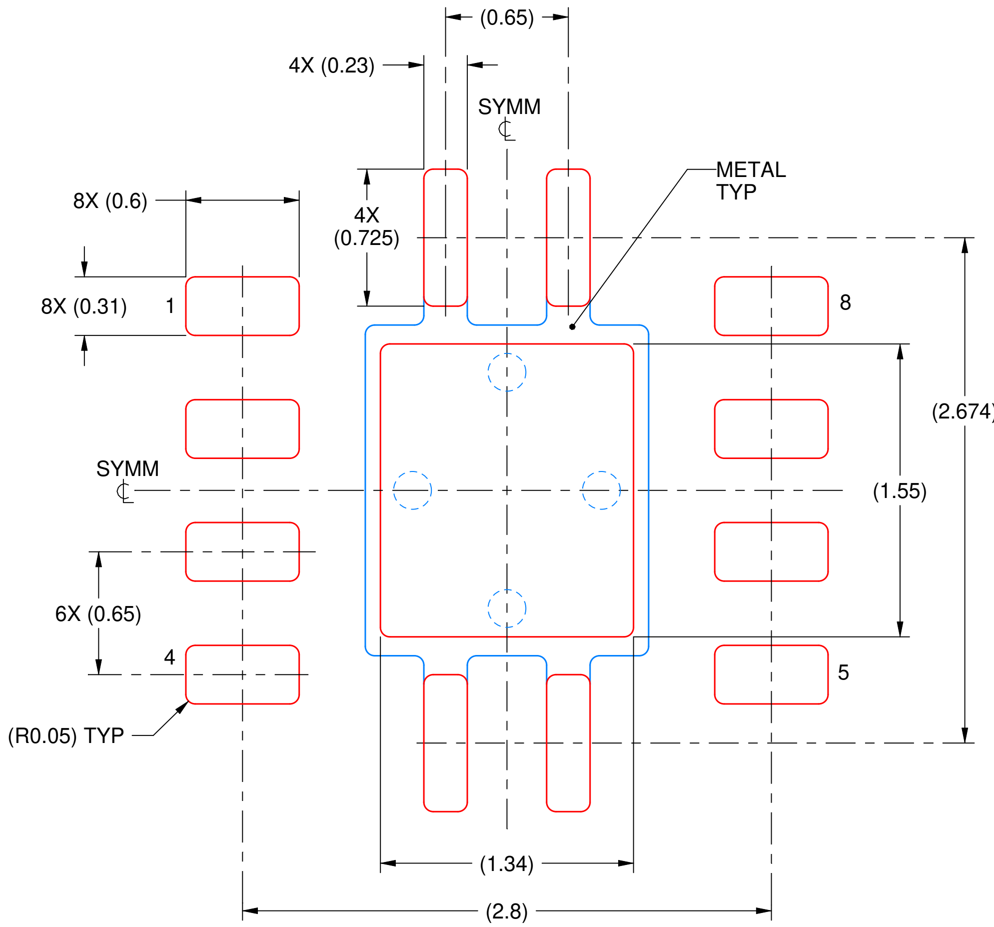


SOLDER MASK DETAILS

4218875/A 01/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
84% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218875/A 01/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.