PTFA180701E
PTFA180701F

green Product

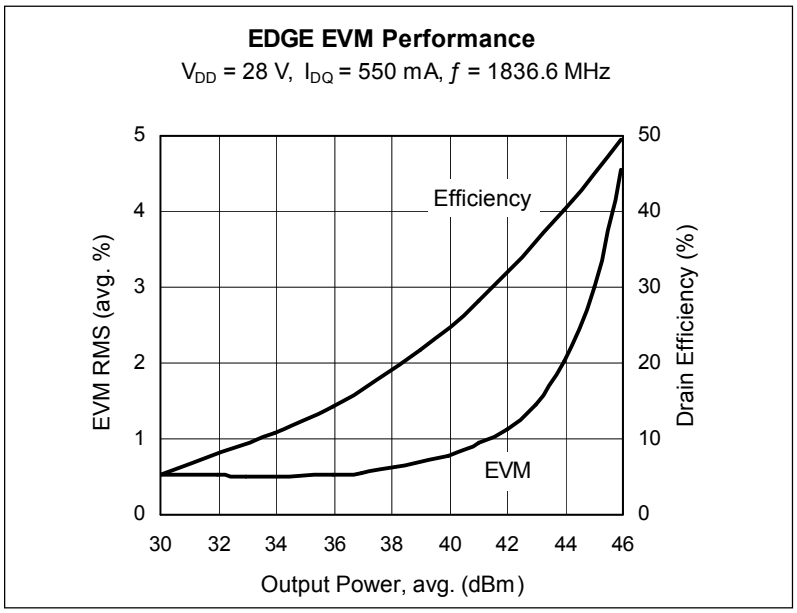
Thermally-Enhanced High Power RF LDMOS FETs
70 W, 1805 – 1880 MHz

Description

The PTFA180701E and PTFA180701F are 70-watt LDMOS FETs designed for GSM and GSM EDGE power amplifier applications in the 1805 MHz to 1880 MHz band. Features include input and output matching, and thermally-enhanced packages with slotted or earless flanges. Manufactured with Infineon's advanced LDMOS process, these devices provide excellent thermal performance and superior reliability.

PTFA180701E
Package H-36265-2

PTFA180701F
Package H-37265-2



Features

- Thermally-enhanced packages, Pb-free and RoHS-compliant
- Broadband internal matching
- Typical EDGE performance
  - Average output power = 44 dBm
  - Gain = 16.5 dB
  - Efficiency = 40.5%
  - EVM = 2.0%
- Typical CW performance
  - Output power at P–1dB = 72 W
  - Gain = 15.5 dB
  - Efficiency = 59%
- Integrated ESD protection: Human Body Model, Class 2 (minimum)
- Excellent thermal stability, low HCI drift
- Capable of handling 10:1 VSWR @ 28 V, 70 W (CW) output power

RF Characteristics

EDGE Measurements (not subject to production test—verified by design/characterization in Infineon test fixture)
V_{DD} = 28 V, I_{DQ} = 550 mA, P_{OUT} = 44 dBm, f = 1836.6 MHz

Characteristic		Symbol	Min	Typ	Max	Unit
Error Vector Magnitude		EVM RMS	—	2.0	—	%
Modulation Spectrum	@ 400 kHz	ACPR	—	–62	—	dBc
	@ 600 kHz	ACPR	—	–76	—	dBc
Gain		G_{ps}	—	16.5	—	dB
Drain Efficiency		η_D	—	40.5	—	%

All published data at T_{CASE} = 25°C unless otherwise indicated

ESD: Electrostatic discharge sensitive device—observe handling precautions!

RF Characteristics (cont.)

Two-tone Measurements (tested in Infineon test fixture)
V_{DD} = 28 V, I_{DQ} = 550 mA, P_{OUT} = 60 W PEP, f = 1840 MHz, tone spacing = 1 MHz

Characteristic	Symbol	Min	Typ	Max	Unit
Gain	G_{ps}	15.5	16.5	—	dB
Drain Efficiency	η_D	44	45	—	%
Intermodulation Distortion	IMD	—	–30	–29	dBc

DC Characteristics

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_{DS} = 10 mA	$V_{(BR)DSS}$	65	—	—	V
Drain Leakage Current	V_{DS} = 28 V, V_{GS} = 0 V	I_{DSS}	—	—	1.0	µA
	V_{DS} = 63 V, V_{GS} = 0 V	I_{DSS}	—	—	10.0	µA
On-State Resistance	V_{GS} = 10 V, V_{DS} = 0.1 V	$R_{DS(on)}$	—	0.125	—	Ω
Operating Gate Voltage	V_{DS} = 28 V, I_D = 550 mA	V_{GS}	2.0	2.5	3.0	V
Gate Leakage Current	V_{GS} = 10 V, V_{DS} = 0 V	I_{GSS}	—	—	1.0	µA

Maximum Ratings

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	65	V
Gate-Source Voltage	V_{GS}	–0.5 to +12	V
Junction Temperature	T_J	200	°C
Total Device Dissipation	P_D	201	W
Above 25°C derate by		1.15	W/°C
Storage Temperature Range	T_{STG}	–40 to +150	°C
Thermal Resistance (T_{CASE} = 70°C, 70 W CW)	$R_{\theta JC}$	0.87	°C/W

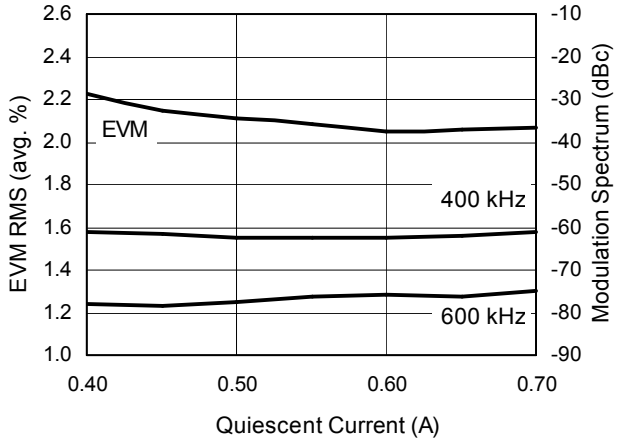
Ordering Information

Type and Version	Package Type	Package Description	Marking
PTFA180701E V4	H-36265-2	Thermally-enhanced slotted flange, single-ended	PTFA180701E
PTFA180701E V4	H-37265-2	Thermally-enhanced earless flange, single-ended	PTFA180701F

Typical Performance (measurements taken in production test fixture)

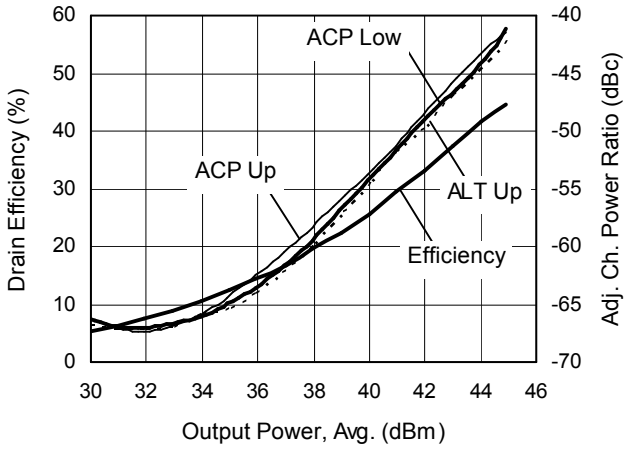
Edge EVM and Modulation Spectrum vs. Quiescent Current

V_{DD} = 28 V, f = 1836.6 MHz, P_{OUT} = 44 dBm



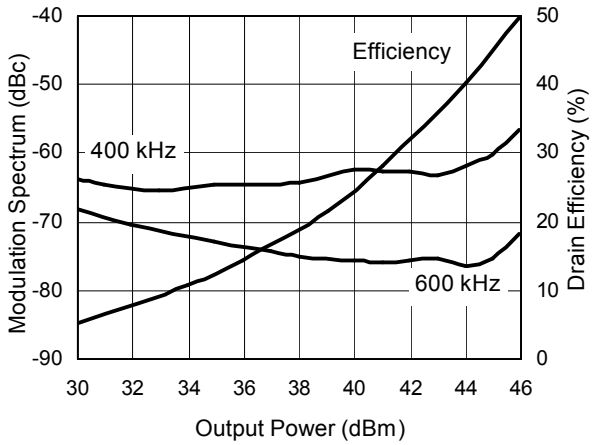
Three-Carrier CDMA2000 Performance

V_{DD} = 28 V, I_{DQ} = 550 mA, f = 1840 MHz



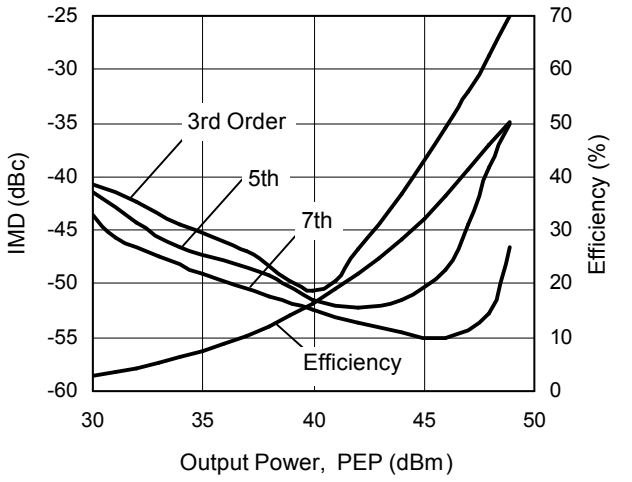
EDGE Modulation Spectrum Performance

V_{DD} = 28 V, I_{DQ} = 550 mA, f = 1836.6 MHz



Intermodulation Distortion vs. Output Power

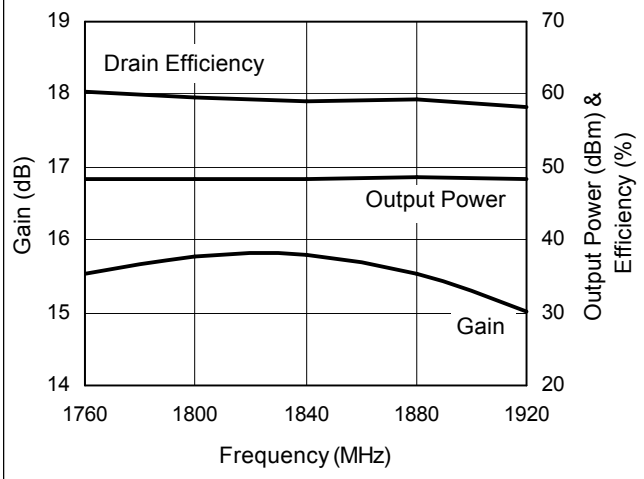
V_{DD} = 28 V, I_{DQ} = 550 mA, f = 1840 MHz, tone spacing = 1 MHz



Typical Performance (cont.)

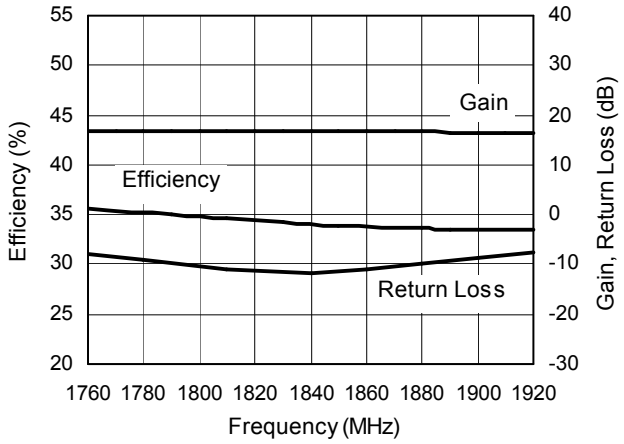
Broadband Test Fixture Performance (P–1dB)

V_{DD} = 28 V, I_{DQ} = 550mA



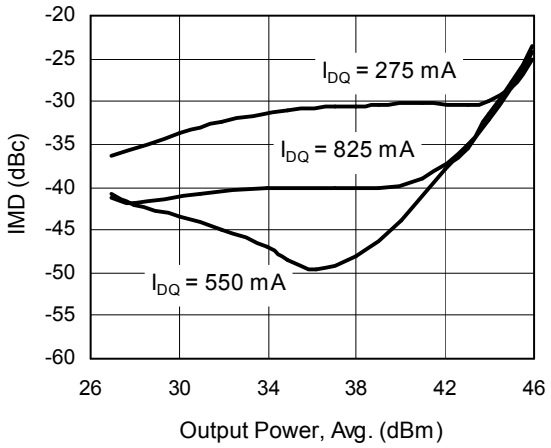
CW Broadband Performance

V_{DD} = 28 V, I_{DQ} = 550 mA, P_{OUT} = 43 dBm



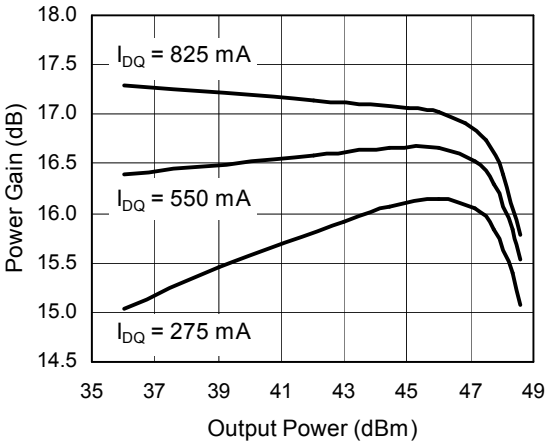
IM3 vs. Output Power at Selected Biases

V_{DD} = 28 V, f_1 = 1849, f_2 = 1840 MHz



Power Sweep

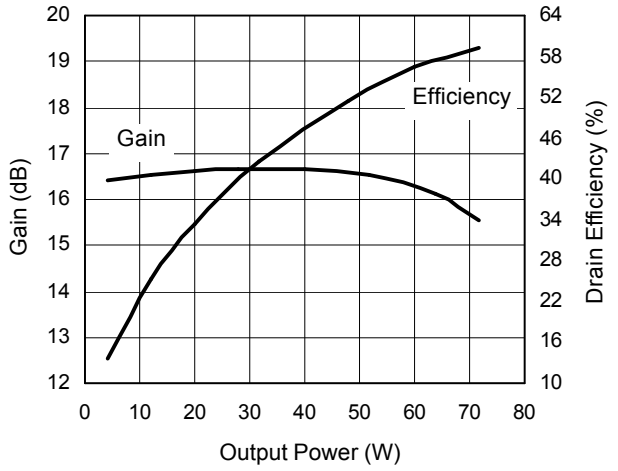
V_{DD} = 28 V, f = 1880 MHz



Typical Performance (cont.)

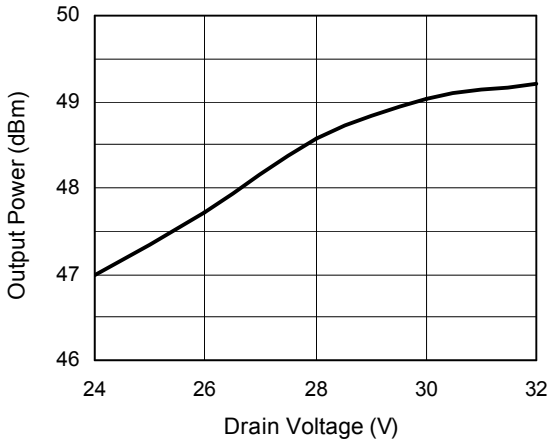
Gain & Efficiency vs. Output Power

V_{DD} = 28 V, I_{DQ} = 550 mA, f = 1880 MHz



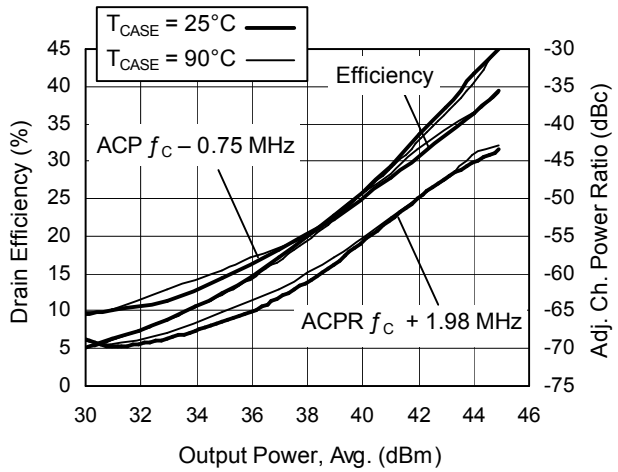
Output Power (P–1dB) **vs. Drain Voltage**

I_{DQ} = 550 mA, f = 1880 MHz



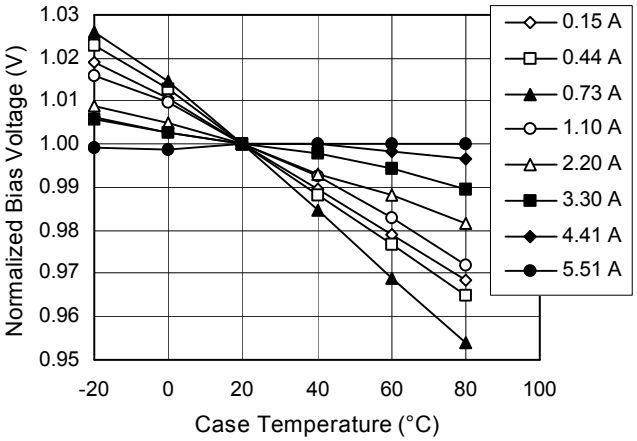
IS-95 CDMA Performance

V_{DD} = 28 V, I_{DQ} = 550 mA, f = 1840 MHz

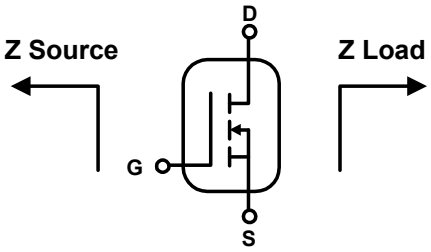


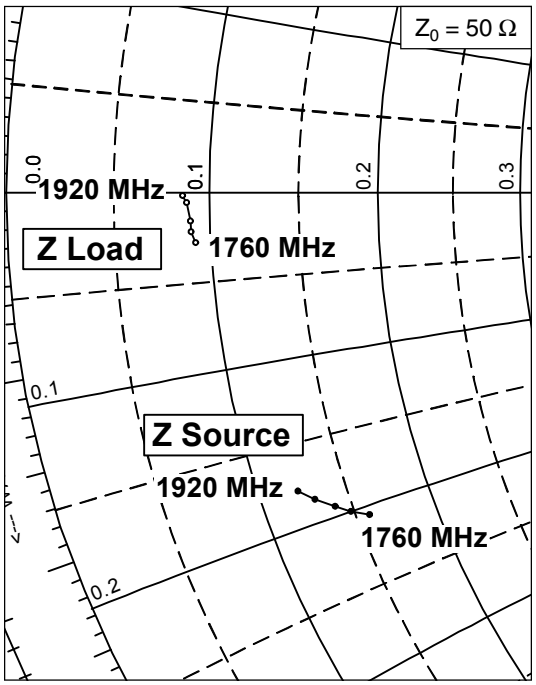
Bias Voltage vs. Temperature

Voltage normalized to typical gate voltage, series show current



Broadband Circuit Impedance

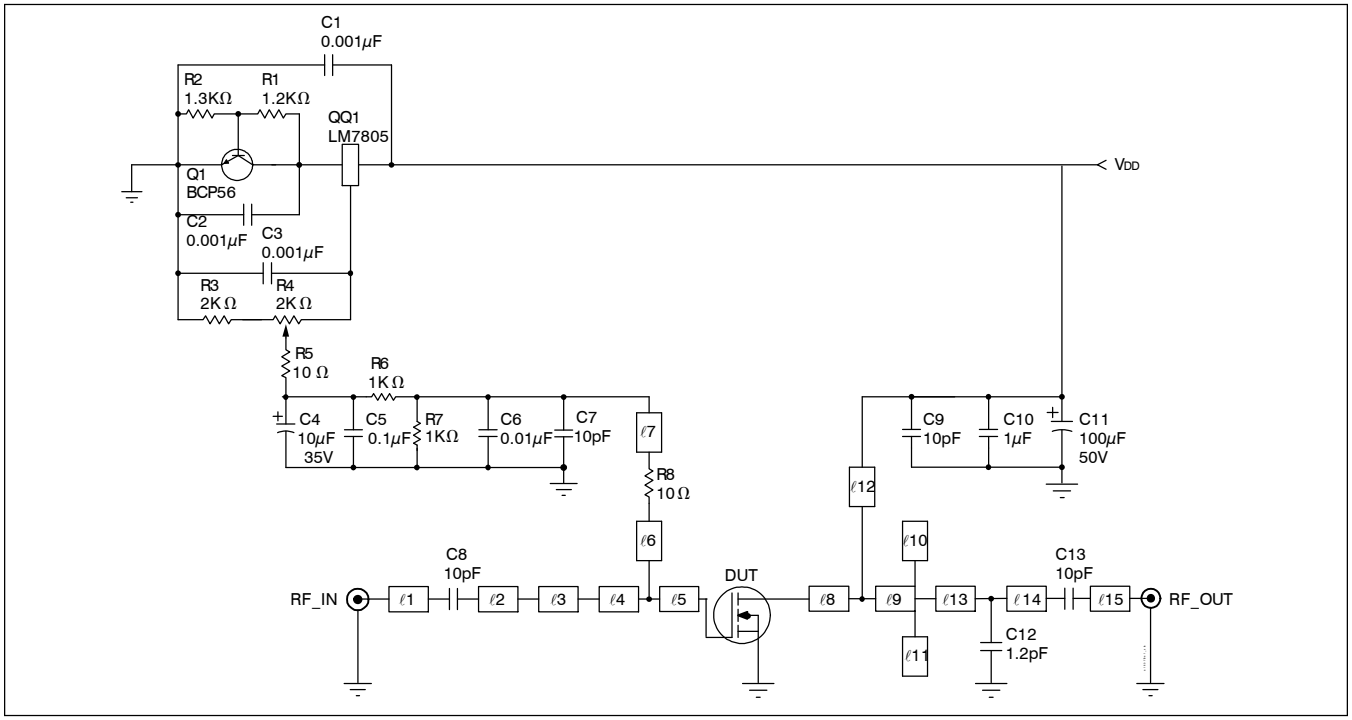




Frequency	Z Source Ω		Z Load Ω	
MHz	R	jX	R	jX
1760	7.9	–10.3	4.6	–1.4
1800	7.4	–10.0	4.5	–1.1
1840	7.0	–9.7	4.5	–0.8
1880	6.5	–9.3	4.4	–0.3
1920	6.1	–8.9	4.3	–0.1

See next page for circuit information

Reference Circuit



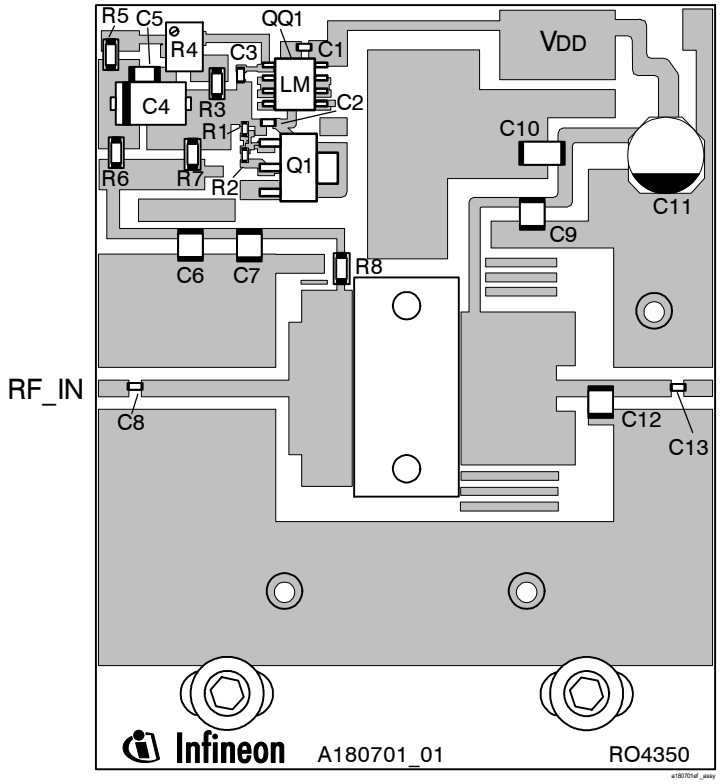
Reference circuit schematic for 1840 MHz

Circuit Assembly Information			
DUT	PTFA180701E or PTFA180701F	LDMOS Transistor	
PCB	0.76 mm [.030"], ε_r = 3.48	Rogers, RO4350	1 oz. copper

Microstrip	Electrical Characteristics at 1840 MHz[1]	Dimensions: L x W (mm)	Dimensions: L x W (in.)
ℓ1	0.034 λ, 50.0	3.33 x 1.70	0.131 x 0.067
ℓ2	0.149 λ, 50.0	14.68 x 1.70	0.578 x 0.067
ℓ3	0.014 λ, 10.2	1.27 x 13.28	0.050 x 0.523
ℓ4	0.044 λ, 7.1	3.86 x 19.61	0.152 x 0.772
ℓ5	0.014 λ, 7.1	1.27 x 19.61	0.050 x 0.772
ℓ6	0.012 λ, 78.0	1.22 x 0.74	0.048 x 0.029
ℓ7	0.115 λ, 65.0	11.51 x 1.07	0.453 x 0.042
ℓ8	0.016 λ, 8.9	1.37 x 15.34	0.054 x 0.604
ℓ9	0.090 λ, 8.9	8.13 x 15.34	0.320 x 0.604
ℓ10, ℓ11	0.020 λ, 21.8	1.91 x 5.36	0.075 x 0.211
ℓ12	0.162 λ, 64.0	16.18 x 1.12	0.637 x 0.044
ℓ13	0.042 λ, 50.0	4.11 x 1.70	0.162 x 0.067
ℓ14	0.074 λ, 50.0	7.29 x 1.70	0.287 x 0.067
ℓ15	0.032 λ, 50.0	3.12 x 1.70	0.123 x 0.067

[1]Electrical characteristics are rounded

Reference Circuit (cont.)



Reference circuit assembly diagram (not to scale)*

Component	Description	Suggested Manufacturer	P/N or Comment
C1, C2, C3	Capacitor, 0.001 µF	Digi-Key	PCC1772CT-ND
C4	Tantalum capacitor, 10 µF, 35 V	Digi-Key	399-1655-2-ND
C5	Capacitor, 0.1 µF	Digi-Key	PCC104BCT-ND
C6	Capacitor, 0.01 µF	ATC	200B 103
C7, C9	Ceramic capacitor, 10 pF	ATC	100B 100
C8, C13	Ceramic capacitor, 10 pF	ATC	100A 100
C10	Ceramic capacitor, 1 µF	Digi-Key	445-1411-1-ND
C11	Electrolytic capacitor, 100 µF, 50 V	Digi-Key	PCE3718CT-ND
C12	Ceramic capacitor, 1.2 pF	ATC	100B 1R2
Q1	Transistor	Infineon Technologies	BCP56
QQ1	Voltage regulator	National Semiconductor	LM7805
R1	Chip resistor 1.2 k-ohms	Digi-Key	P1.2KGCT-ND
R2	Chip resistor 1.3 k-ohms	Digi-Key	P1.3KGCT-ND
R3	Chip resistor 2 k-ohms	Digi-Key	P2KECT-ND
R4	Potentiometer 2 k-ohms	Digi-Key	3224W-202ETR-ND
R5, R8	Chip resistor 10 ohms	Digi-Key	P10ECT-ND
R6, R7	Chip resistor 1 k-ohms	Digi-Key	P1KECT-ND

**Gerber files for this circuit available on request.*

Package Outline Specifications

Package H-36265-2

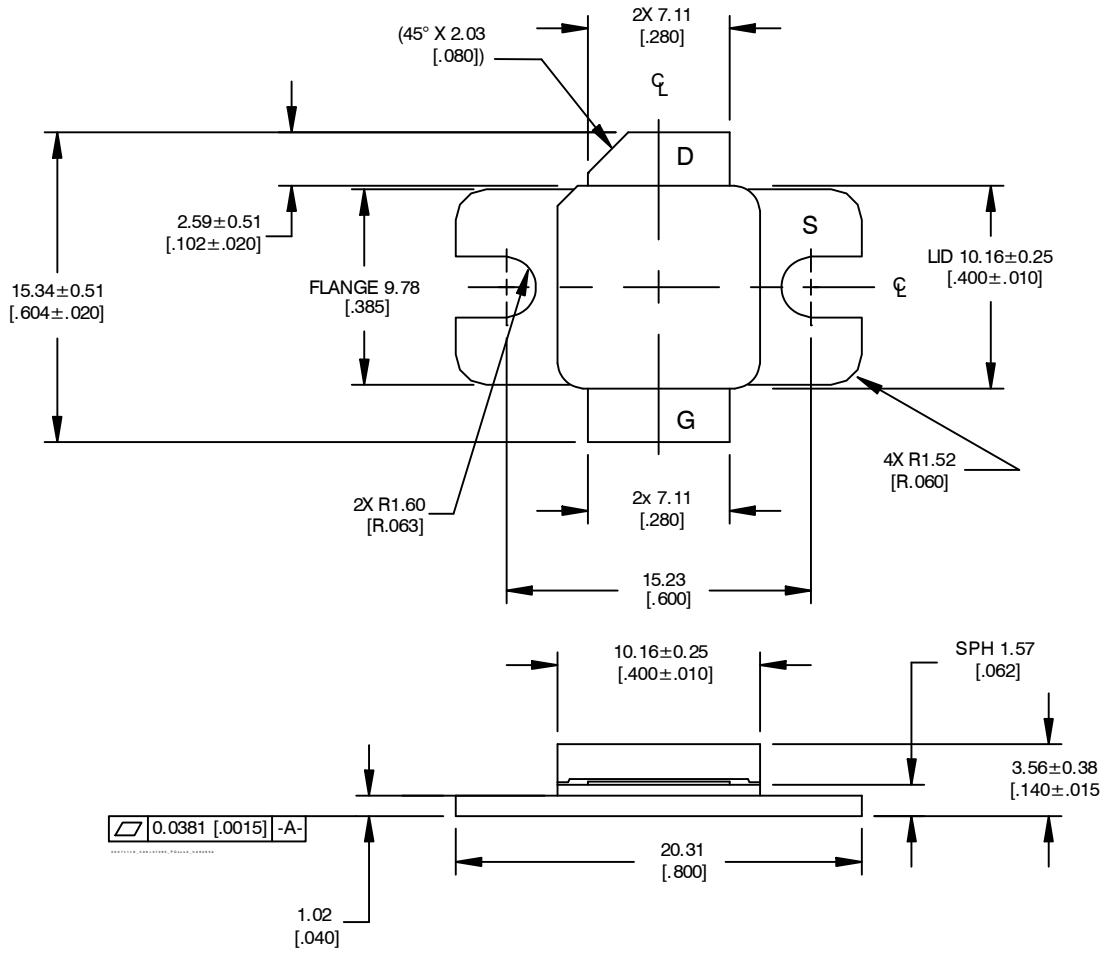


Diagram Notes—unless otherwise specified:

1. Lead thickness: 0.10 +0.051/–0.025 [.004 +.002/–.001].
2. All tolerances ± 0.127 [.005] unless specified otherwise.
3. Pins: D = drain, S = source, G = gate.
4. Interpret dimensions and tolerances per ASME Y14.5M-1994.
5. Primary dimensions are mm. Alternate dimensions are inches.
6. Gold plating thickness:
   S, D, G - flange & leads: 1.14 ± 0.38 micron [45 ± 15 microinch]

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Package Outline Specifications (cont.)

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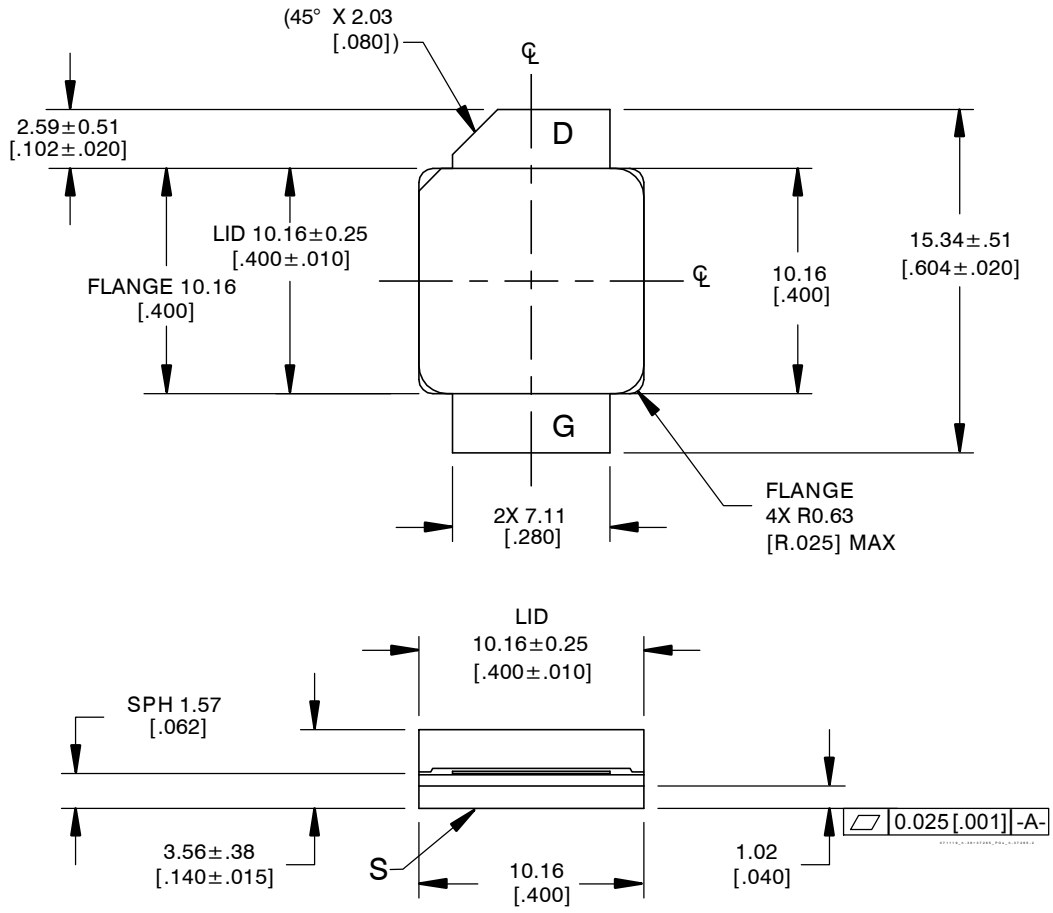

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Revision History:	**2009-02-20**	Data Sheet
Previous Version:	2006-08-10, Data Sheet	
Page	Subjects (major changes since last revision)	
1, 3, 9, 10	Update to product V4, with new package technologies. Update package outline diagrams.	
8	Fixed typing error	

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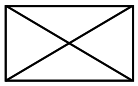

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