12 W three-phase power supply for smart meters and home appliances

About this document

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Scope and purpose

This document is an engineering report describing a three-phase-input 12 V 12 W Flyback converter power supply using the ICE5QSAG QR Flyback controller and the new 950 V CoolMOS™ P7 SJ MOSFET IPD95R1K2P7, which are the latest generation of devices from Infineon. The converter is operated in Discontinuous Conduction Mode (DCM) with variable frequency, has a low standby power, and has various protection modes built in for a highly reliable system. This demo board is designed to evaluate the performance of the IPD95R1K2P7 for ease of use in applications such as smart meter power supplies. This board could also be used as an auxiliary power supply for home appliances such as air-conditioning units or induction cookers.

Intended audience

Power supply designers for smart meters and home appliances.

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1 Overview and key results

Smart metering technologies are evolving quickly as energy suppliers and users demand more advanced communication interfaces and usage data, and more flexibility with electric power utilization. Low power consumption of the meter is a key operating criterion. Smart meters in the field are consuming energy, which is a cost that must be paid by the end user. Smart meters need to operate in harsh environmental conditions as they are installed indoors and outdoors and operate with wide input voltage ranges. They also need to be immune to strong magnetic fields and still maintain continuous and accurate metering. All these requirements are driving the demand for more innovative power supply designs for powering smart meters. This application note examines some of the typical power supply designs used in smart meters and provides an optimal solution for the challenges currently faced by power supply design engineers. The power supply design shown in the subsequent sections can also be used as an auxiliary power supply in home appliances such as induction cookers and air-conditioners. As in smart meters, in these home appliances it is essential to withstand high input voltages to protect against a single-phase unit being accidentally connected to two phases rather than phase to neutral.

Power supply efficiency is now an important aspect in any application that requires AC-DC power conversion. For this reason both energy suppliers and regulators demand lower power consumption. The average power consumption requirement could be as low as 1 W for a single-phase meter, so the efficiency of the power supply itself plays a critical role in delivering this. It is a tough requirement, because smart meter power supplies also often need to deliver a 10 to 12 W peak power demand. Several approaches are being used to increase low power efficiency, for example reducing the quiescent current of the switching controller, or techniques such as cycle-by-cycle current limiting, adaptive switching frequency control and frequency hopping.

Different power supply topologies used in smart meter power supplies and their trade-offs are shown in the table that follows:

Topologies / features	**Capacitive dropper**	**Buck converter**	**Flyback converter with integrated MOSFET**	**Flyback converter with external MOSFET**
Component count	Six to eight per phase	15 to 20 single-phase or three-phase	15 to 20 single-phase or three-phase	More than 20 single-phase or three-phase Modular
Efficiency	50 percent	60 percent	70 percent	80 percent
Design flexibility – increasing output current capability	Low	High	High	Highest
EMI	Low	High – needs more filtering efforts due to high-side switch at the input	High – needs more filtering efforts due to integrated MOSFET switch	Medium – easy with right component selection and accessible gate control via ext. R_g
Cost	Low	High – due to increased EMI filter size, high-side gate driver	High – due to integration feature set, limited internal $R_{DS(on)}$ options	Medium – due to smaller EMI filter size, low-side PWM controller, wide options in $R_{DS(on)}$

Overview and key results

Topologies / features	Capacitive dropper	Buck converter	Flyback converter with integrated MOSFET	Flyback converter with external MOSFET
Package options	Not applicable	Many DIP, DSO DPAK/SOT-223	Limited DIP, DSO	Many DIP, DSO DPAK/SOT-223

As shown in the table above, Flyback converters with an external MOSFET look to be the most efficient, cost-effective, EMI-friendly and modular design approach to use in smart meter power supplies.

Therefore such a converter was designed to operate with three-phase AC input voltage up to 465 V AC and provide a stable output of 12 V with 1 A load current capability.

Key performance features of the design (see the short summary at the end) are visualized in Figures 1 to 4, below:

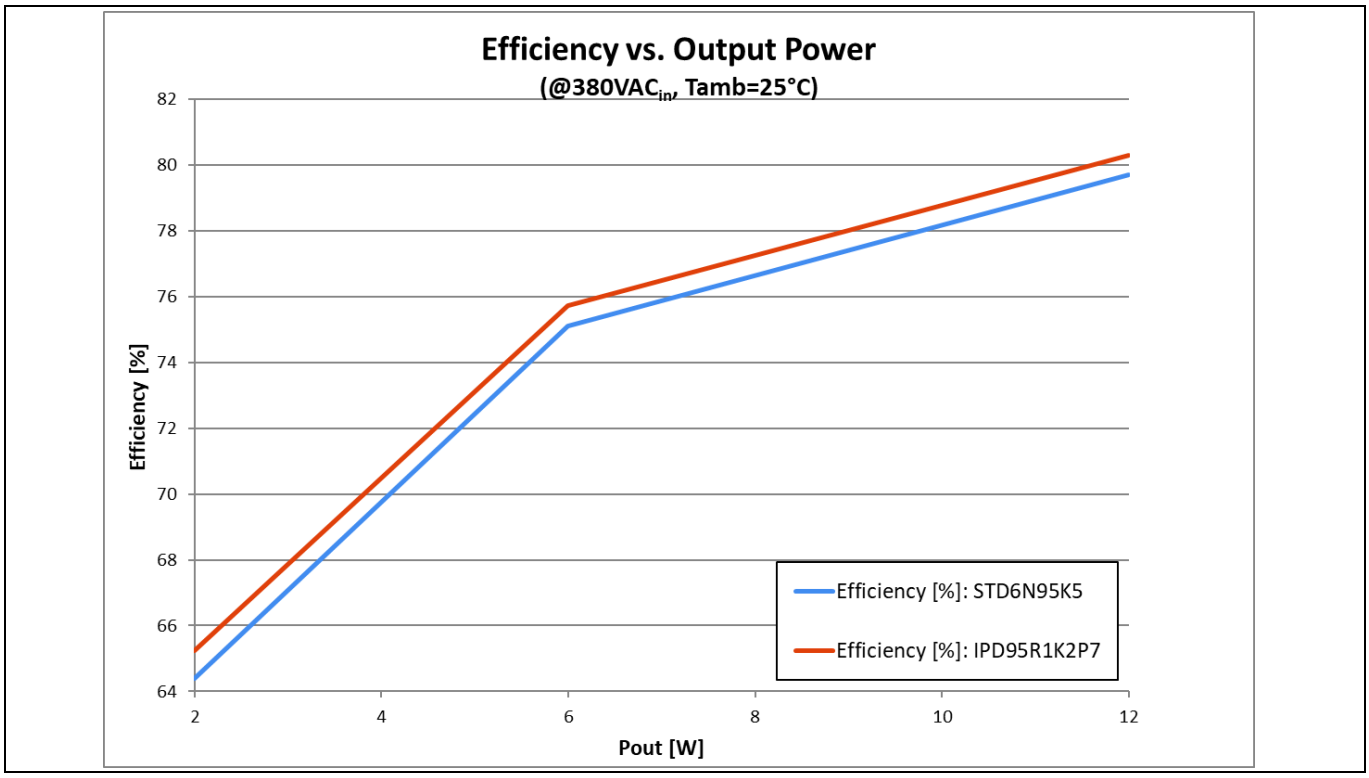


Figure 1 IPD95R1K2P7 shows better efficiency benefits across the load range compared to the competition

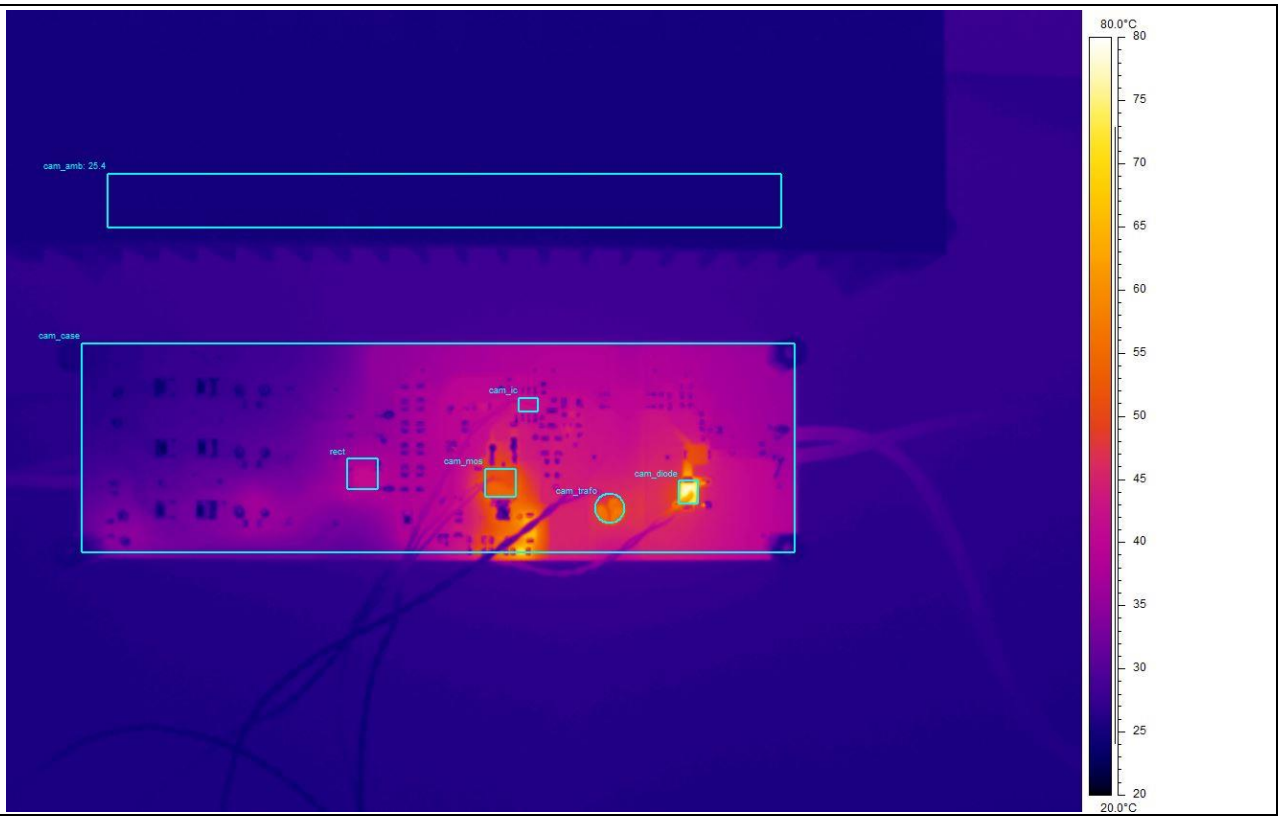
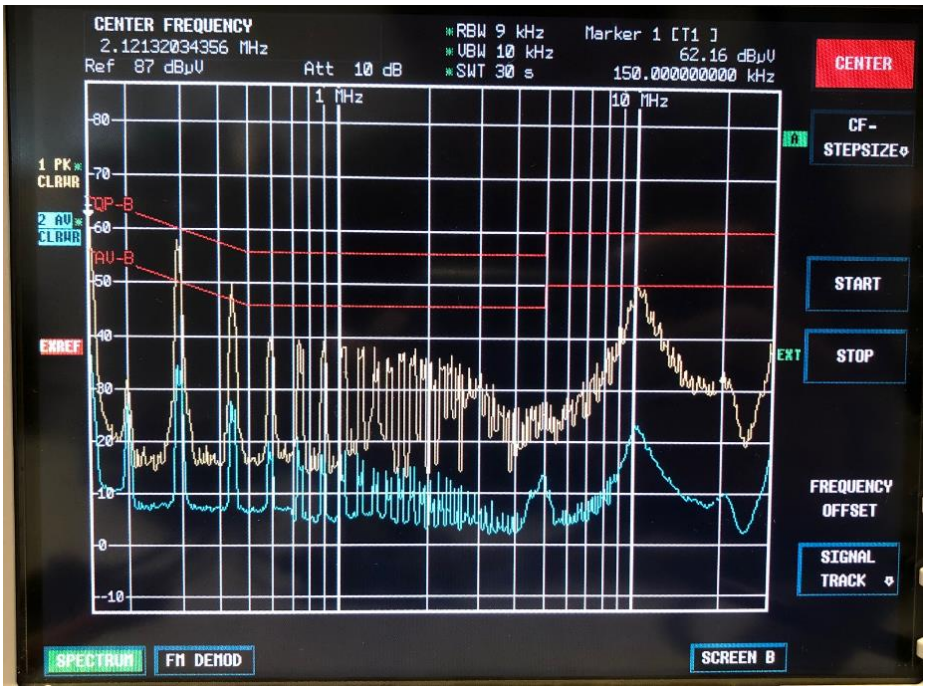


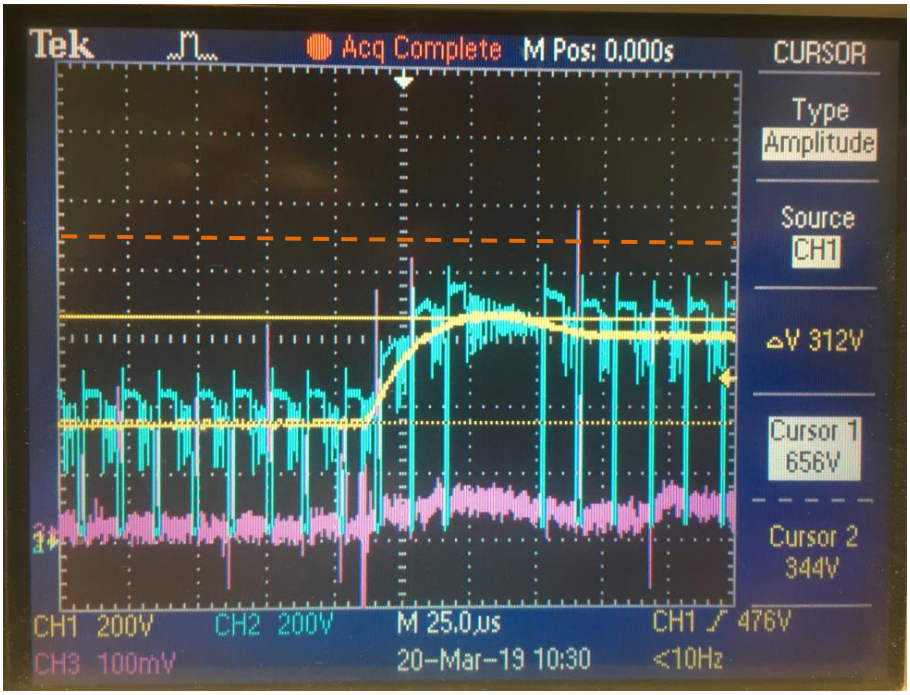
Figure 2 **IPD95R1K2P7 meets thermal requirements with a maximum temperature on board of less than 80°C seen at 12 W full-load operation with a 25°C ambient temperature and a 230 V AC_{in} (open-case measurement)**



Ch1 (yellow): QP spectrum
Ch2 (blue): Average spectrum

Figure 3 **IPD95R1K2P7-based 12 W smart meter power supply demo board meets conducted EMI (EN 55022 class B)**

Overview and key results



Ch1 (yellow): Voltage across the bulk capacitor (V_{bulk})
Ch2 (blue): MOSFET drain-source voltage (V_{DS})
Ch3 (red): Voltage across the sense resistor (R_{sense} 1.8 Ω)
Orange: 950 V breakdown voltage rating of switch

Figure 4 IPD95R1K2P7-based 12 W smart meter power supply demo board meets IEC61000-4-5 combination wave surge test (2 kV L-N)

Key features summary:

- Suitable evaluation board for validation of ICE5 controller in combination with the latest 950 V CoolMOS™ P7
- Overall system efficiency is boosted up to 80 percent at the 12 W full-load point
- 950 V CoolMOS™ P7 out-performs closest competitor part and former 900 V C3 technology
- Further increased overall lifetime and voltage spike safety margin with 950 V technology
- MOSFET temperature stays below 80°C with 950 V CoolMOS™ P7 (T_{amb} = 25°C; open case; 230 V AC_{in})
- Conducted and radiated EMI spectrum passes engineering standards (with around 2 dB margin)
- Board passed 2 kV surge test (L-N) with adequate headroom to breaking voltage of switch
- Excellent protection features of ICE5QSAG controller provide additional safety in abnormal contitions

2 Board introduction

The distinguishing features of this 12 W reference design are high efficiency, the regulation of output voltage and current over a wide input voltage range, good EMI performance, and various protection modes for high reliability.

This document contains the list of features, the power supply specification, schematic, bill of materials and the transformer construction documentation. Typical operating characteristics such as performance curves and oscilloscope waveforms are shown at the end.

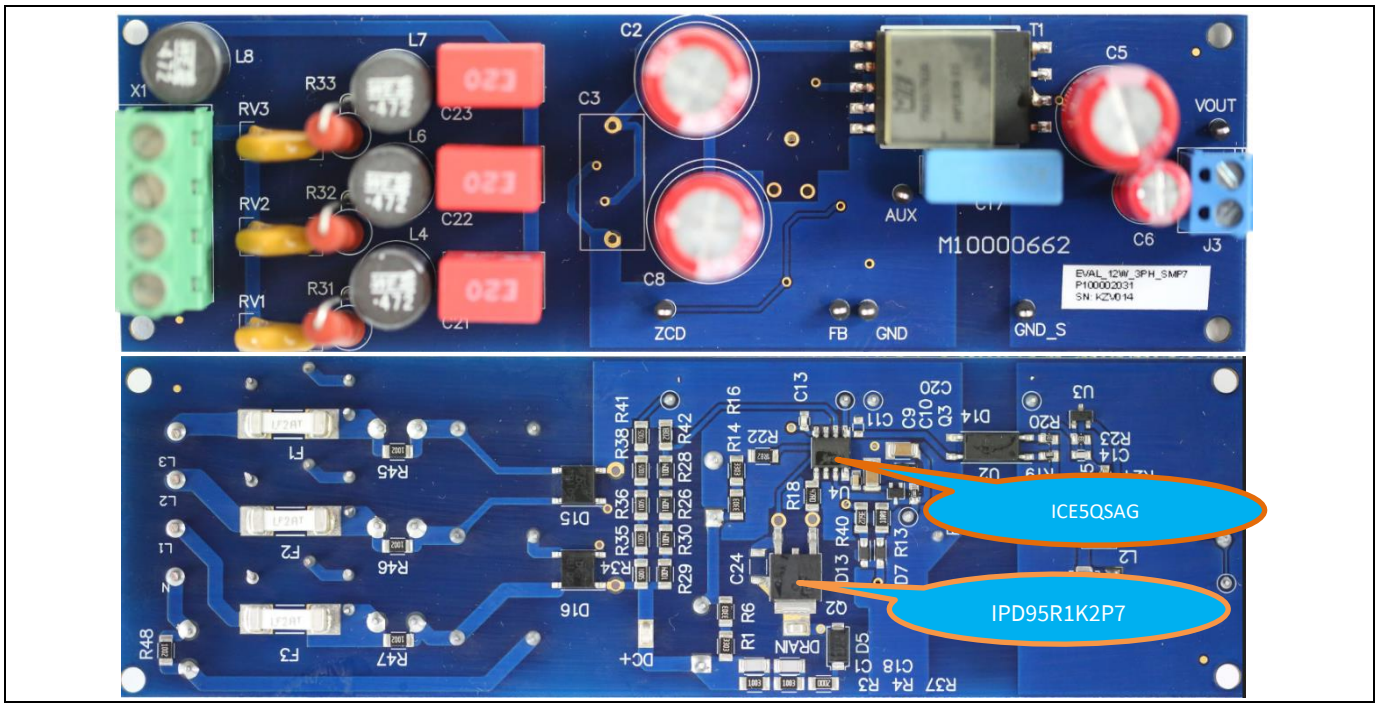


Figure 5 12 W/12 V, 1 A single-output demo board based on IPD95R1K2P7, the new 950 V CoolMOS™ P7

The new 950 V CoolMOS™ P7 SJ MOSFET is used in the power conversion stage. The need for and benefits of such a device are explained below:

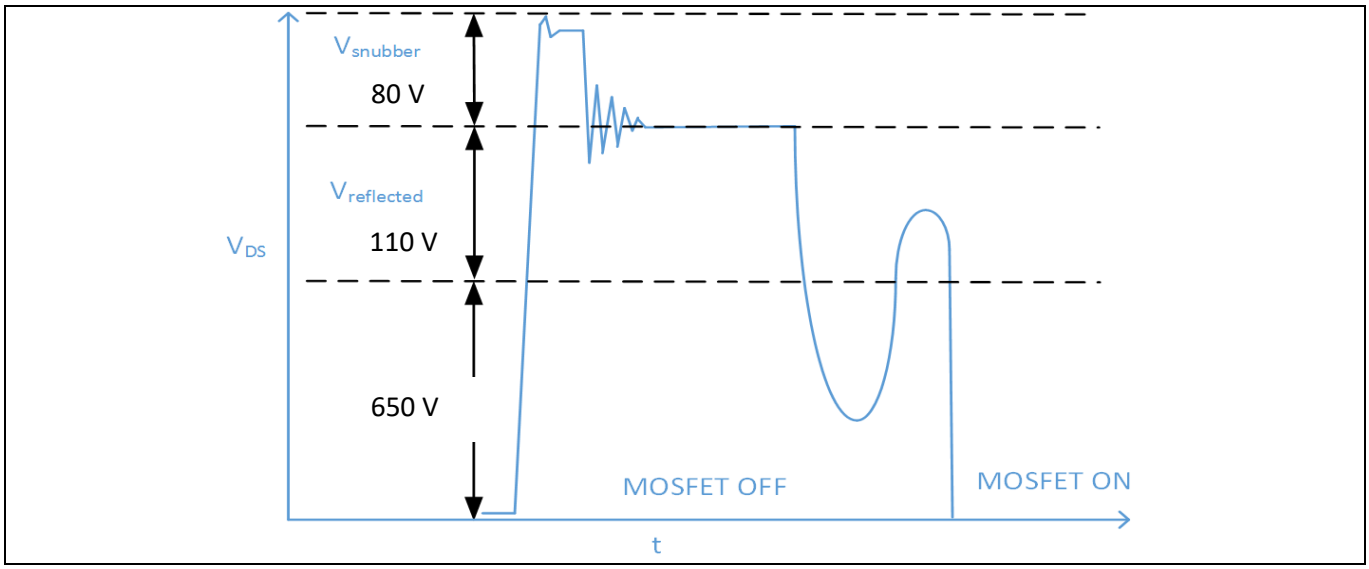


Figure 6 The MOSFET drain-source voltage in a Flyback converter is the sum of the bus voltage (V_{bus}), reflected voltage ($V_{reflected}$), and snubber voltage ($V_{snubber}$).

Board introduction

In general the 950 V CoolMOS™ P7 provides several benefits in low-power three-phase-input power supply applications when compared to 700 V and 800 V MOSFETs. The additional breakdown voltage is used to increase the safety margin during cold ambient temperature start-up and regular operation, with the increase in allowable AC input voltage increasing the surge capability of designs. The P7 family of devices also performs better when comparing switching losses to previous generations of MOSFETs. This increases the efficiency of the overall power supply design.

A 950 V breakdown voltage allows a higher combination of bus voltage, reflected voltage and snubber voltage. This enables increasing the snubber and reflected voltage to lower the switching losses of the Flyback converter. This extra voltage margin is a requirement as bus voltages in three-phase systems are beyond the typical 300 V AC high-line of a single-phase system. The device can also be used as a drop-in replacement for 700 V and 800 V devices to give additional margin for abnormal conditions such as surge and output short-circuit conditions in existing designs that need improved margins. This additional 150 to 250 V of drain-source breakdown voltage gives designers more flexibility to improve the overall design.

The CoolMOS™ P7 family of devices also has an improved switching performance that is better than existing Infineon and competitor devices. One switching loss mechanism is the E_{OSS} of the MOSFET. The E_{OSS} is the main loss contributor for the turn-on of the MOSFET in a QR Flyback. The energy that is stored in the output capacitance of the MOSFET needs to be discharged every cycle before the MOSFET is turned on. The output capacitance energy storage of the 950 V CoolMOS™ P7 is better when compared to equivalent competitor devices. This improvement is most significant at higher AC input voltages.

Additional details about the 950 V CoolMOS™ P7 device improvements such as the reduced gate charge Q_g, $R_{DS(on)}$ temperature dependency, the charge stored in the output capacitance Q_{OSS}, and transfer characteristics can be found in the 950 V CoolMOS™ P7 application note [3].

2.1 DCM Flyback (fixed frequency)

The DCM Flyback is typically used at lower output loads. In a standard DCM Flyback the output is also regulated by the duty cycle. This set-up is popular in smart meter applications due to the EMI concerns with the PLC communication and potential noise issues caused by variable frequency operation. Since there are no efficiency standards requiring light-load efficiency improvements, this mode of operation is still acceptable. The principle of operation and simplified waveforms are shown in Figure 7, below.

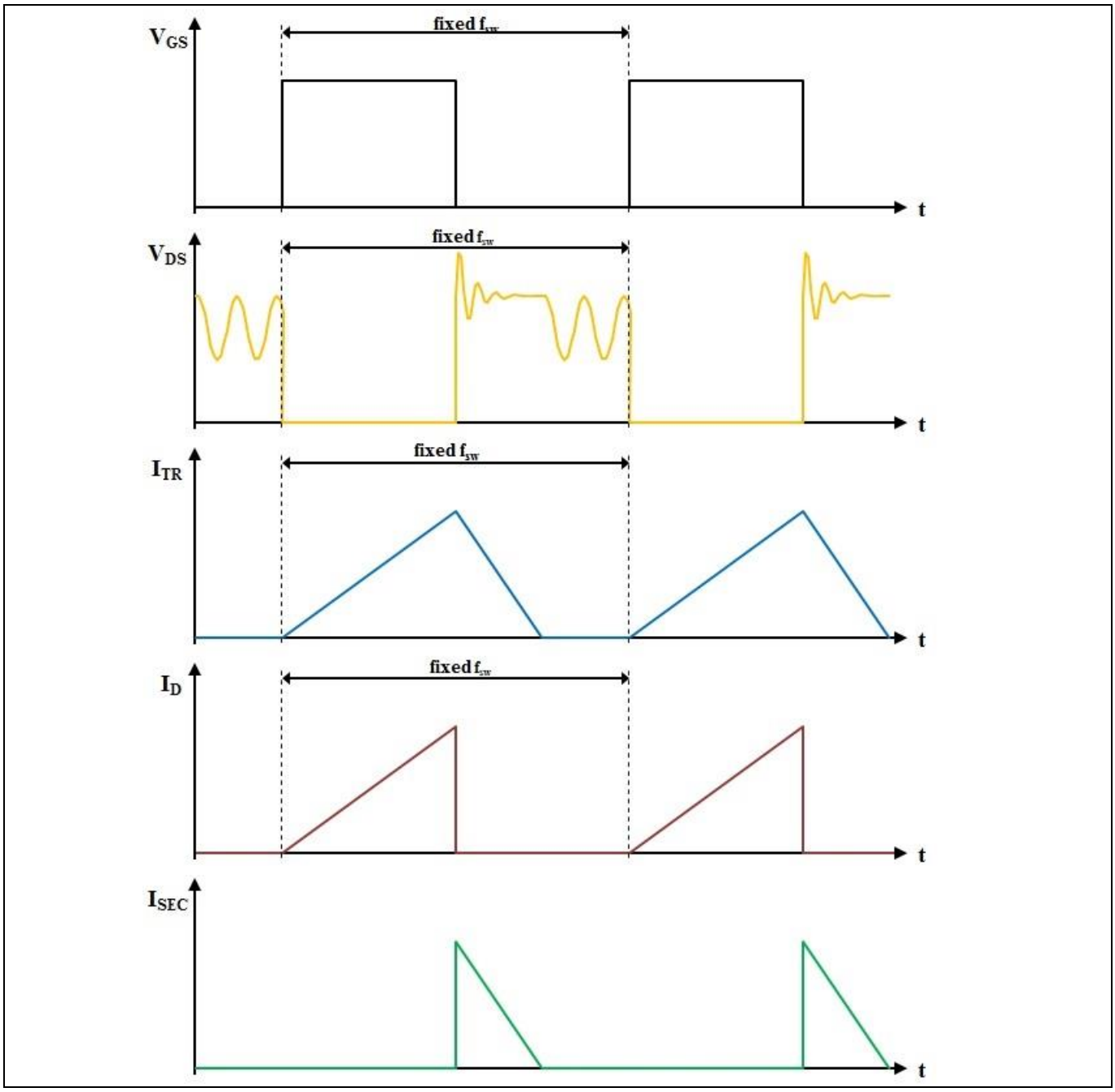


Figure 7 DCM Flyback principle of operation

2.2 QR Flyback (variable frequency)

QR Flyback topologies are now being considered in smart meter applications. They offer better performance due to lowering the switching losses. A QR Flyback can only operate in DCM, because it switches the MOSFET on during the oscillation phase of drain node capacitance and transformer main inductance when the current through the main transformer is 0 A. The difference between a standard DCM Flyback and QR operation is that the MOSFET is able to turn on at minimum V_{DS}, which reduces the E_{OSS} losses. This behavior is called valley switching and can be seen in Figure 8.

Board introduction

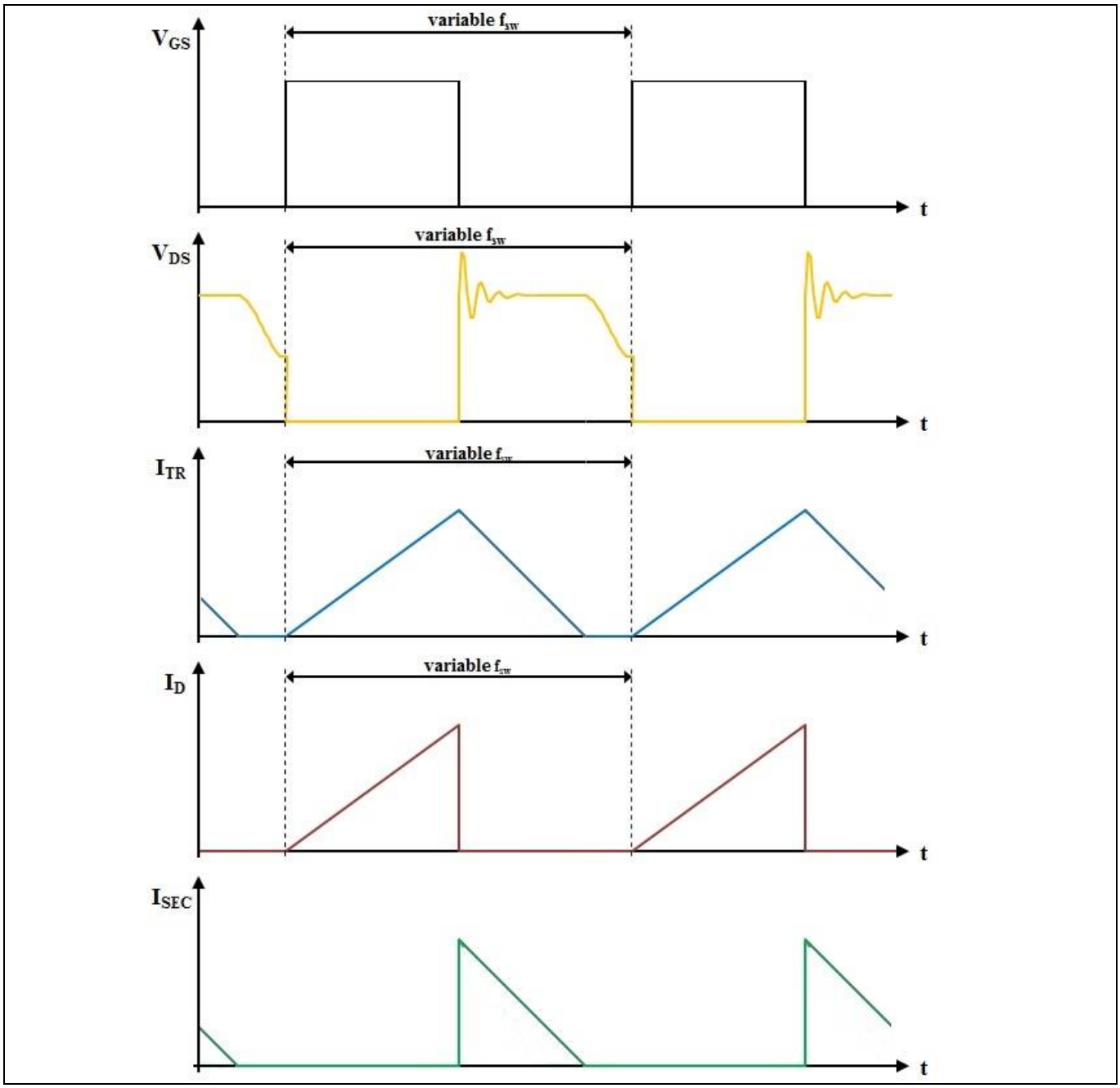


Figure 8 QR Flyback principle of operation

Typically, at very light loads, the MOSFET turns on in a later valley while at heavy loads the MOSFET turns on in the first valley. As described, the V_{DS} oscillation is given by the capacitance value on the drain node and is influenced by the output capacitance of the MOSFET (C_{OSS}). In this case the switching frequency can be influenced by MOSFET selection.

There are other Flyback solutions available, such as cascaded (StackFET™) Flyback or cascoded (Infineon patented topology) Flyback, used in smart metering power supplies. These solutions are not considered in this application note. The 950 V CoolMOS™ P7 is intended for a Flyback application only where there is no hard commutation of a conducting body diode, which can occur due to the ruggedness of the body diode, commonly seen in half-bridge topologies.

2.3 Unique features of the fifth-generation QR controller

2.3.1 Fast self-start-up and sustaining of V_{CC}

The IC start-up uses the cascode structure integrated into the package to charge up the V_{CC} capacitor during the start-up stage. The Zero Crossing Detection (ZCD) pin (pin 4) is a multi-function pin and it serves as the start-up pin with the connection of pull-up resistors R34 to R38 and R41, which has the other end connecting to the bus voltage during the start-up phase. The device is implemented with two steps of charging current: the smaller current 0.2 mA (VVCC_typ = 0 V~1.1 V) and the larger current 3.2 mA (VVCC_typ = 1.1 V~16 V). The start-up time consists of the addition of those two charging times. With a V_{CC} capacitor C20 at 10 µF, the start-up time is shortened to around 0.35 s.

After start-up, the IC V_{CC} supply is sustained by the auxiliary winding of transformer T1, which needs to support the V_{CC} to be above Under Voltage Lockout (UVLO) voltage (10 V typ.) through the rectifier circuit D7, R13 and C20.

2.3.2 QR switching with valley sensing

ICE5QSAG is a QR Flyback controller, which always turns on at the lowest valley point of the drain voltage. The IC senses the valley point through the ZCD pin (pin 4), which monitors the auxiliary winding voltage by R40, D13 and C13 to the ZCD pin (pin 4) together with the internal resistor R_{ZCD}. The IC detects the valley crossing signal. When the ZCD voltage drops below 100 mV (typ.), the CoolMOS™ is switched on. With QR switching, the lowest switching losses can be achieved for good efficiency.

2.3.3 System robustness and reliability through protection features

2.3.3.1 Input voltage monitoring and protection

To avoid system damage due to the high AC input transient, the SMPS unit requires the input-line Over Voltage Protection (OVP) to stop the Flyback converter switching whenever the V_{bus} voltage exceeds the operating range. The IC has a VIN pin (pin 2), which can sense V_{bus} voltage through voltage dividers R29, R30, R26 and R28. When the VIN pin exceeds the protection threshold 2.9 V (typ.), the IC stops switching. With the same VIN sensing, ICE5QSAG also implements input Under Voltage Protection (UVP) (brown-in/brown-out) to prevent the Over Current (OC) stress of the power-stage components when the input voltage is too low.

2.3.3.2 Other protections with auto-restart

Besides input OVP and UVP, the ICE5QSAG has more comprehensive system protection features, such as V_{CC} OV, V_{CC} UV, over-load, output short-circuit, open-loop protection, output OV, over-temperature, Current Sense (CS) short-to-GND, V_{CC} short-to-GND, etc.

2.4 Demo board protection features

Fold-back point protection – For a QR Flyback converter, the maximum possible output power is increased when a constant current limit value is used across the entire mains input voltage range. This is usually not desired, as this will increase the cost of the transformer and output diode in the case of output over-power conditions. The internal fold-back protection is implemented to adjust the V_{CS} voltage limit according to the bus voltage. Here the input-line voltage is sensed using the current flowing out of the ZC pin, during the MOSFET on-time. As the result, the maximum current limit adjusts with the AC-line voltage.

V_{CC} OVP and UVP – During normal operation, the V_{CC} voltage is continuously monitored. When the V_{CC} voltage increases to V_{VCC} OVP or V_{CC} voltage falls below the UVLO level V_{VCC} off, the IC will enter auto-restart mode.

Board introduction

Over-load/open-loop protection – In the case of an open control loop, the feedback voltage is pulled up with an internal block. After a fixed blanking time, the IC enters auto-restart mode. In case of a secondary short-circuit or over-load, the regulation voltage V_{FB} will also be pulled up, the same protection is applied and the IC will auto-restart.

Adjustable output OVP – During the off-time of the power switch, the voltage at the ZC pin is monitored for output OV detection. If the voltage is higher than the pre-set threshold 3.7 V for a pre-set period of 100 µs, the IC is latched off.

Auto-restart for over-temperature protection – The IC has a built-in over-temperature protection function. When the controller's temperature reaches 140°C, the IC will shut down the switch and enter auto-restart. This can protect the power MOSFET from overheating.

Short winding protection – The source current of the MOSFET is sensed via an external resistor R22. If the voltage at the CS pin is higher than the pre-set threshold V_{CSSW} of 1.68 V during the on-time of the power switch, the IC is latched off. This constitutes a short-winding protection. To avoid an accidental latch-off, a spike blanking time of 190 ns is integrated into the output of the internal comparator.

3 Board specifications

This demo board is targeted at smart meter and home appliances requiring an auxiliary power supply with an input from a single- or three-phase source.

The power efficiency of the demo board is in the range of 80 percent.

Default full-load operating condition (also in all measurements in this document) is 12 V and 1 A at the output for the DPAK evaluation. Ambient temperature was stabilized to 25°C (+/-1°C).

Attention: ***This is a high input voltage design. Lethal voltages are present on the primary side. Using appropriate safety equipment is advised while evaluating this demo board.***

Board design specifications

Description	Symbol	Min.	Typ.	Max.	Units	Comments
Input						
Voltage	V_{IN}	185	–	460	V AC	Three-phase, four wires
Frequency	f_{LINE}	47	50/60	64	Hz	
Output						
Output voltage	V_{OUT}	–	12	–	V	±5 percent
Output current	I_{OUT}	0	–	1	A	
Output voltage ripple	V_{RIPPLE}	–	–	200	mV	20 MHz BW
Max. power output	P_{OUT_Max}	–		12	W	
Efficiency						
Max. load	η	–	80	–	%	230 V AC
Environmental						
Conducted EMI		2	–	–	dB	Margin, CISPR 22 class B
Surge immunity						
Differential Mode (DM)		2	–	–	kV	EN 61000-4-2
Common Mode (CM)		4	–	–	kV	EN 61000-4-5
Ambient temperature	T_{amb}	0*	–	50	°C	Free convection, sea level *usage less than 0°C possible

4 Build information

All design details and raw data can be downloaded from the official 950 V CoolMOS™ P7 webpage, which can be found under www.infineon.com/P7 following the path to 950 V and “Boards” to the download section.

The evaluation board was laid out with the Altium Designer v18.

4.1 Schematic

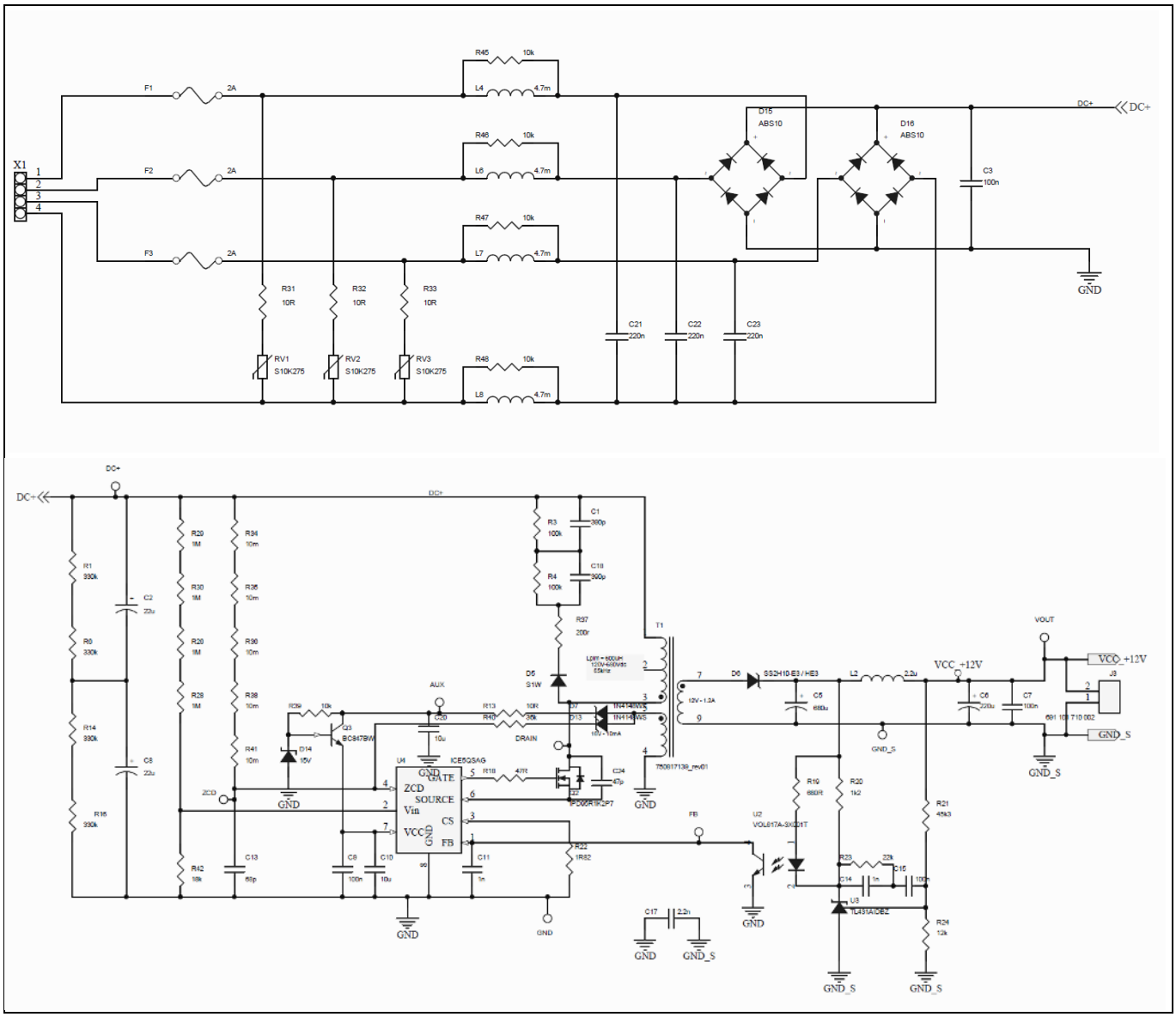


Figure 9 Board schematic (EVAL_12W_3PH_SM_P7)

4.2 Board layout

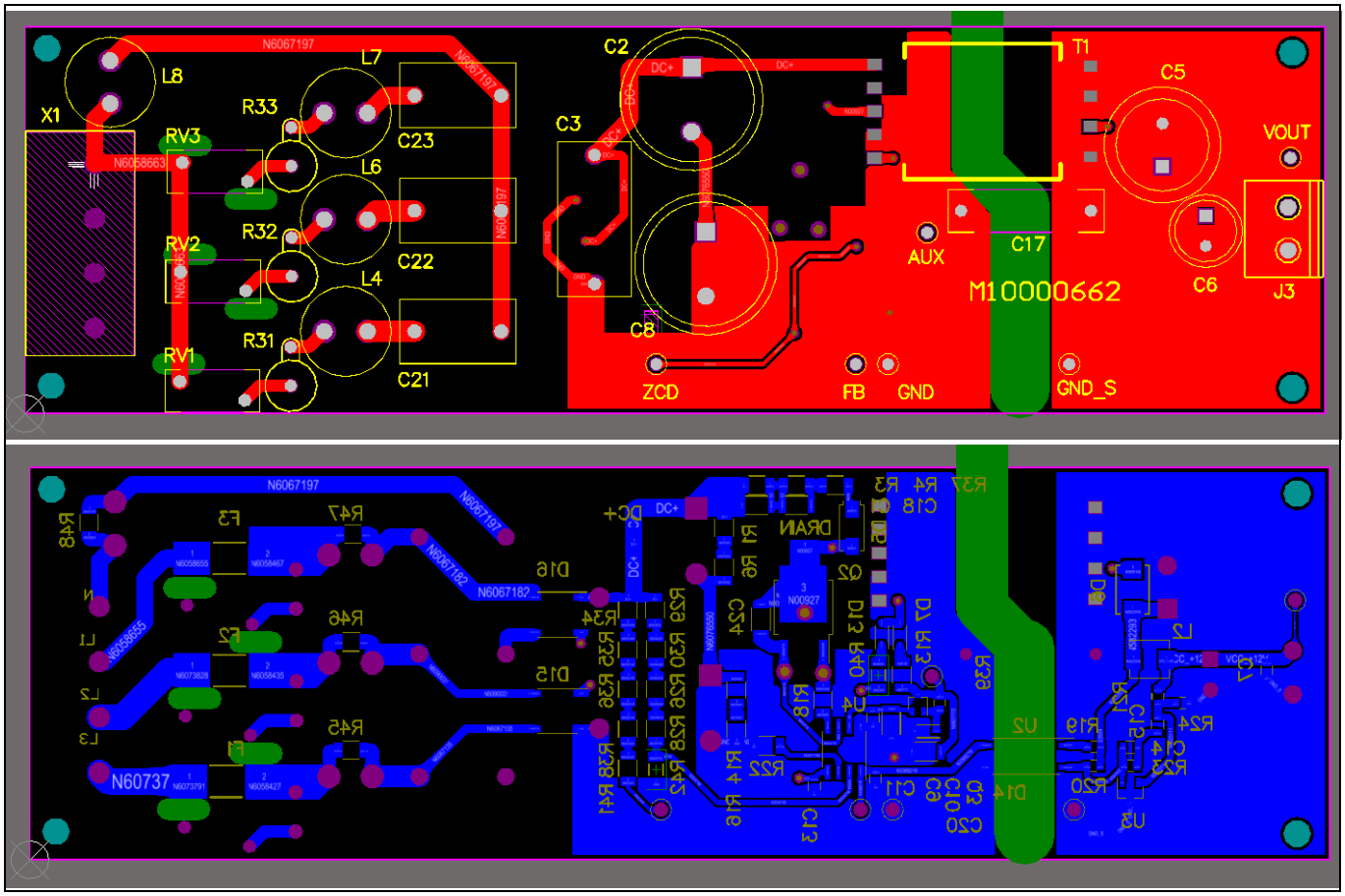


Figure 10 Board layout top view (up) and bottom view (down)

4.3 Bill of Materials

The Bill of Materials (BOM) for manufacturing can be seen in the table below:

Quantity	Part reference	Value	Description	Manufacturer
6	AUX FB GND GND_S VOUT ZCD	Test point	(THM) Thru-hole test points	Keystone
2	C1, C18	390 pF	390 pF/630 10 percent C0G 3216	TDK
2	C2, C8	22 µF	22 µF/400 V 20 percent aluminum 12.5 x 20	Würth
1	C5	680 µF	680 µF/35 V aluminum 13 x 20	Würth
1	C6	220 µF	220 µF/35 V 20 percent aluminum 8 x 16	Würth
3	C7, C9, C15	100 nF	100 nF/50 10 percent X7R 1608	TDK
2	C10, C20	10 µF	10 µF/35 10 percent X7R 3216	TDK
1	C13	68 pF	68 pF/50 5 percent C0G 1608	TDK
1	C14	1 nF	1 nF/50 5 percent C0G 1608	TDK
1	C17	2.2 nF	2.2 nF/500 V AC 20 percent EMI suppression capacitors Y1/500 V AC	TDK

Build information

Quantity	Part reference	Value	Description	Manufacturer
3	C21, C22, C23	220 nF	220 nF/310 V 10 percent EMI suppression capacitors X2/310 V AC	Würth
1	D5	S1W	Surface-mount silicon rectifier diodes	Diotec
1	D6	SS2H10-E3/ HE3	HV surface-mount Schottky rectifier	Vishay
2	D7, D13	1N4148WS	Small-signal fast-switching diode	Vishay
1	D14	15 V	15 V 0.2 W small-signal Zener diodes	Vishay
2	D15, D16	ABS10	Surface-mount Si-bridge rectifier with 4 mm pitch	Diotec
2	DC + DRAIN	Test point	(SMT) Surface-mount test points	Keystone
3	F1, F2, F3	2 A	2 A 600 V AC surge resistant 461 series TeleLink® fuse	Littelfuse
3	J1, J2, J3	691, 101, 710 002	2-pin series 101 to 5.00 mm Horiz. entry modular WR-TBL	Würth
1	L2	2.2 µH	WE-LHMI SMD power inductor	Würth
4	L4, L6, L7, L8	4.7 mH	WE-TIS shielded radial leaded wire-wound inductor	Würth
1	Q2	IPD95R1K2P7	950 V CoolMOS P7 power transistor	Infineon
1	Q3	BC847BW	NPN silicon AF transistors	Infineon
4	R1, R6, R14, R16	330 k	330 k 0.25 W 1 percent 1206	Vishay
2	R3, R4	100 k	100 k 0.25 W 1 percent 1206	Vishay
1	R13	10 R	10 R 0.25 W 1 percent 1206	Vishay
1	R18	47 R	47 R 0.25 W 1 percent 1206	Vishay
1	R19	680 R	680 R 0.1 W 1 percent 0603	Vishay
1	R20	1k2	1k2 0.1 W 1 percent 0603	Vishay
1	R21	45k3	45k3 0.1 W 1 percent 0603	Vishay
1	R22	1R82	1R82 0.25 W 1 percent 1206	Vishay
1	R23	22 k	22 k 0.1 W 1 percent 0603	Vishay
1	R24	12 k	12 k 0.1 W 1 percent 0603	Vishay
4	R26, R28, R29, R30	1 M	1 M 0.25 W 1 percent 1206	Vishay
3	R31, R32, R33	10 R	3 W power metal film leaded resistors	Vishay
5	R34, R35, R36, R38, R41	10 M	10 M 0.25 W 1 percent 1206	Vishay
1	R37	200 R	200 R 0.25 W 1 percent 1206	Vishay
1	R39	10 k	10 k 0.1 W 1 percent 0603	Vishay
1	R40	36 k	36 k 0.1 W 1 percent 0603	Vishay
1	R42	18 k	18 k 0.1 W 1 percent 1206	Vishay
4	R45, R46, R47, R48	10 k	10 k 0.25 W 1 percent 1206	Vishay
3	RV1, RV2, RV3	820412711	Disk varistor high surge WE-VD	Würth
1	T1	750317626	Transformer for 15 W 12 V V_{ref} = 108 V SMPS	Würth

Build information

Quantity	Part reference	Value	Description	Manufacturer
1	U2	VOL617A-3X001T	Optocoupler, phototransistor output, 4-pin LSOP, long creepage mini-flat package	Vishay
1	U3	TL431AIDBZ	Precision programmable reference	TI
1	U4	ICE5QSAG	QR controller	Infineon

4.4 Transformer specification

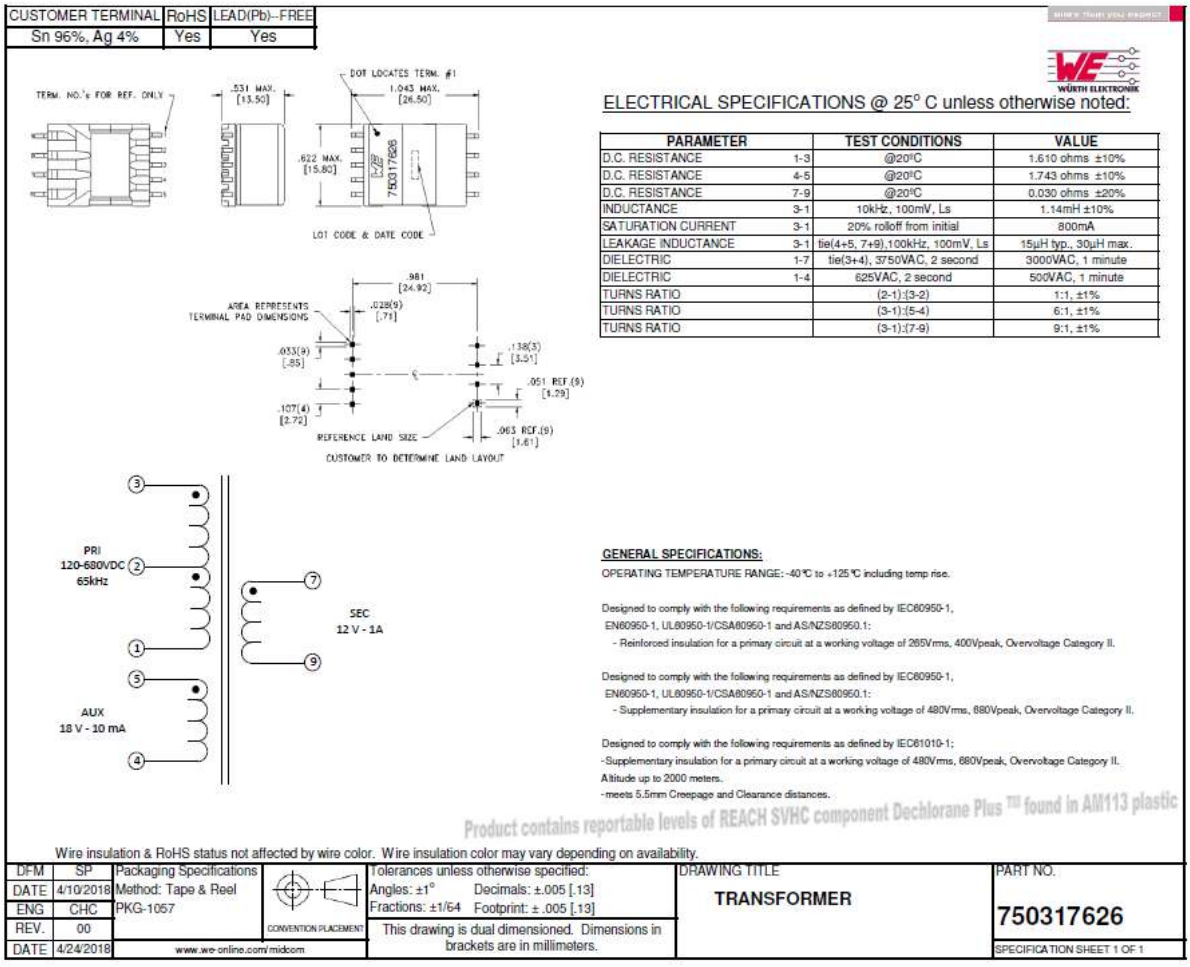


Figure 11 Transformer construction (Würth customized design for Infineon Technologies Austria AG)

The transformer for the 12 W demo board is a customized part manufactured by Würth Electronik (part no. 750317626). This transformer is designed for metering applications.

The turns ratio, primary inductance and other design specifications are calculated with the online tool for the QR controller: Calculation Tool Quasi-Resonant CoolSET™ Generation 5

Key characteristics of the chosen transformer are as follows:

- Low profile: 12.7 mm max. height
- Wide V_{IN}: 85 to 480 V AC
- Meets 5.5 mm creepage and clearance distances
- Single or dual outputs

Build information

- Output options of 5, 12, 15 and 18 V DC
- Self-shielding package
- Reinforced insulation
- Isolation voltage: 3000 V AC (4000 V AC at 1 s)
- Lead-free and RoHS compliant
- Designed to meet IEC61010-1, IEC60950-1 (up to 10 kV surge)
- Operating temp.: -40°C to 125°C

5 Circuit description

In this section, the design circuit for the SMPS unit will be briefly described by the different functional blocks. For details of the design procedure and component selection for the Flyback circuitry please refer to the IC design guide and calculation tool.

5.1 EMI filtering and line rectification

The input of the demo board is taken from the three-phase AC power grid, which is in the range of 185 V AC~460 V AC. The fuses F1 to F3 are at the entrance to protect the system in case of excess current entering the system circuit due to any fault. Following are the varistors RV1, RV2, RV3, connected across L and N to absorb the line surge transient. Inductors L1, L3 and C3 form a filter to attenuate the DM conducted EMI noise. C3, when mounted, must be X-capacitor grade. The CM noise filtering is mainly done by C17. The bridge rectifiers D15, D16 rectify the AC input into DC voltage, filtered and stabilized by the bulk capacitor C2, C8.

5.2 Flyback converter power stage

The Flyback converter power stage consists of C2, C8, transformer T1, a primary HV MOSFET (CoolMOS™ IPD95R1K2P7), secondary rectification diode D6, secondary output capacitors and filtering (C5, C6 and L2).

When the primary HV MOSFET turns on, some energy is stored in the transformer. When it turns off, the stored energy is released to the output capacitors and the output loading through the output diode D6.

A sandwich winding structure for the transformer T1 is used to reduce the leakage inductance, reducing the loss in the RCD snubber circuit. T1 has one output winding for the V_{OUT} (12 V). The output rectification of V_{OUT} is provided by the diode D6 through the filtering of C5, L2 and C6. All the secondary capacitors must be the low-ESR type, which can effectively reduce the switching ripple. Together with the Y-capacitor C17 across the primary and secondary side, the EMI noise can be further reduced.

5.3 Control of Flyback converter through fifth-generation QR controller ICE5QSAG

5.3.1 PWM control and switching MOSFET

The PWM pulse is generated by the fifth-generation QR PWM current-mode controller ICE5QSAG, and this PWM pulse drives the HV power MOSFET IPD95R1K2P7. The CoolMOS™ provides all the benefits of a fast-switching SJ MOSFET while not sacrificing ease of use. It achieves extremely low conduction and switching losses and can make switching applications more efficient, more compact, lighter and cooler. The PWM switch-on is determined by the ZC input signal and the value of the up/down counter. The PWM switch-off is determined by the FB signal V_{FB} and the CS signal V_{CS}. ICE5QSAG also performs all necessary protection functions in Flyback converters. More details are provided in the product datasheet.

5.3.2 Current sensing

The ICE5QSAG is a current mode controller. The peak current is controlled cycle-by-cycle through the CS resistor R22 on the CS pin (pin 3) so transformer saturation can be avoided and the system is more robust and reliable.

5.3.3 FB and compensation network

Resistor R24 is used to sense the V_{OUT} and FB to pin 1 of U4, which has an error amplifier inside. A type 2 compensation network C14, C15 and R23 is connected between the output pin (pin 3) and the demo pin (pin 2)

of the U3 to stabilize the system. The U3 further connects to pin 2 of the optocoupler, and U2 converts the control signal to the primary side through the connection of pin 4 of the U2 to ICE5QSAG FB pin (pin 1) and complete the control loop.

5.4 Clamping circuit

A clamping network D5, C1, C18, R37, R3 and R4 is used to reduce the switching spikes for the drain pin, which are generated from the leakage inductance of the transformer T1 (see Figure 12).

5.5 PCB design hints

For a good PCB design layout, there are several points to note:

- The power loop needs to be as small as possible (see Figure 12).
- For the primary side, it starts from the bulk capacitor (C2 + C8) positive to the bulk capacitor negative. The power loop components include C2 + C8, the main primary transformer winding (pin 1 and pin 3 of T1), the power MOSFET (Q2) and the CS pin of the controller U4 and CS resistor R22. For the secondary side, the 12 V output starts from the secondary transformer windings (pin 7 of T1), output diode D6 and output capacitor C5.
- A star-ground concept should be used to avoid unexpected HF noise coupling, which can affect control. The ground of the small-signal components, e.g. C9, C10, C11, C13 and R42, and the emitter of optocoupler (pin 3 of U2) etc. should connect directly to the IC ground (pin 8 of U4). Then it connects to the negative terminal of the C8 capacitor directly.

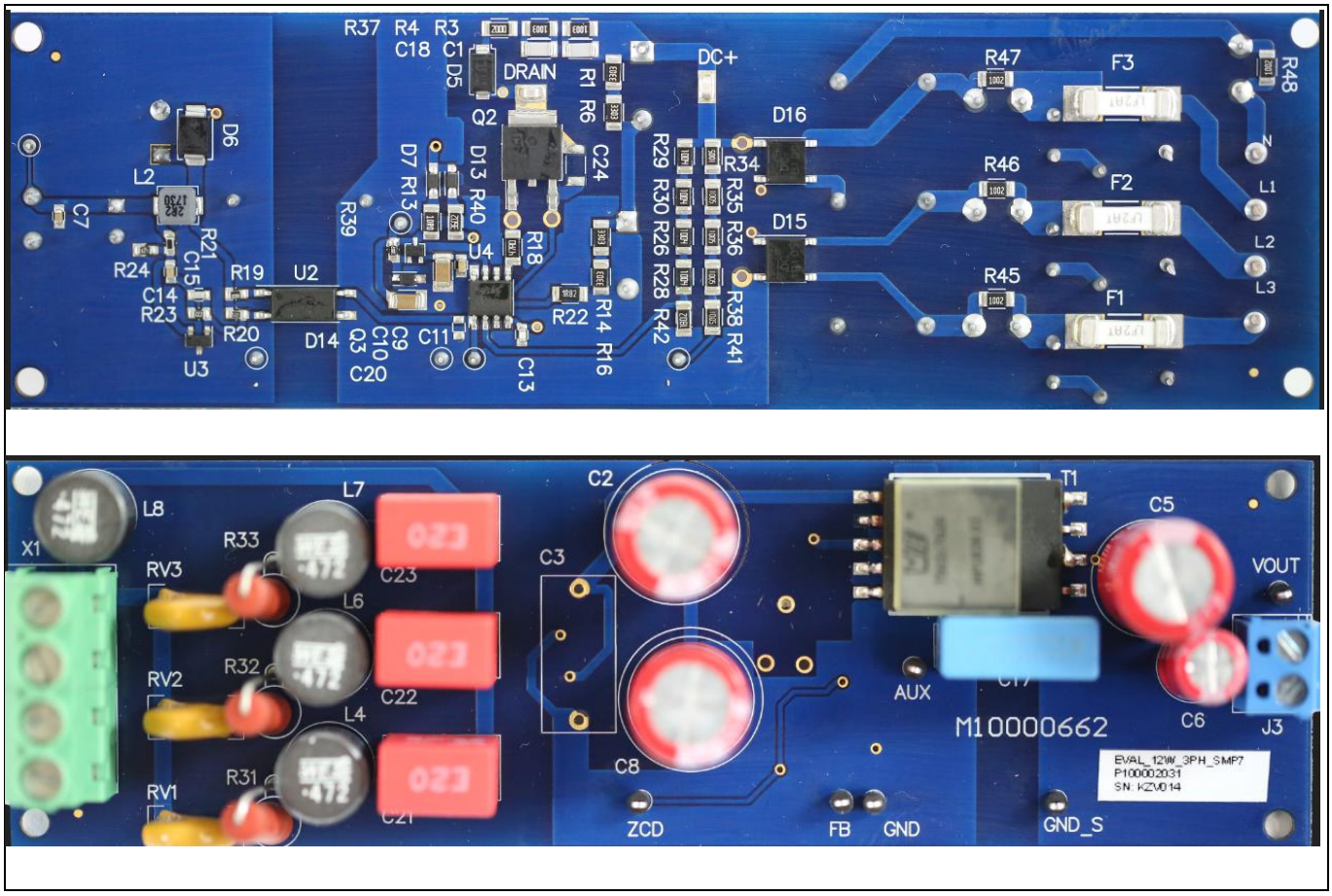


Figure 12 PCB layout (with bottom and top view)

5.6 EMI reduction hints

EMI compliance is critical for smart meter power supply. There are several critical points to consider to achieve satisfactory EMI performance.

- Good transformer winding coupling is very important. Without this there would be high leakage inductance and a lot of switching spike and HF noise. The most effective method is to adopt sandwich winding, where the secondary winding is in the middle of the winding and covered by the primary winding on the bottom and top layer. Shielding the transformer can reduce the HF noise. The outermost shield wrapped around the transformer cores with copper foil can help to reduce leakage flux and reduce the noise coupling to nearby components. The inner shield (copper foil or copper wire winding) between the transformer windings can help to reduce the parasitic capacitance and reduce the HF noise coupling. It has one drawback of increasing common mode noise generated between the primary and the secondary.
- Use short power-loop design in the PCB and terminate to the low-ESR capacitor for the primary-side loop and C5, C6 and C7 for the secondary-side loops. This can help to reduce the switching ripple, which comes out to the input terminals VIN.
- Adequate input LC filter design is important to pass the EMI requirement.
- The Y-capacitor C3 has a function to return the HF noise to the source and reduce the overall HF noise going out to the input terminals. The larger capacitance is more effective; however, a larger value will introduce a larger leakage current and may fail the safety requirements.
- Adding a HV capacitor between drain and source (C24) of the MOSFET can reduce the high switching noise. However, it also reduces efficiency.
- Adding an output common mode choke can also help to reduce the HF noise.

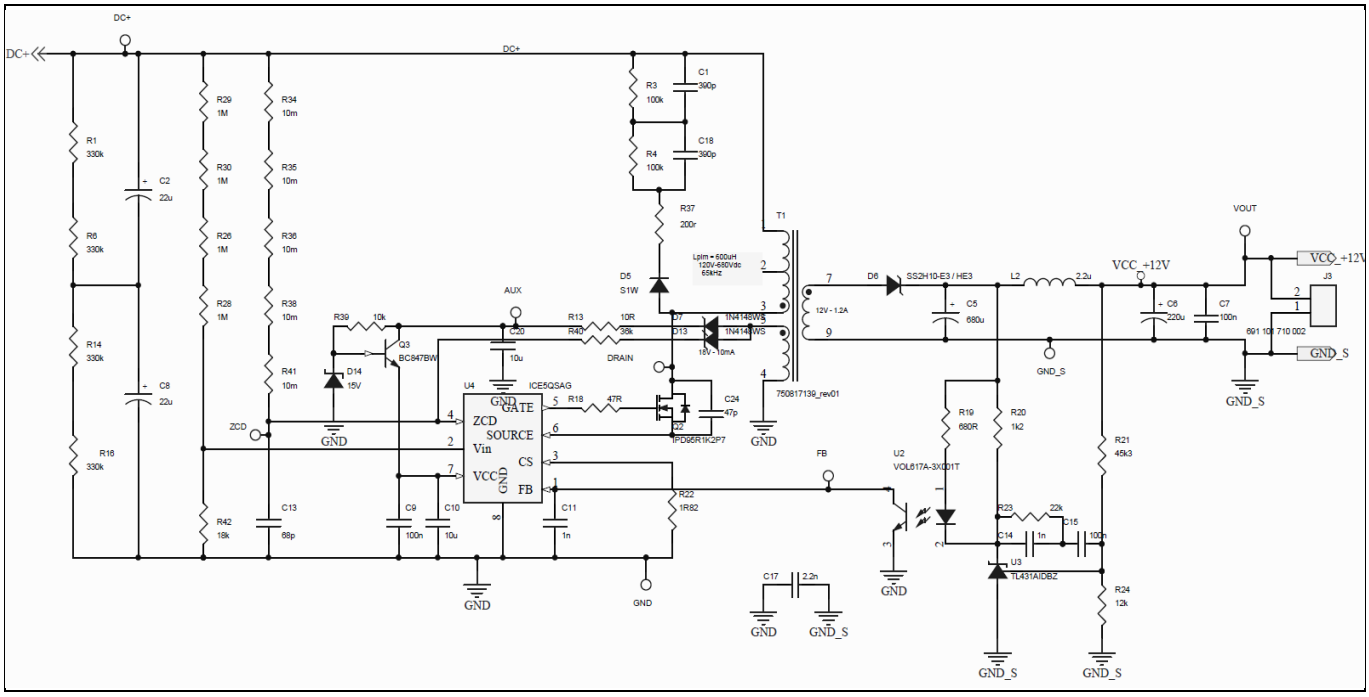


Figure 13 Schematic

6 Test results

6.1 Connections and initial power-up

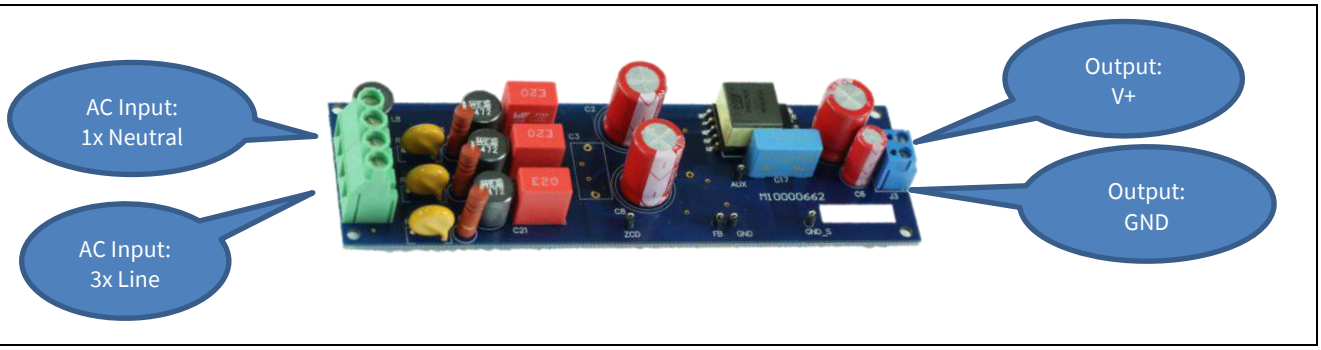
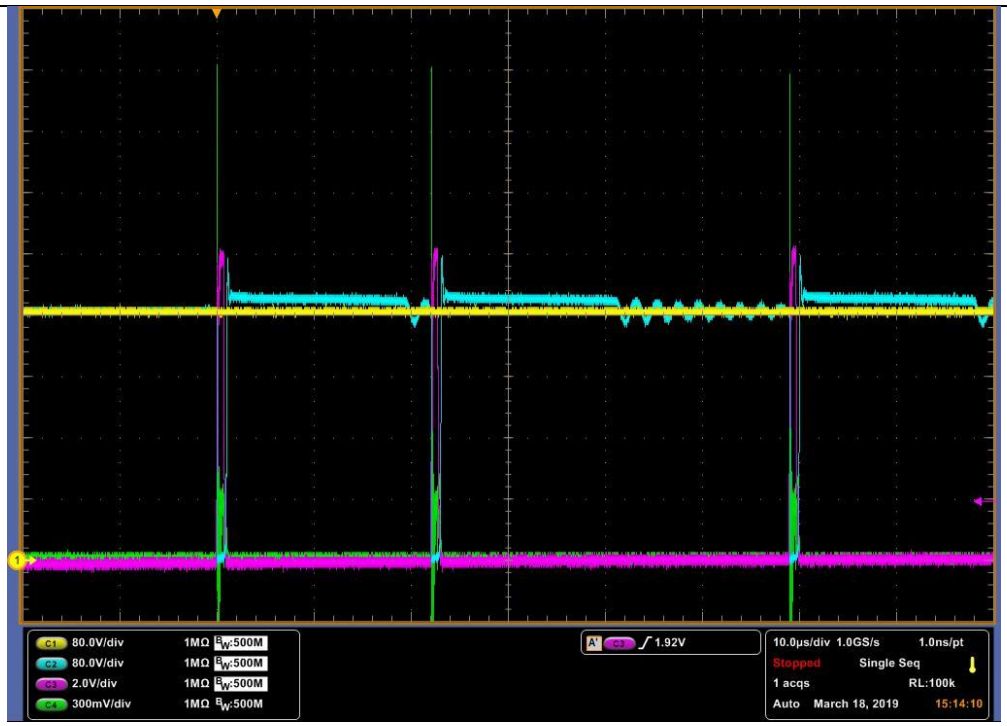


Figure 14 PCB top side showing where to connect AC input and load

Connect the AC input to the board as shown above. The output voltage (V+) and ground (GND) should be connected to an external load on the proper terminals. To load with an external resistor for testing, use a 12 Ω resistor to get 12 W or 1 A at 12 V.

6.2 Start-up

One potential issue with controllers on start-up is that the first few pulses from the controller are a very low voltage, causing the MOSFET channel to not fully turn on. This can cause failures in the system. To check the reliability of the board during start-up the oscilloscope was triggered on the first pulse, which is already outputting 10 V and is not an issue.



Ch1 (yellow): Voltage across the bulk capacitor (V_{bulk})
Ch2 (blue): MOSFET drain-source voltage (V_{DS})
Ch3 (red): MOSFET gate-source voltage (V_{GS})
Ch4 (green): Voltage across the sense resistor (R_{sense} 1.8 Ω)

Figure 15 Start-up waveform at single-phase 230 V AC_{in}

Test results

Ch1 (yellow): Voltage across the bulk capacitor (V_{bulk})
Ch2 (blue): MOSFET drain-source voltage (V_{DS})
Ch3 (red): MOSFET gate-source voltage (V_{GS})
Ch4 (green): Voltage across the sense resistor (R_{sense} 1.8 Ω)

Figure 16 Steady-state switching waveform at single-phase 230 V AC_{in}

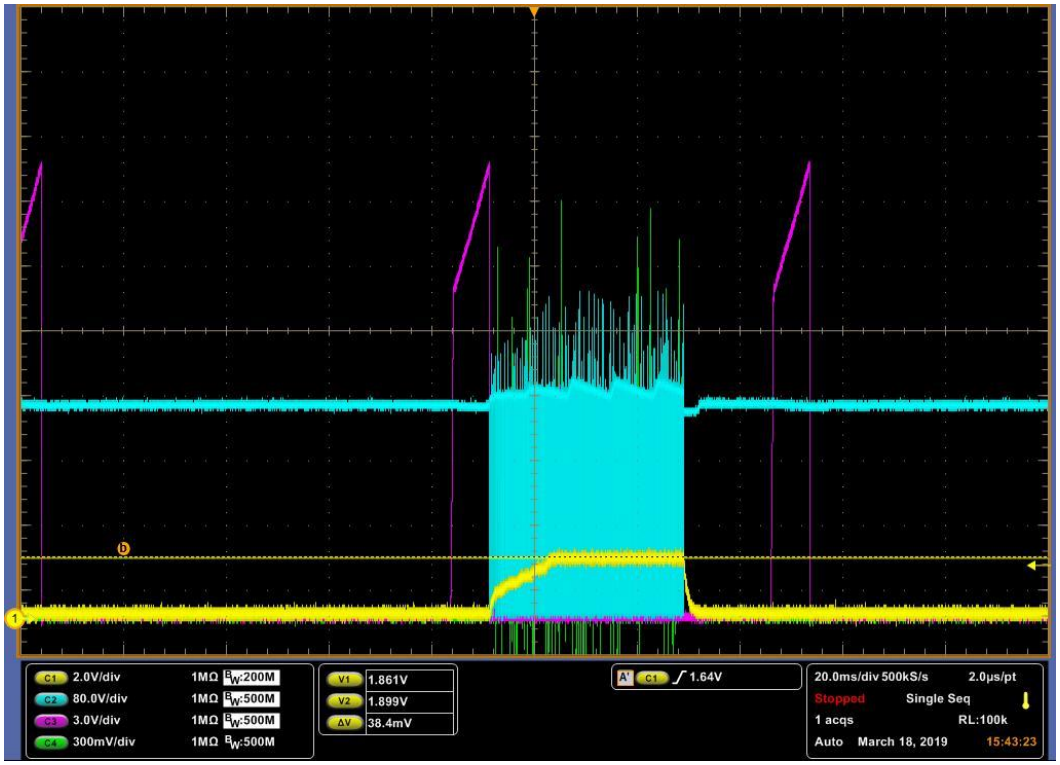
In Figure 16 a standard steady-state switching waveform is shown. The input voltage was 230 V AC single-phase under full-load condition (1 A) setting at the output.

A QR switching in the third valley is given by the QR controller under this condition. Voltage spikes stay below 550 V. With this huge margin, a cold start-up scenario will not lead to a violation of the breakdown voltage rating even at low temperatures.

7 Protections, reliability and EMI

7.1 Output short protection

The tested waveform at start-up and during operation is shown as below; the controller enters into latch mode, and therefore is protected against output short destruction.



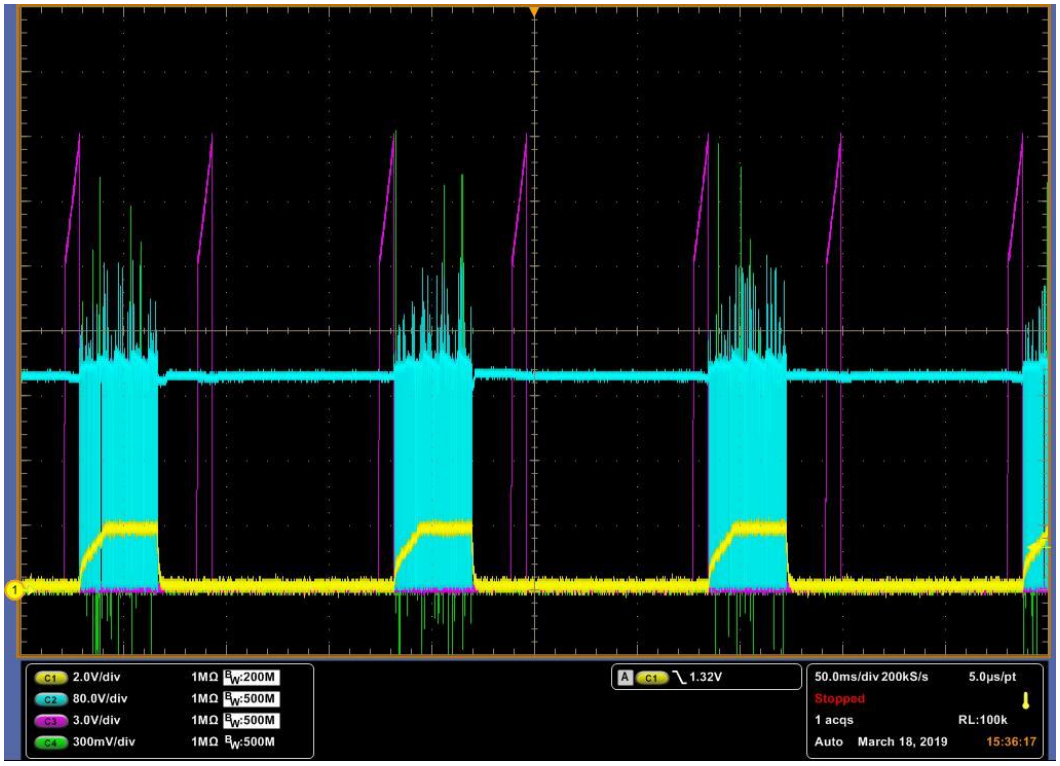
Ch1 (yellow): Voltage across the bulk capacitor (V_{bulk})
Ch2 (blue): MOSFET drain-source voltage (V_{DS})
Ch3 (red): MOSFET gate-source voltage (V_{GS})
Ch4 (green): Voltage across the sense resistor (R_{sense} 1.8 Ω)

Figure 17 Waveform during start-up at single phase 230 V AC_{in}

While running full load and no load the system was tested with a “short” applied to the output to ensure that the hiccup mode was entered quickly enough to avoid any failures of the MOSFET or output diodes.

The short was then removed after running in steady-state short-circuit to ensure that the system recovers and there is no large output voltage overshoot during the recovery.

It can be seen in the waveform below (Figure 18) that there is a hiccup period in between when the system is trying to start up. This ensures that the steady-state temperature at output short-circuit does not get too high.



Ch1 (yellow): V_{CC} voltage (V_{CC})
Ch2 (red): MOSFET drain-source voltage
Ch3 (blue): LED module voltage (V_{LED})
Ch4 (green): LED module current (I_{LED})

Figure 18 Short-circuit waveform during run mode at single-phase 230 V AC_{in}

Due to the optimized control scheme of the ICE5QSAG the whole SMPS is protected against being destroyed after a short-circuit event, no matter if it is in running or start-up mode.

7.2 Breakdown voltage headroom

Running at the maximum allowable AC input voltage of 465 V, 844 V is seen as the maximum MOSFET drain-source voltage. This still gives ~11 percent of margin from the MOSFET breakdown voltage even under worst-case conditions.

Ch1 (yellow): MOSFET gate-source voltage (V_{GS})
Ch2 (blue): MOSFET drain-source voltage (V_{DS})

Figure 19 Voltage headroom at maximum input voltage (465 V AC_{in} three-phase, full load)

With the 950 V CoolMOS™ P7 this margin of around 100 V is still present, also making the design ready to be used under harsh environmental conditions or in cold start-up conditions.

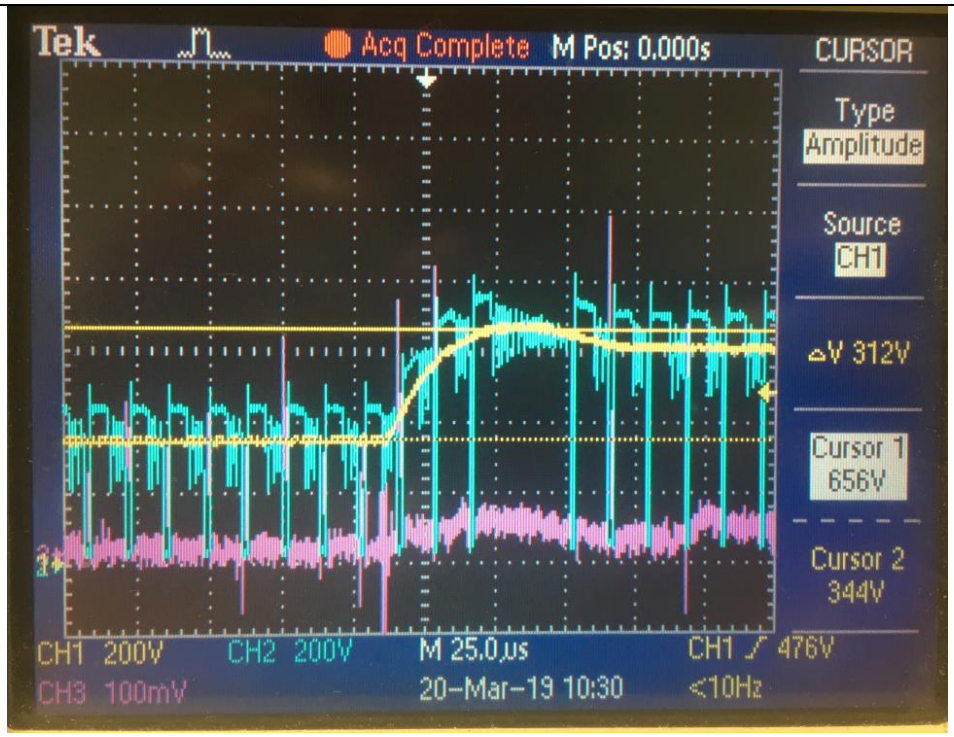
When the design is used below 25°C, the drain-source voltage rating of the MOSFET is reduced (details can be seen in the datasheet of the corresponding product).

Furthermore, at extreme cold start-up scenarios (-40°C) and worst-case conditions, the 950 V CoolMOS™ P7 is still able to block around 880 V. Therefore to design and keep at least 50 to 100 V margin increases the overall system reliability.

7.3 Surge waveforms

In order for the power supply to be robust enough for abnormal line conditions such as lightning strikes or failures of other electronics on the line, it needs to survive surge testing.

The 12 W power supply was tested to 2 kV using the EN 61000-4-5 combination wave surge standard conditions with a 90-degree phase and positive polarity from line to neutral, which is the worst-case condition for the MOSFET. Under these conditions the MOSFET still had 100 V of margin under worst-case conditions when using 230 V AC_{in} single-phase.



Ch1 (yellow): Voltage across the bulk capacitor (V_{bulk})
Ch2 (red): Voltage across the sense resistor (R_{sense} 1.8 Ω)
Ch3 (blue): MOSFET drain-source voltage (V_{DS})

Figure 20 IEC61000 2 kV surge test was performed on the adapter while operating under full load (12 W)

The highest voltage measured across the MOSFET (Q2) was ~850 V. The surge event can be seen when the V_{bulk} (Ch2) rapidly rises. The bus capacitor (Ch1) and input line filter values are critical for determining the peak surge voltage.

Further tests higher than 2 kV at 230 V AC_{in} showed that the line filter input-side resistors R31, R32, R33 (red) start to arc to the case of the nearby filter inductors (L4, L6 or L7) shown in Figure 21, but the supply does not fail after this arcing event.

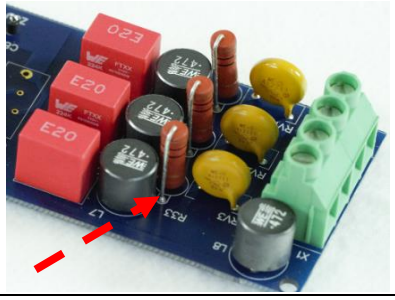


Figure 21 Possible arcing when applying surge pulses greater than 2 kV (L-N)

Protections, reliability and EMI

For moving to mass production this arcing could present a reliability issue, so heatshrink tubing should be used to cover the resistor body and leads, or the resistors should be moved away from the input inductors to give more clearance.

The board was tested up to 4 kV when the MOSFET failed due to avalanche and no output power was visible any more. It is not recommended to go higher than 2 kV with the existing design without adjusting the line input filter.

Several steps can increase the surge capability further; one would be a total new filter design according to the end customer needs where the size and the position of the Metal Oxide Varistor (MOV) are also changed, for example. As this would have a direct influence on the EMI behavior, a new design cycle would be required.

7.4 EMI test results (conducted and radiated)

Based on the detector used in the spectrum analyzer, average, QP or peak measurements can be obtained. Peak detection will always give the highest reading, followed by QP and then average readings. Therefore, to perform EMI scans quickly most engineers prefer peak detection and then compare the results against QP limits.

Meeting conducted emission specifications does not necessarily confirm that the radiated emission specification would be met. Nevertheless there are several factors influencing the EMI system behavior.

In this section of the application note, conducted and radiated EMI results are shown. It is clear that this board is intended for evaluation purposes. There is no special focus on EMI performance or separate investigations; the main goal is the evaluation of the new 950 V CoolMOS™ P7 used in an auxiliary power supply for smart meters and home appliances.

7.4.1 Conducted EMI

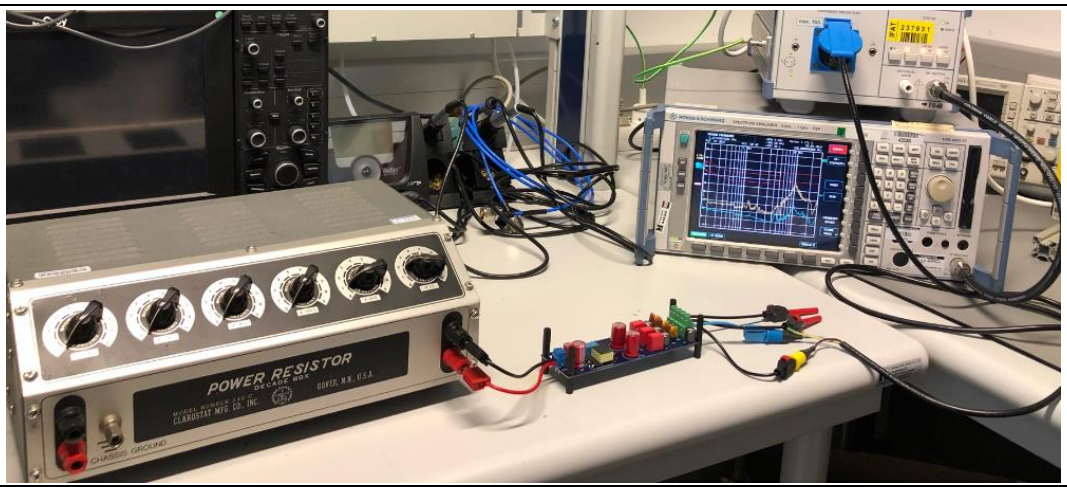


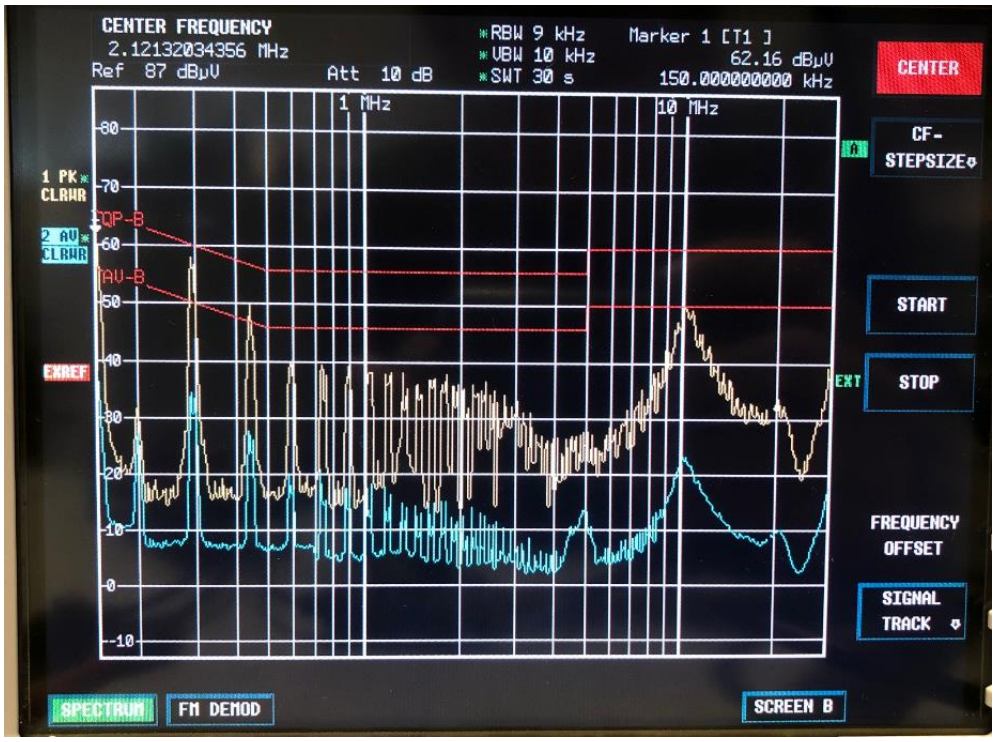
Figure 22 Conducted EMI test set-up

All EMI tests were conducted in an Infineon Technologies Austria AG application laboratory using the set-up shown in Figure 22Figure 22.

The following equipment was used for the conducted EMI test:

- Chroma 6530 AC source
- DUT (12 W SMPS) with IPD95R1K2P7
- Clarostat 240C Decade Power Resistor Box
- Rohde & Schwarz Spectrum Analyzer FSP 9 kHz to 7 GHz

- Rohde & Schwarz ENV216 Two-line v-network
- Measurements under full-load condition (single-phase 230 V AC_{in}, 12 W, resistive load with 12 Ω)



Ch1 (yellow): QP spectrum
Ch2 (blue): Average spectrum

Figure 23 The 12 W demo board EMI test results show passing conducted EMI through most of the band with low margin at the first harmonic (EN 55022 class B)

It can be seen in Figure 23 that a slightly higher filter impedance is needed for additional margin at the first and second harmonics of the switching frequency.

EMI is a system-level topic, and the optimization needs to be done at system level only. As shown in Figure 23 the IPD95R1K2P7 passed the conducted EMI with standard EN 55022 class B with some small margin (3 dB) less than 1 MHz from the QP and around 10 dB of margin in the range from 1 to 30 MHz.

7.4.2 Radiated EMI

To give the full performance picture of the SMPS, the radiated EMI tests were performed with an external certified partner of Infineon Technologies Austria AG, the EMI Laboratory FH Kaernten in Villach (Figure 24).

These tests were performed on one single board, with one MOSFET out of running production. Every component on the board has its own tolerances, and because the board was intended as a pure evaluation board for the 950 V CoolMOS™ P7, these results only give an approximate estimation of the frequency range a mass-market optimization could achieve.

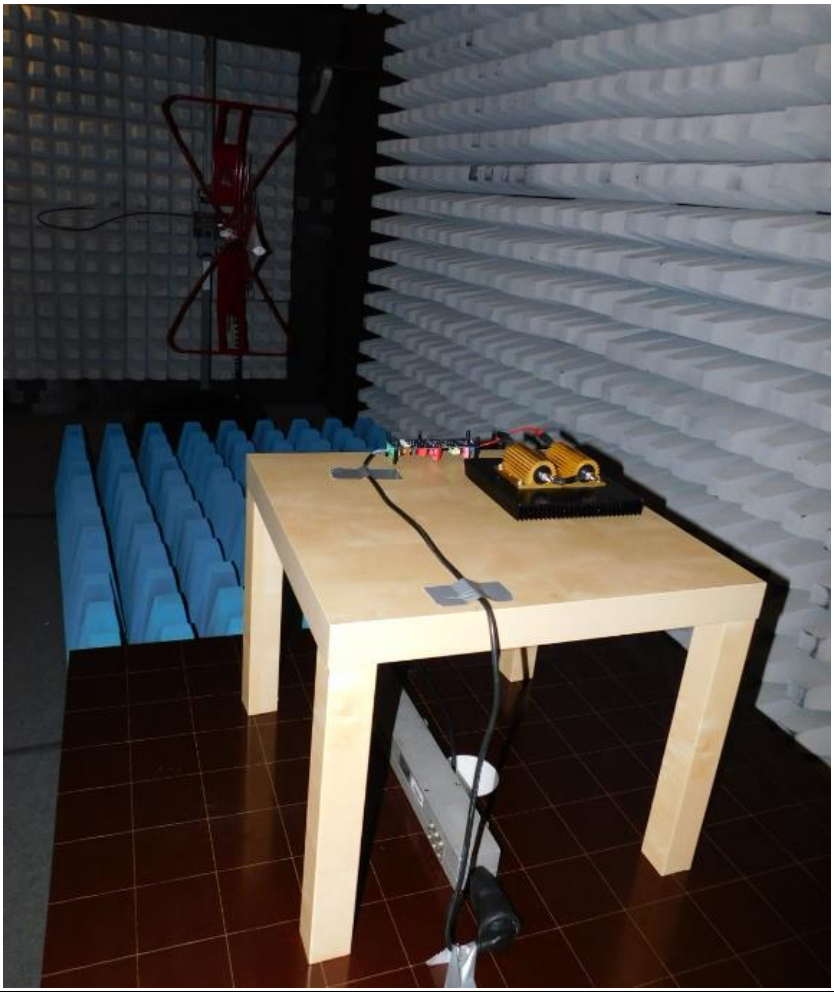
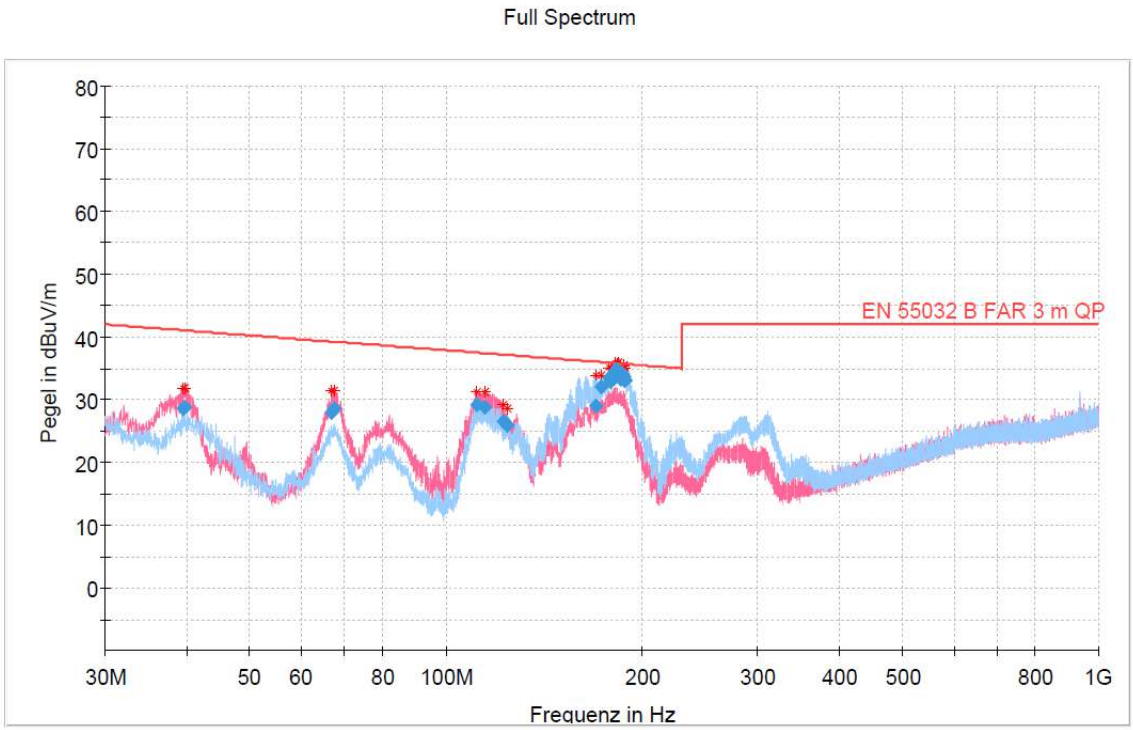


Figure 24 Radiated EMI test set-up (EMI Laboratory FH Kaernten, Villach)

In Figure 24 the test set-up including the device under test, placed on a table with 3 m of distance to the antenna, can be seen. The big yellow resistors acted as reliable loads in terms of low temperature drift and stable power consumption.



Final_Result

Frequenz (MHz)	Quasi Peak (dBuV/m)	Limit (dBuV/m)	Margin (dB)	Messzeit (ms)	Bandbreite (kHz)	Höhe (cm)	Pol	Azimut (deg)	Korr. (dB/m)
39.440000	28.61	41.06	12.45	1000.0	120.000	140.0	V	46.0	17.8
39.640000	28.86	41.04	12.19	1000.0	120.000	140.0	V	46.0	17.7
66.560000	27.98	39.26	11.28	1000.0	120.000	140.0	V	138.0	13.8
67.400000	28.49	39.22	10.73	1000.0	120.000	140.0	V	138.0	13.8
111.600000	29.19	37.49	8.30	1000.0	120.000	140.0	V	138.0	8.2
114.640000	28.69	37.39	8.70	1000.0	120.000	140.0	V	138.0	8.2
122.040000	26.43	37.18	10.75	1000.0	120.000	140.0	V	184.0	8.2
124.160000	25.97	37.12	11.15	1000.0	120.000	140.0	V	138.0	8.3
169.880000	28.88	36.04	7.16	1000.0	120.000	140.0	H	276.0	9.9
173.200000	32.06	35.98	3.91	1000.0	120.000	140.0	H	276.0	9.9
178.120000	33.54	35.88	2.33	1000.0	120.000	140.0	H	276.0	10.0
178.520000	32.80	35.87	3.07	1000.0	120.000	140.0	H	276.0	10.0
181.120000	34.38	35.82	1.44	1000.0	120.000	140.0	H	276.0	10.0
181.360000	33.92	35.82	1.90	1000.0	120.000	140.0	H	276.0	10.0
181.760000	34.15	35.81	1.66	1000.0	120.000	140.0	H	276.0	10.0
181.880000	34.67	35.81	1.14	1000.0	120.000	140.0	H	276.0	10.0
182.160000	34.68	35.80	1.12	1000.0	120.000	140.0	H	276.0	10.0
182.560000	34.60	35.79	1.19	1000.0	120.000	140.0	H	276.0	10.0
182.960000	34.61	35.79	1.18	1000.0	120.000	140.0	H	276.0	10.0
183.360000	34.42	35.78	1.36	1000.0	120.000	140.0	H	276.0	10.0
183.760000	34.24	35.77	1.53	1000.0	120.000	140.0	H	276.0	10.0
184.160000	33.97	35.76	1.79	1000.0	120.000	140.0	H	276.0	10.0
184.720000	34.00	35.75	1.75	1000.0	120.000	140.0	H	276.0	10.0
185.520000	33.22	35.74	2.52	1000.0	120.000	140.0	H	276.0	10.0
185.640000	34.18	35.74	1.56	1000.0	120.000	140.0	H	276.0	10.0
186.320000	34.08	35.72	1.65	1000.0	120.000	140.0	H	276.0	10.0
186.440000	33.97	35.72	1.75	1000.0	120.000	140.0	H	276.0	10.0
186.720000	33.71	35.72	2.00	1000.0	120.000	140.0	H	276.0	10.0
187.120000	33.29	35.71	2.42	1000.0	120.000	140.0	H	276.0	10.0
187.880000	33.01	35.70	2.69	1000.0	120.000	140.0	H	276.0	10.0

Figure 25 The 12 W demo board EMI test results show successful passing radiated EMI test (Norm EN 55032 B)

As an option for EMI optimization a separation from the turn-on and turn-off of the resistor can be implemented. At the moment there is only one external resistor (R_g) placed in front of the MOSFET influencing the MOSFET switching behavior. Instead of a single resistor, a resistor for turning on the MOSET and a diode for a fast turn-off can be designed.

8 Performance comparison results

The 12 W demo board efficiency and thermal results are as shown in the following chapter. As the board can be used from 185 V AC_{in} up to 465 V AC_{in}, several tests were performed.

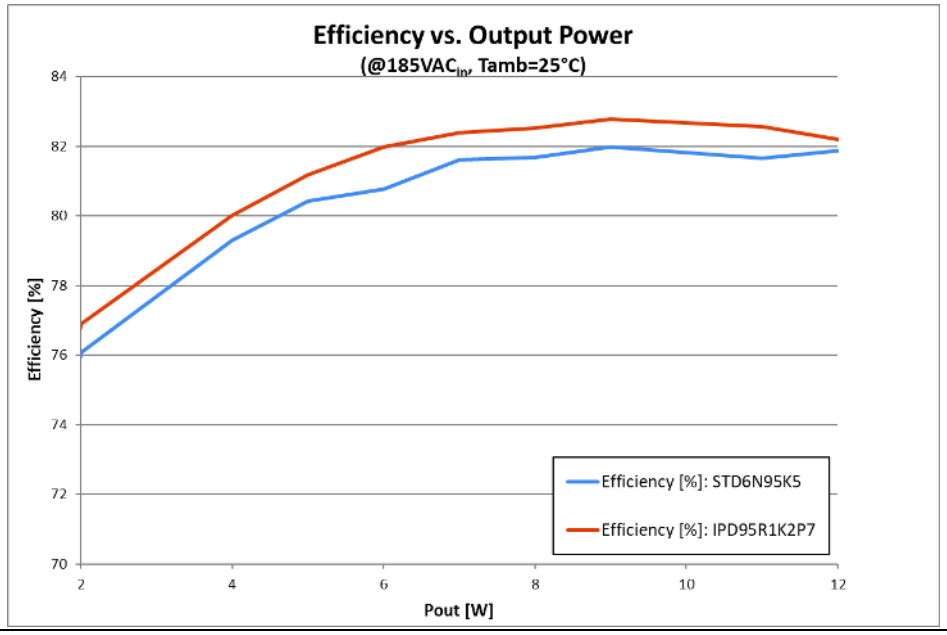
For a competitor part the STD6N95K5 from STMicroelectronics was chosen, as the closest reference part to Infineon's IPD95R1K2P7. To make the performance more visible, the lowest possible voltage (185 V AC_{in} – single-phase) and the highest voltage (465 V AC_{in} – three-phase) are shown in the following graphs.

$R_{DS(on)}$ characterization of parts used:

- IPD95R1K2P7 ~980 mΩ
- STD6N95K5 ~900 mΩ

All characterization was done with Infineon datasheet condition of IPD95R1K2P7 – V_{GS} = 10 V; I_D = 2.7 A; T_j = 25°C

8.1 Efficiency and thermals (185 V AC_{in} – single-phase input)



Performance comparison results

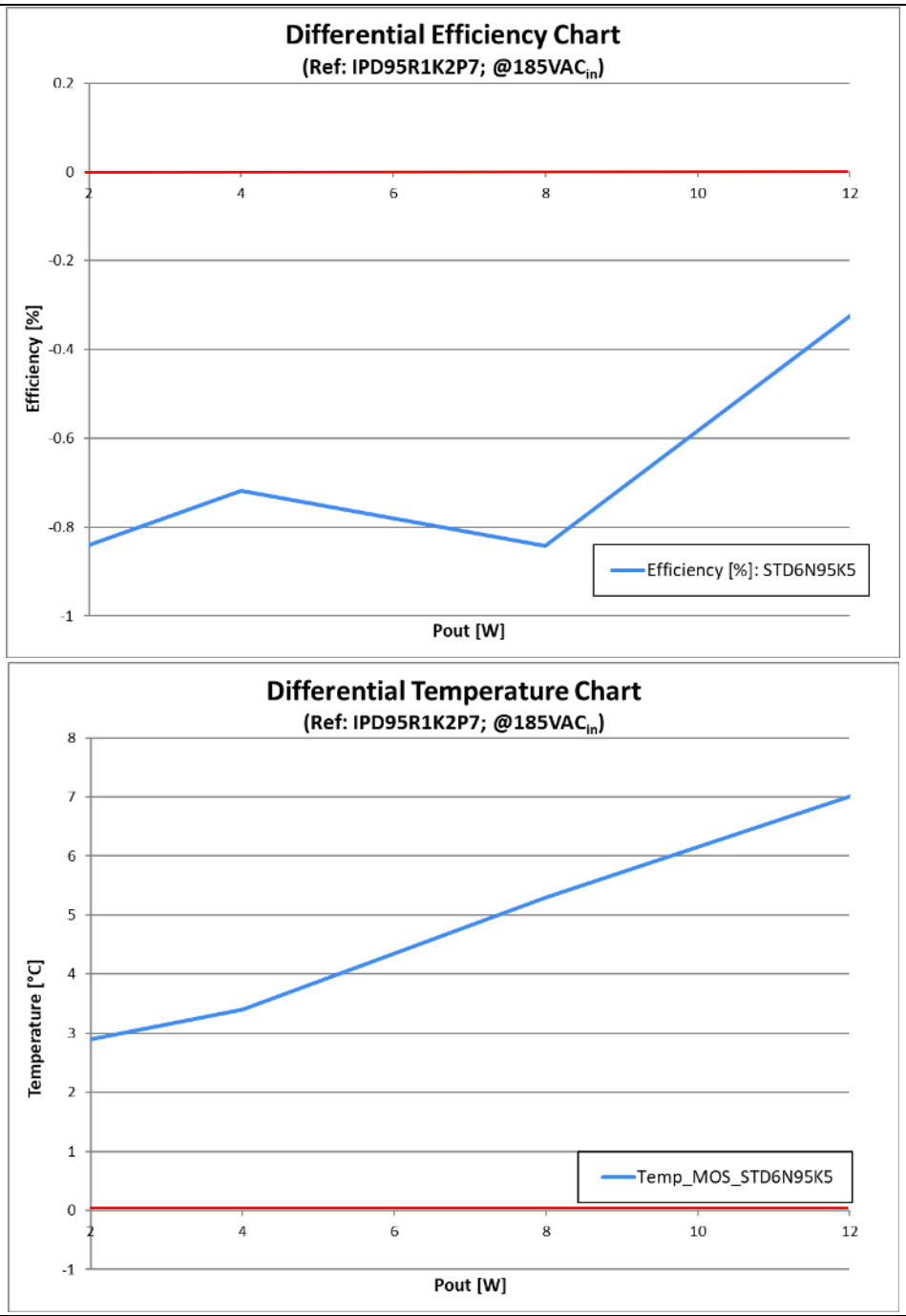


Figure 26 Efficiency comparison/differential chart/thermals (DPAK – IPD95R1K2P7 vs. STD6N95K5)

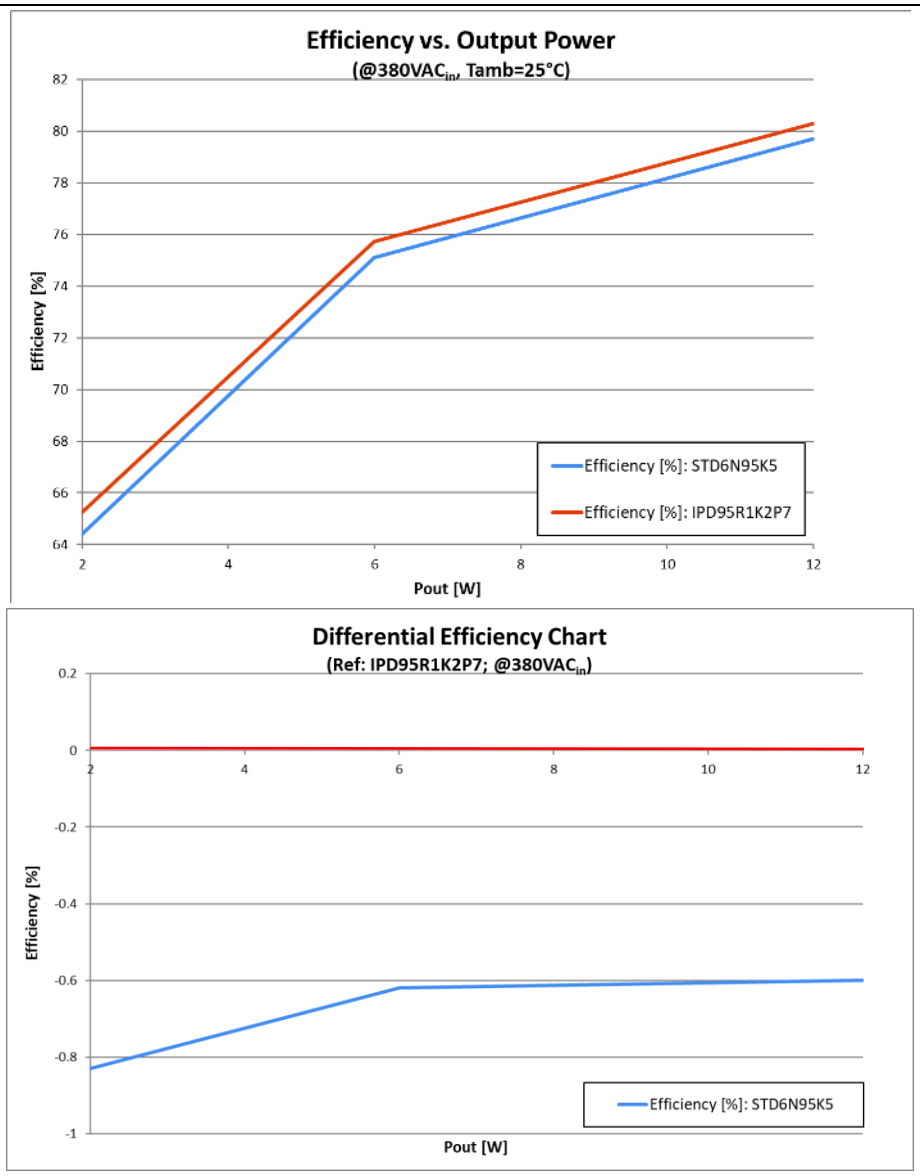
As can be seen in the efficiency over output power chart, the new 950 V CoolMOS™ P7 out-performs the competitor part over the entire load range. An optimized gate charge combined with reduced output capacitance of the MOSFET itself gives not only an efficiency advantage at the lowest power level, but also at the most critical full-load point. This is visible on the second graph, the differential efficiency chart.

Furthermore, all improvements in terms of driving and switching, combined with an optimization of conduction losses, leads to a lower MOSFET temperature of around 7°C at the lowest input voltage at the higher load point (12 W). Another advantage of the P7 series is the $R_{DS(on)}$ over-temperature behavior, where at working condition and higher temperature, the P7 MOSFET $R_{DS(on)}$ stays lower compared to the competitor part.

Performance comparison results

Overall the new switch gives the designer more design flexibility: more thermal margin when making a plug-and-play change in an existing design, and also an increase of efficieny in the range of 0.2 percent up to 0.8 percent in this dedicated design.

8.2 Efficiency and thermals (380 V AC_{in} – three-phase input)



Performance comparison results

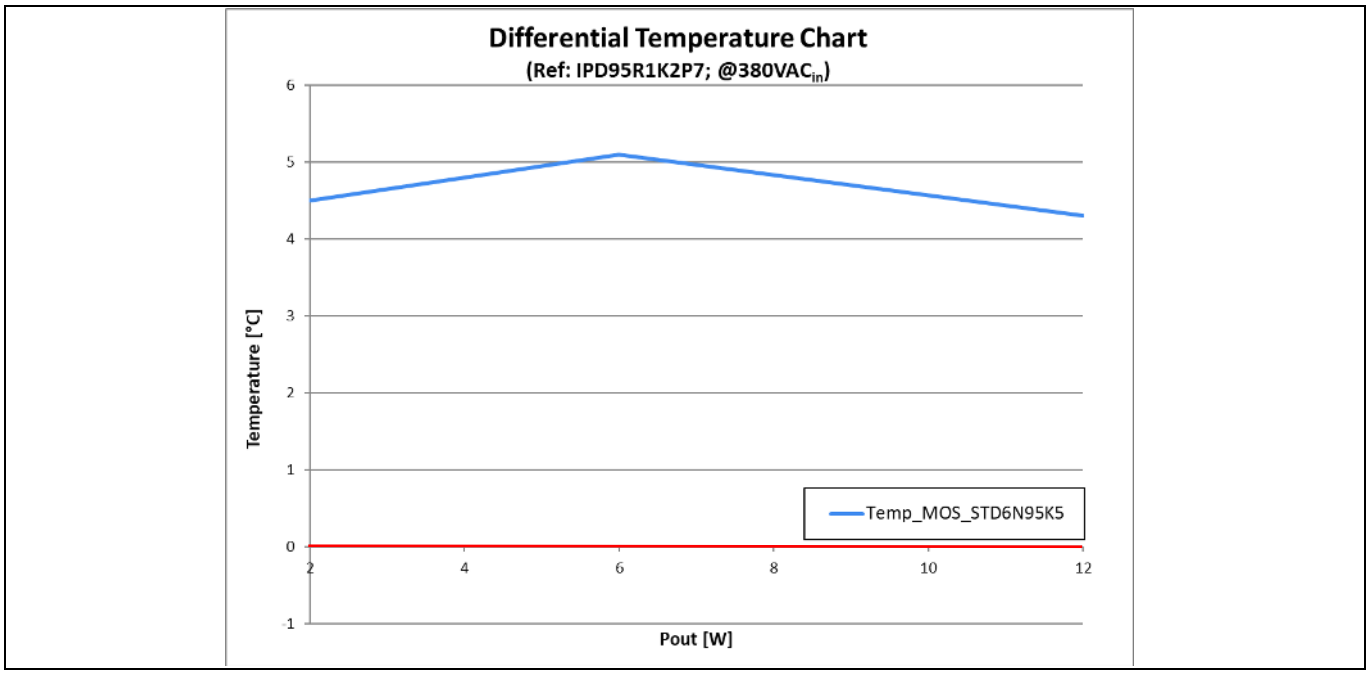


Figure 27 Efficiency comparison/differential chart/thermals (DPAK – IPD95R1K2P7 vs. STD6N95K5)

To get a feeling for the system performance at a different input voltage level, in addition 380 V AC as input voltage was used to repeat the tests.

As can be seen in Figure 27 the 950 V CoolMOS™ P7 can outperform the competitor part in the range of 0.6 percent in efficiency over the whole load range, resulting in a 4 to 5°C lower MOSFET temperature in the system.

9 Thermal performance

The table below shows the thermal performance of the IC and power MOSFET after running for ~30 minutes without an enclosure in a 25°C ambient temperature (two different conditions shown below; single- and three-phase AC). The IPD95R1K2P7 was considered as a reference device. The ambient temperature was stabilized to 25°C (+/-1°C of tolerance).

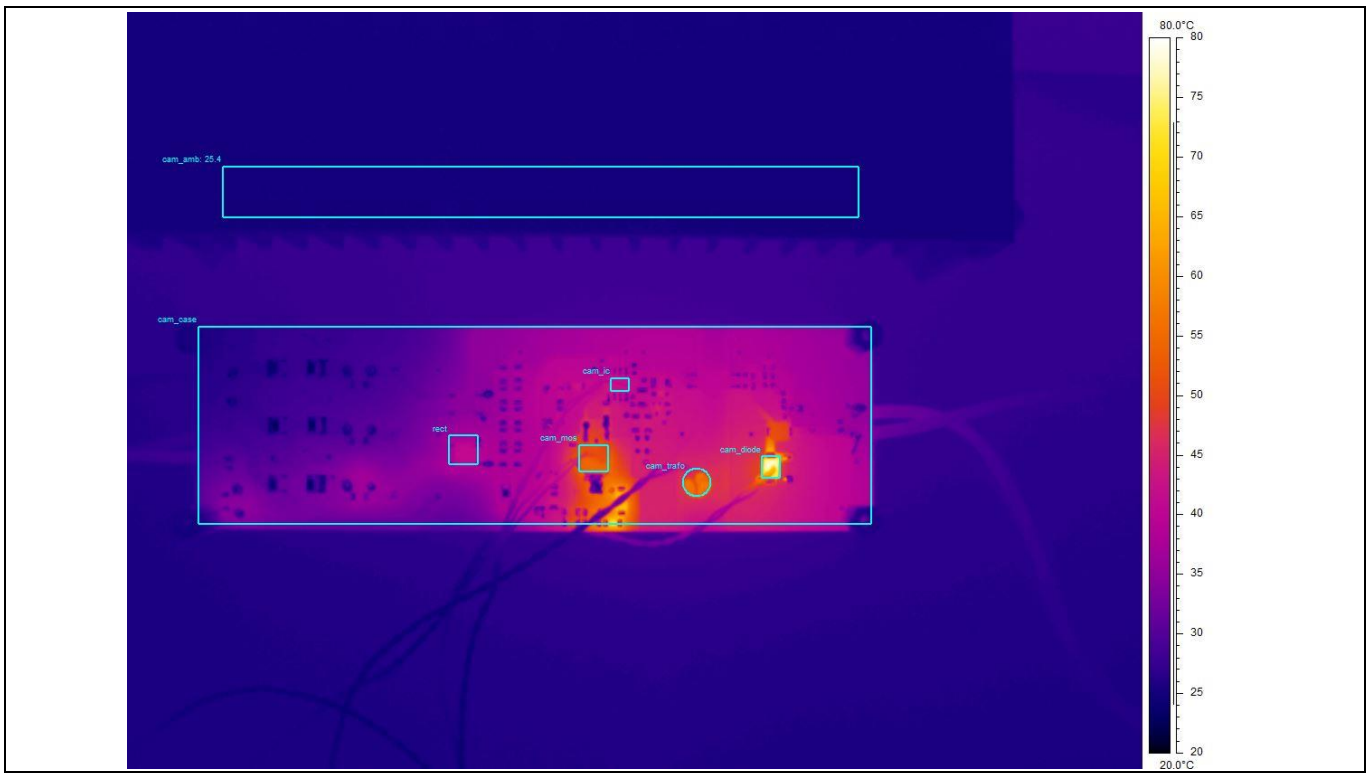


Figure 28 Thermal image (example view from board bottom 185 V AC_{IN}, P_{OUT} 12 W)

Condition A: single-phase input voltage = 185 to 265 V AC_{IN}, P_{OUT} = 12 W (12 V/1 A)

Thermal performance at 12 V output voltage (full load, electronic load, 30-minute warm-up, FLIR thermal camera)

Input voltage	185 V AC	230 V AC	265 V AC
Q2 (MOSFET)	59.6°C	60°C	63°C
U4 (IC)	45.6°C	44.7°C	45.4°C
T1 (Trafo)	57.2°C	58.2°C	60.3°C
D8 (output diode)	74.2°C	75°C	74°C
Ambient temp.	25°C	25°C	25°C

Thermal performance

Condition B: three-phase input voltage = 380 to 465 V AC_{IN}, P_{OUT} = 12 W (12 V/1 A)

Thermal performance at 12 V output voltage (full load, resistive load 12 Ω, 30-minute warm-up, thermocouples)

Input voltage	380 V AC	465 V AC
Q2 (MOSFET)	73.3°C	81°C
U4 (IC)	45.5°C	48.9°C
T1 (Trafo)	58.9°C	60°C
D8 (output diode)	75.8°C	75°C
Ambient temp.	25°C	25°C

10 Portfolio

950 V CoolMOS™ P7 shows a finely graduated portfolio with respect to $R_{DS(on)}$ classes and offers the most relevant packages for low-power applications.

All main applications are Flyback-based low-power applications including smart meters, lighting and auxiliary power supply in home appliances.

All products listed in Figure 29 are tested to industrial-grade standards enabling high performance and reliability and long lifetimes.

Portfolio 950 V P7 SJ MOSFET

Industrial Grade

ESD Class (HBM)	RDS(ON) [mΩ]	TO220FP	IPAK LL	DPAK	SOT223
1C	3700		IPU95R3K7P7		IPN95R3K7P7
2	2000		IPU95R2K0P7	IPD95R2K0P7	IPN95R2K0P7
	1200	IPA95R1K2P7	IPU95R1K2P7	IPD95R1K2P7	IPN95R1K2P7
	750	IPA95R750P7	IPU95R750P7	IPD95R750P7	
	450	IPA95R450P7	IPU95R450P7	IPD95R450P7	

Figure 29 950 V CoolMOS™ P7 portfolio

11 Further cost-lowering potential by using SOT-223

As it was shown already in the portfolio, the 950 V CoolMOS™ P7 comes along with the new cost-optimized package SOT-223. This means a further cost-lowering potential is enabled plus the gain of extra creepage distance (4 mm between gate and source pins) on board and package level when designed according to the SOT-223 footprint (see datasheet IPN95R1K2P7).

Furthermore and without any layout changes the SOT-223 package can be a direct pin-to-pin replacement for a DPAK package with the outer dimensions and lead spacing shown in Figure 30.

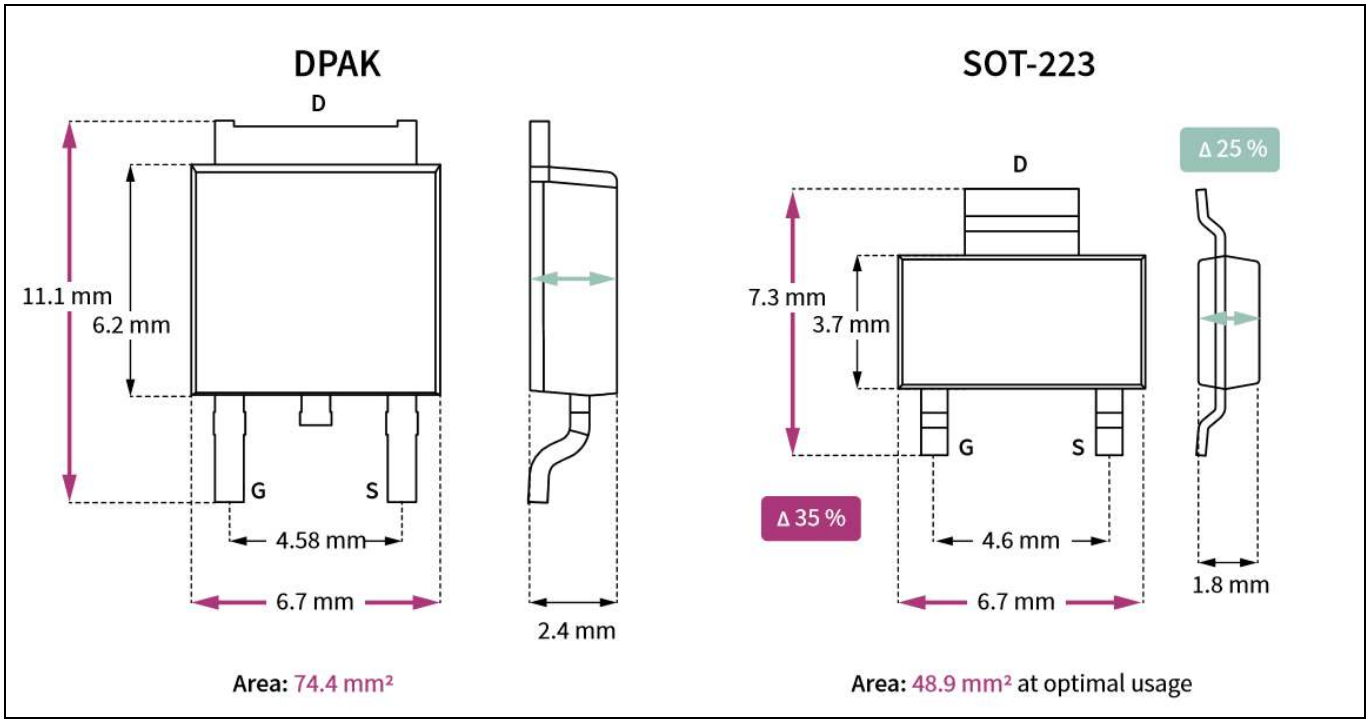


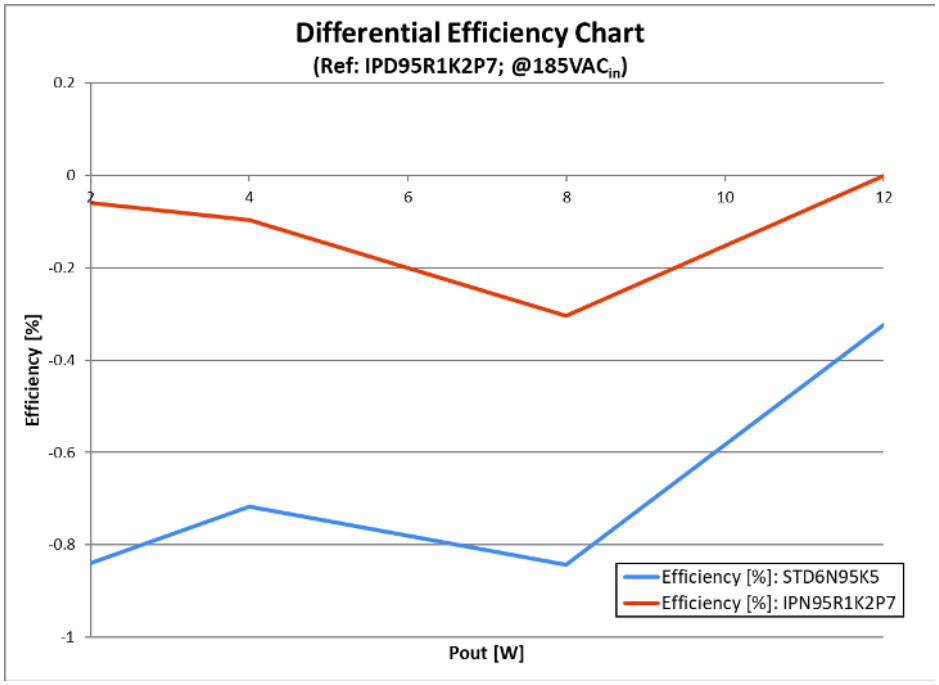
Figure 30 Package comparison DPAK vs. SOT-223

It can be seen that the middle pin of a standard SOT-223 is removed, which allows the inclusion of 950 V MOSFETs. This version of SOT-223 is even safer with respect to soldering processes (reflow or especially wave) as there is less possibility for solder residues between the leads (as middle pin of DPAK package is connected to drain potential). Additionally, the optical solder inspection after the soldering process, allows a greater visibility compared to the DPAK package.

The biggest challenge with SOT-223 is the thermal behavior. There is a detailed application note available that discusses the thermal trade-offs between DPAK and SOT-223, assisting in the quick implementation of this new package in low-power designs.

To prove this statement an efficiency and thermal comparison was done for the 12 W auxiliary power supply. Changing from a 1.2 Ω DPAK to a 1.2 Ω SOT-222 is described in the figures below.

Further cost-lowering potential by using SOT-223



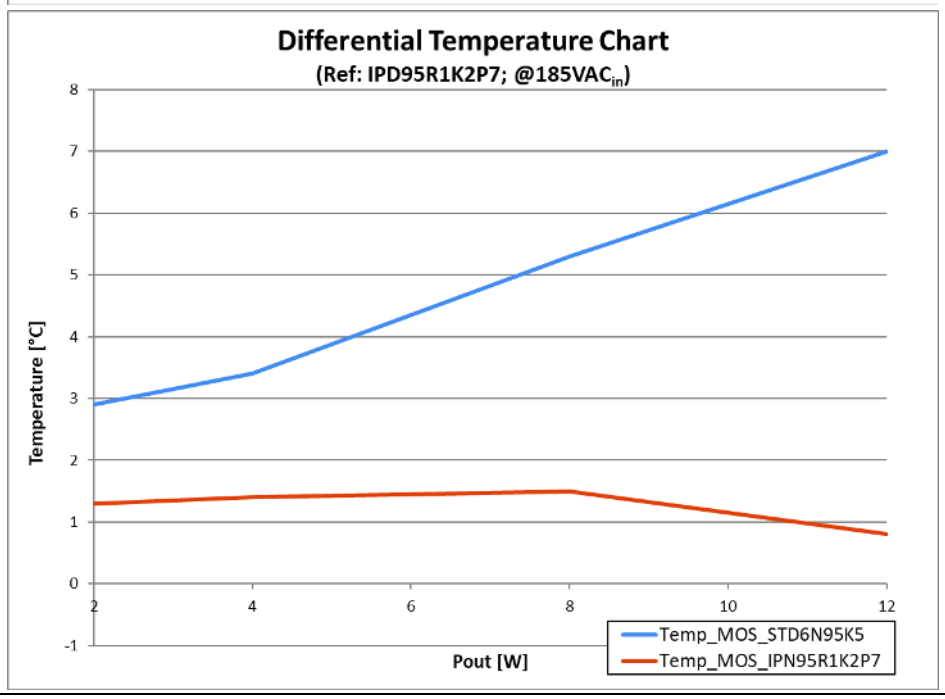


Figure 31 Efficiency and thermal comparison (transfer from DPAK to SOT-223 IPN95R1K2P7)

In Figure 31Figure 31 it can be seen that the efficiency (reference part IPD95R1K2P7) stays at nearly the same efficiency level when making the switch to the SOT-223 package, even though the package is smaller and thinner. Since the copper area around the drain pin was designed with extra margin already, no major disadvantage in the overall system efficiency is visible. As a general recommendation 20 mm^2 of copper should be added on for SOT-223 when replacing DPAK with the same $R_{DS(on)}$. Finally, it can be seen in the lower graph in Figure 31 that the temperature is slightly higher compared to the DPAK, but still stays within +2°C.

With the cost-optimized SOT-223 package, the BOM cost can be reduced while not sacrificing performance, reliability or thermal stability.

12 Conclusion

This board effectively shows the performance of the new 950 V CoolMOS™ P7 in combination with the QR Flyback controller ICE5QSAG as auxiliary power supply in smart meters and home appliances.

Good efficiency and EMI performance along with PCB area savings and package height reductions give extra value, especially for smart meter customers who have increased power density requirements.

The additional improvement in switching performance helps for HV low power applications, and the additional headroom when using a 950 V device helps in designing a system that is robust enough for HV inputs and harsh environments.

These benefits for smart meter and home appliance auxiliary power supply applications make 950 V CoolMOS™ P7 an ideal fit for low-cost low-power applications.

The most cost-competitive SOT-223 package from Infineon is a further lever for lowring system cost, and opens the possibility of increased power density designs.

13 References

[1] 950 V CoolMOS™ P7 Datasheet

[2] The benefits of SOT-223 CoolMOS™ CE device

[3] CoolMOS™ in SOT-223

[4] ICE5QSAG QR Flyback Controller Datasheet

[5] Optimizing EMI in Flyback power supplies using external MOSFETs

[6] Calculation Tool Quasi-Resonant CoolSET™ Generation 5

Revision history

Major changes since the last revision

Page or reference	Description of change
v1.0	Release of final application note

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