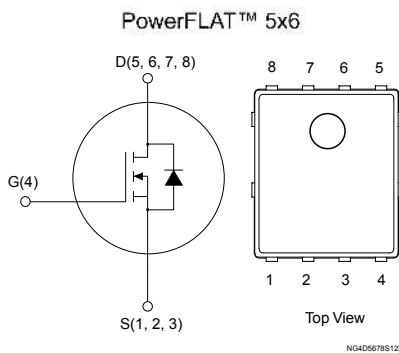
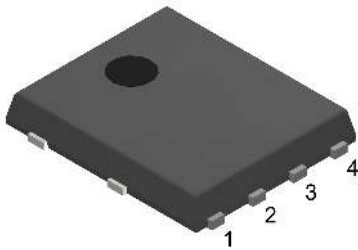


N-channel 40 V, 0.9 mΩ typ., 120 A, STripFET F7 Power MOSFET in a PowerFLAT 5x6 package



Features

Type	V _{DS}	R _{DS(on)} max.	I _D
STL260N4F7	40 V	1.1 mΩ	120 A

- Among the lowest R_{DS(on)} on the market
- Excellent FoM (figure of merit)
- Low C_{rss}/C_{iss} ratio for EMI immunity
- High avalanche ruggedness

Applications

- Switching applications

Description

This N-channel Power MOSFET utilizes STripFET F7 technology with an enhanced trench gate structure that results in very low on-state resistance, while also reducing internal capacitance and gate charge for faster and more efficient switching.



Product status link

[STL260N4F7](#)

Product summary

Order code	STL260N4F7
Marking	260N4F7
Package	PowerFLAT™ 5x6
Packing	Tape and reel

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	40	V
V_{GS}	Gate-source voltage	± 20	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	120	A
	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	120	A
$I_{DM}^{(1)(2)}$	Drain current (pulsed)	480	A
$I_D^{(3)}$	Drain current (continuous) at $T_{pcb} = 25\text{ }^\circ\text{C}$	50	A
	Drain current (continuous) at $T_{pcb} = 100\text{ }^\circ\text{C}$	35	A
$I_{DM}^{(2)(3)}$	Drain current (pulsed)	200	A
$P_{TOT}^{(1)}$	Total power dissipation at $T_C = 25\text{ }^\circ\text{C}$	188	W
$P_{TOT}^{(3)}$	Total power dissipation at $T_{pcb} = 25\text{ }^\circ\text{C}$	4.8	W
T_{stg}	Storage temperature range	-55 to 175	$^\circ\text{C}$
T_j	Operating junction temperature range		

1. This value is rated according to $R_{thj-case}$ and limited by package.
2. Pulse width limited by safe operating area.
3. This value is rated according to $R_{thj-pcb}$.

Table 2. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	0.8	$^\circ\text{C/W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	31.3	$^\circ\text{C/W}$

1. When mounted on FR-4 board of 1 inch², 2 oz Cu, $t < 10\text{ s}$.

2 Electrical characteristics

($T_C = 25\text{ }^\circ\text{C}$ unless otherwise specified)

Table 3. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$, $I_D = 250\text{ }\mu\text{A}$	40			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$, $V_{DS} = 40\text{ V}$			1	μA
I_{GSS}	Gate-body leakage current	$V_{DS} = 0\text{ V}$, $V_{GS} = 20\text{ V}$			100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	2		4	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 24\text{ A}$		0.9	1.1	m Ω

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 25\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$	-	5000	-	pF
C_{oss}	Output capacitance		-	1800	-	pF
C_{rss}	Reverse transfer capacitance		-	145	-	pF
Q_g	Total gate charge	$V_{DD} = 20\text{ V}$, $I_D = 48\text{ A}$,	-	72	-	nC
Q_{gs}	Gate-source charge	$V_{GS} = 0\text{ to }10\text{ V}$	-	28	-	nC
Q_{gd}	Gate-drain charge	(see Figure 13. Test circuit for gate charge behavior)	-	14	-	nC

Table 5. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 20\text{ V}$, $I_D = 48\text{ A}$,	-	27	-	ns
t_r	Rise time	$R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$	-	22	-	ns
$t_{d(off)}$	Turn-off delay time	(see Figure 12. Test circuit for resistive load switching times and Figure 17. Switching time waveform)	-	45	-	ns
t_f	Fall time		-	18	-	ns

Table 6. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{SD}^{(1)}$	Forward on voltage	$I_{SD} = 48\text{ A}$, $V_{GS} = 0$	-	-	1.2	V
t_{rr}	Reverse recovery time	$I_D = 48\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$	-	55		ns
Q_{rr}	Reverse recovery charge	$V_{DD} = 32\text{ V}$ (see Figure 14. Test circuit for inductive load switching and diode recovery times)	-	60		nC
I_{RRM}	Reverse recovery current		-	2.1		A

1. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

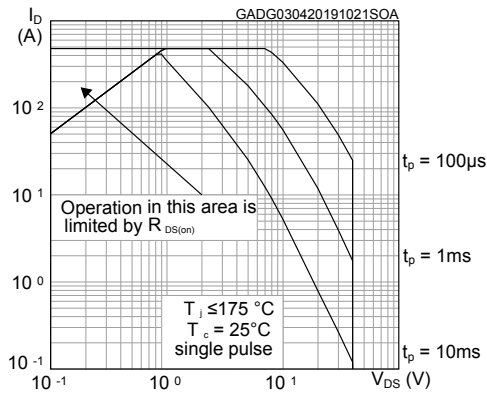


Figure 2. Thermal impedance

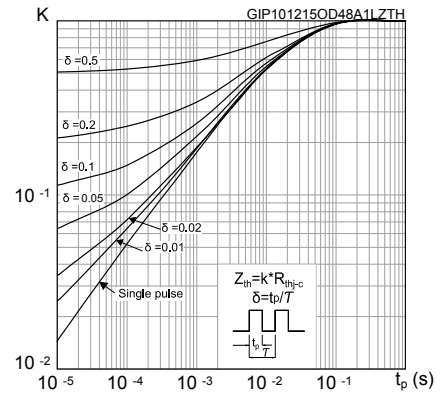


Figure 3. Output characteristics

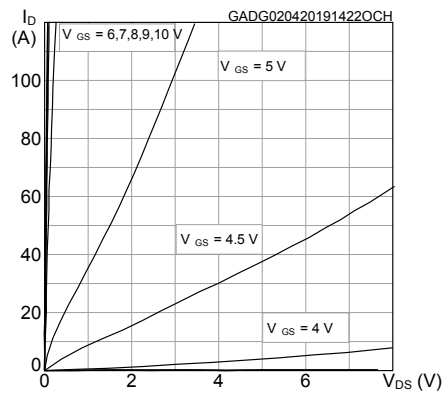


Figure 4. Transfer characteristics

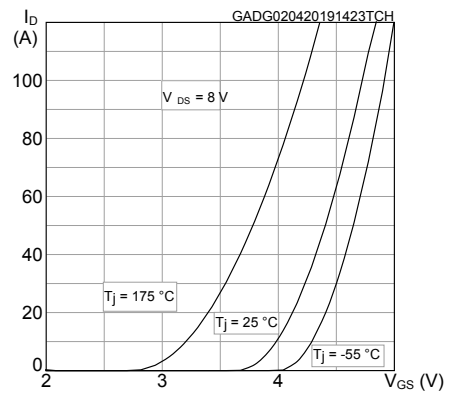


Figure 5. Gate charge vs gate-source voltage

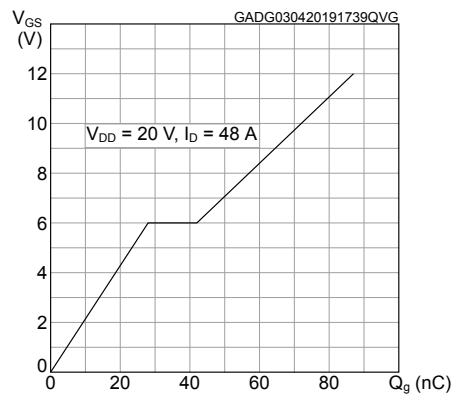


Figure 6. Static drain-source on-resistance

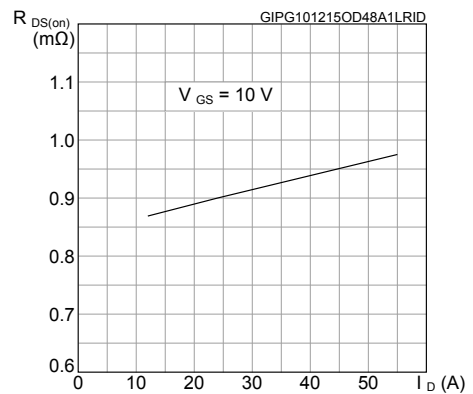


Figure 7. Capacitance variations

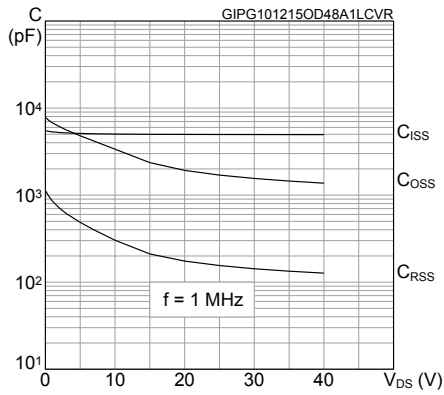


Figure 8. Normalized on-resistance vs temperature

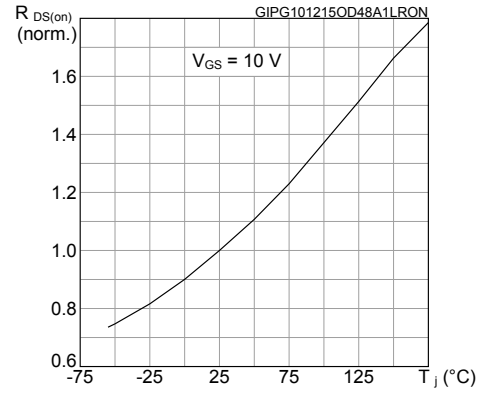


Figure 9. Normalized V_{(BR)DSS} vs temperature

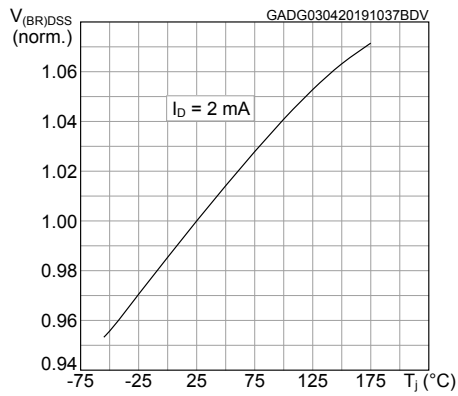


Figure 10. Normalized gate threshold voltage vs temperature

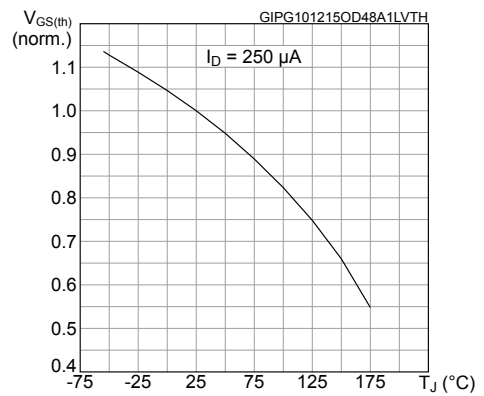
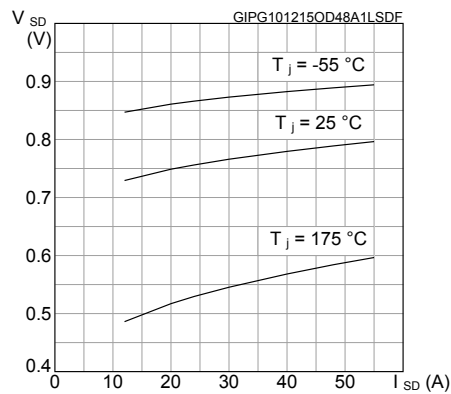
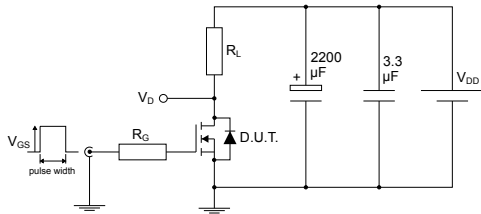


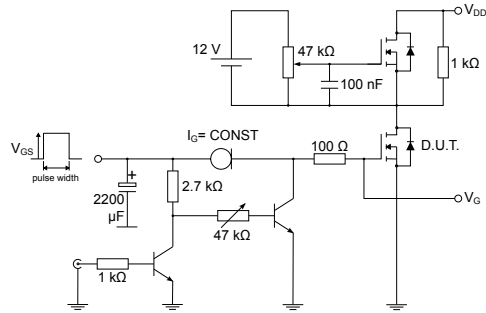
Figure 11. Source-drain diode forward characteristics



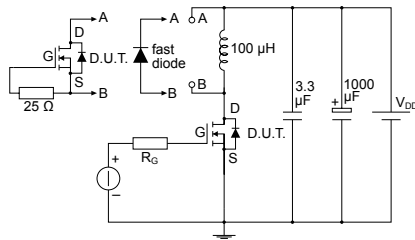
3 Test circuits

Figure 12. Test circuit for resistive load switching times


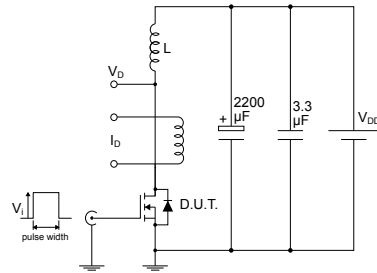
AM01468v1

Figure 13. Test circuit for gate charge behavior


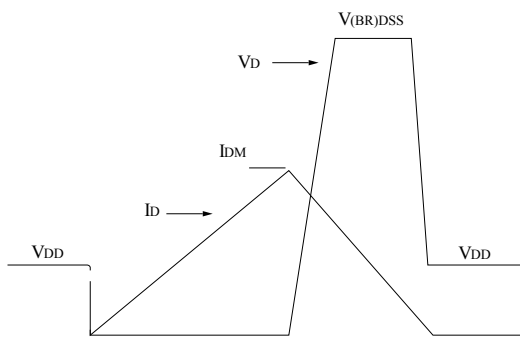
AM01469v1

Figure 14. Test circuit for inductive load switching and diode recovery times


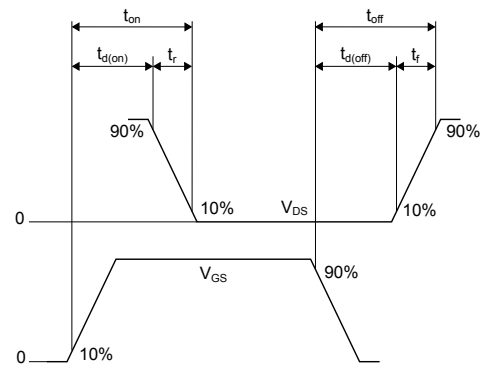
AM01470v1

Figure 15. Unclamped inductive load test circuit


AM01471v1

Figure 16. Unclamped inductive waveform


AM01472v1

Figure 17. Switching time waveform


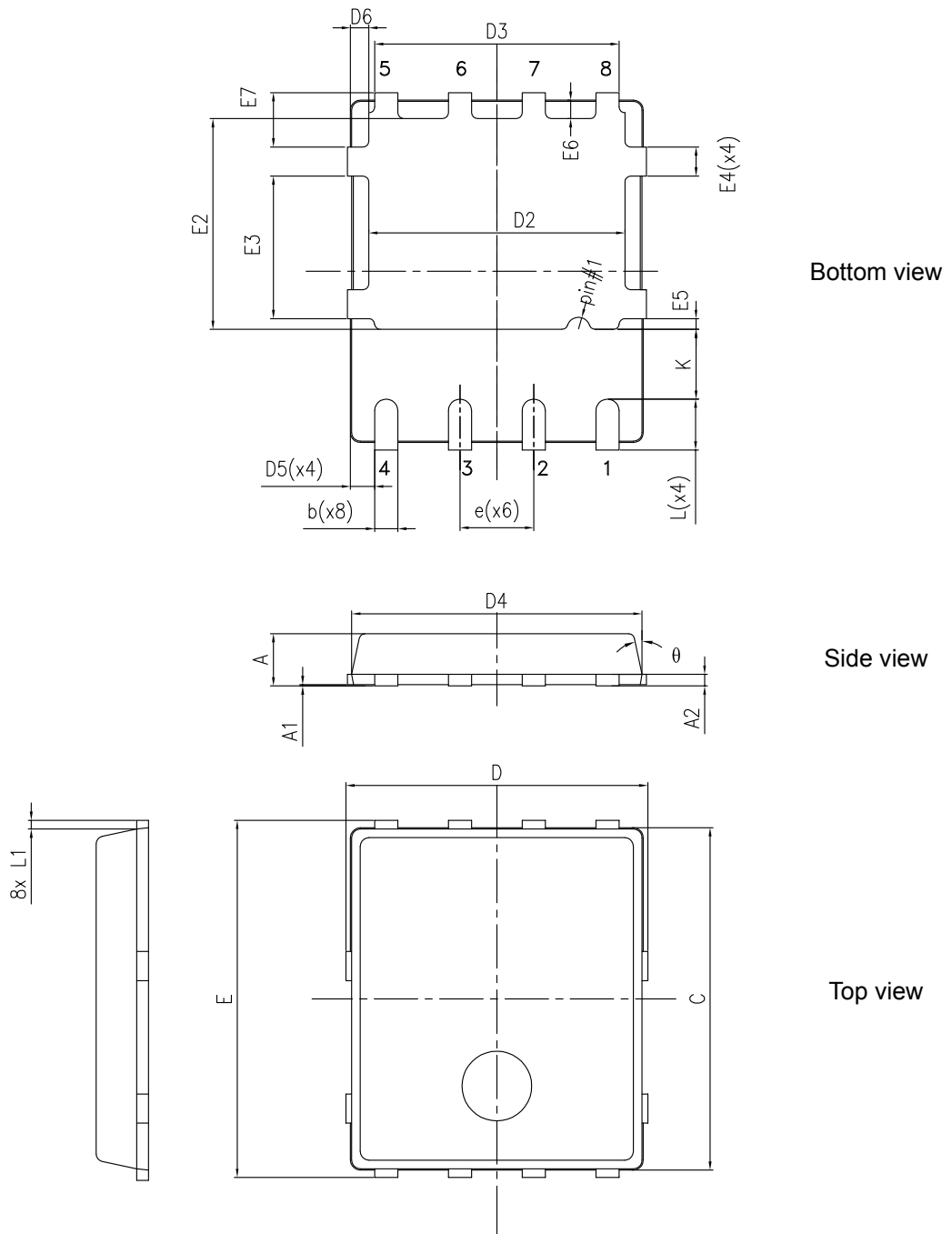
AM01473v1

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 PowerFLAT™ 5x6 type C package information

Figure 18. PowerFLAT™ 5x6 type C package outline

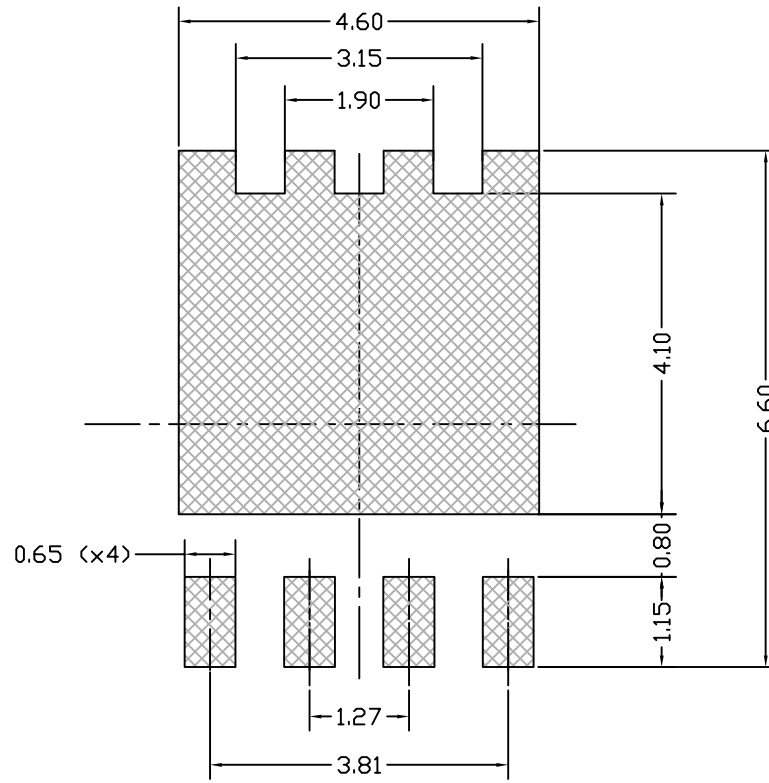


8231817_typeC_Rev18

Table 7. PowerFLAT™ 5x6 type C package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
C	5.80	6.00	6.20
D	5.00	5.20	5.40
D2	4.15		4.45
D3	4.05	4.20	4.35
D4	4.80	5.00	5.20
D5	0.25	0.40	0.55
D6	0.15	0.30	0.45
e		1.27	
E	5.95	6.15	6.35
E2	3.50		3.70
E3	2.35		2.55
E4	0.40		0.60
E5	0.08		0.28
E6	0.20	0.325	0.45
E7	0.75	0.90	1.05
K	1.05		1.35
L	0.725		1.025
L1	0.05	0.15	0.25
θ	0°		12°

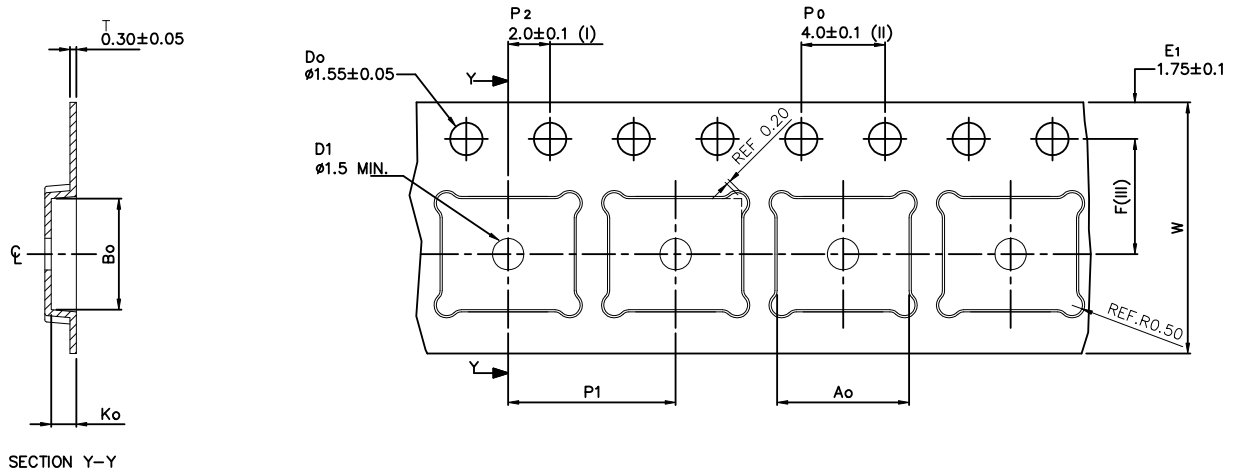
Figure 19. PowerFLAT™ 5x6 recommended footprint (dimensions are in mm)



8231817_FOOTPRINT_simp_Rev_18

4.2 PowerFLAT™ 5x6 packing information

Figure 20. PowerFLAT™ 5x6 tape (dimensions are in mm)



A ₀	6.30 +/− 0.1
B ₀	5.30 +/− 0.1
K ₀	1.20 +/− 0.1
F	5.50 +/− 0.1
P ₁	8.00 +/− 0.1
W	12.00 +/− 0.3

(I) Measured from centreline of sprocket hole to centreline of pocket.

(II) Cumulative tolerance of 10 sprocket holes is ± 0.20 .

(III) Measured from centreline of sprocket hole to centreline of pocket

Base and bulk quantity 3000 pcs
All dimensions are in millimeters

8234350_Tape_rev_C

Figure 21. PowerFLAT™ 5x6 package orientation in carrier tape

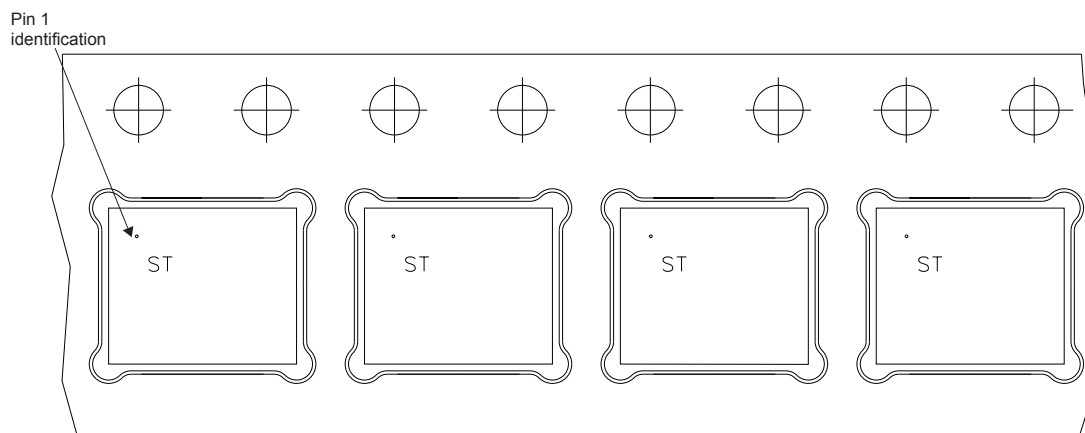
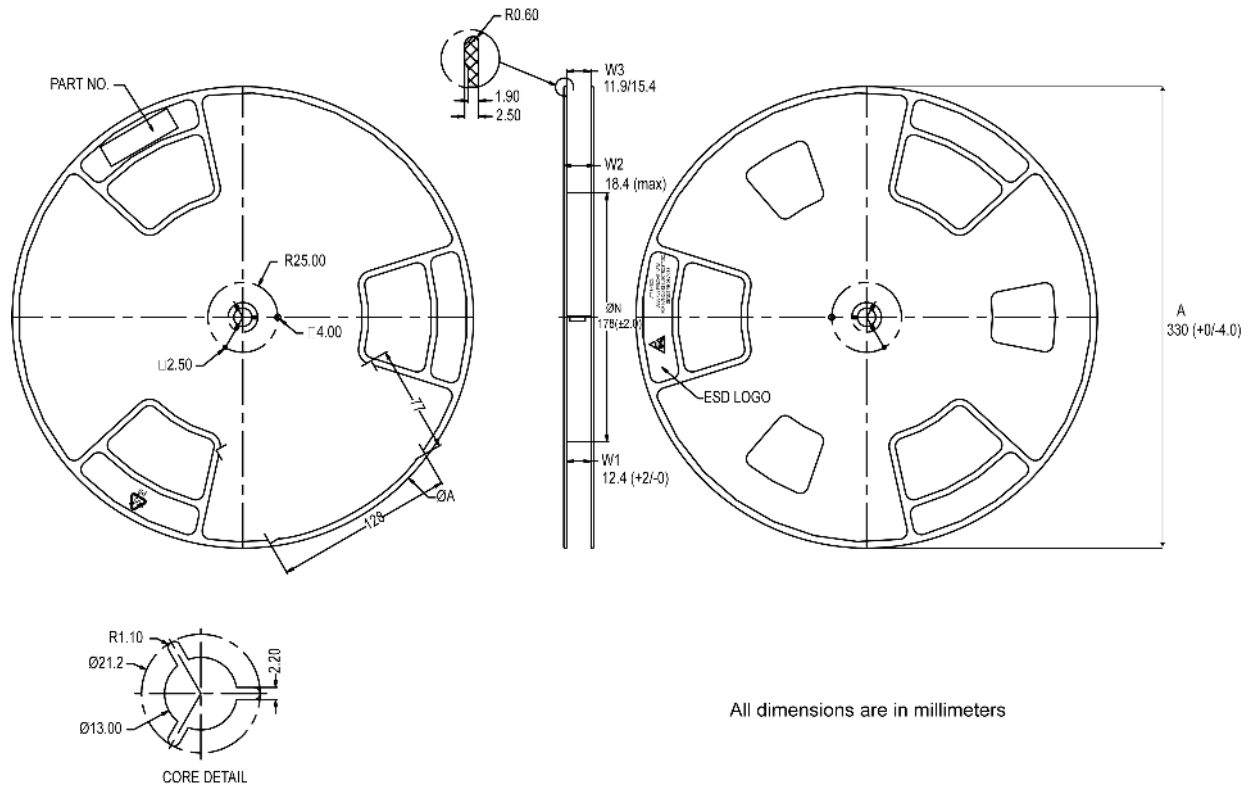


Figure 22. PowerFLAT™ 5x6 reel



8234350_Reel_rev_C

Revision history

Table 8. Document revision history

Date	Revision	Changes
10-Aug-2015	1	Initial release.
24-Sep-2015	2	Updated Title. Updated section <i>Electrical characteristics</i> . Minor text changes.
09-Jun-2016	3	Modified: title and features table in cover page Modified: <i>Table 2: "Absolute maximum ratings", Table 4: "On /off states", Table 5: "Dynamic", Table 6: "Switching times" and Table 7: "Source drain diode"</i> Minor text changes
21-Jan-2019	4	Modified Table 4. Dynamic , Table 5. Switching times and Table 6. Source-drain diode . Modified Figure 1. Safe operating area , Figure 2. Thermal impedance , Figure 4. Transfer characteristics , Figure 5. Gate charge vs gate-source voltage , Figure 7. Capacitance variations , Figure 9. Normalized $V_{(BR)DSS}$ vs temperature and Figure 10. Normalized gate threshold voltage vs temperature . Updated Section 4.1 PowerFLAT™ 5x6 type C package information . Minor text changes.
03-Apr-2019	5	Updated Table 4. Dynamic , Table 5. Switching times and Table 6. Source-drain diode . Updated Figure 1. Safe operating area , Figure 3. Output characteristics , Figure 4. Transfer characteristics , Figure 5. Gate charge vs gate-source voltage and Figure 9. Normalized $V_{(BR)DSS}$ vs temperature .

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