



ABSTRACT

The [TPS7H2221EVM](#) is the Evaluation Module (EVM) for the [TPS7H2221-SEP](#) load switch and provides a platform to electrically evaluate its features. This user's guide provides details about the EVM, including its configuration, schematics, and BOM. Test results that were collected using the EVM are also shown.

Table of Contents

1 Introduction	2
1.1 Default Board Configuration.....	2
1.2 Alternate Board Configurations.....	3
2 EVM Connectors and Test Points	4
3 Test Results	5
3.1 Parallel Configuration Results.....	5
4 Load Transient Circuitry	11
5 Board Layout	12
6 Schematic	15
6.1 Parallel Configuration Schematic.....	15
6.2 Single Configuration Schematic.....	16
7 Bill of Materials (BOM)	17
7.1 Parallel Configuration BOM.....	17
7.2 Single Configuration BOM.....	19
8 Revision History	20
9 Related Documentation	21

Trademarks

All trademarks are the property of their respective owners.

1 Introduction

The TPS7H2221-SEP device is a small, single channel load switch with controlled slew rate. The device contains an N-channel MOSFET that can operate over an input voltage range of 1.6 V to 5.5 V and can support a maximum continuous current of 1.25 A. The switch ON state is controlled by a digital input that is capable of interfacing directly with low-voltage control signals. When power is first applied, a Smart Pull Down is used to keep the ON pin from floating until system sequencing is complete. Once the pin is deliberately driven HIGH ($>V_{IH}$), the Smart Pull Down will be disconnected to prevent unnecessary power loss. The TPS7H2221-SEP load switch is also self-protected, meaning that it protects against short circuit events on the output of the device.

1.1 Default Board Configuration

The EVM is designed to be used across the entire input voltage and output current range of the TPS7H2221-SEP while providing flexibility to configure the device to operate under different conditions. By default, the EVM is configured for parallel-device operation, as summarized in [Table 1-1](#), but the board also allows the parallel circuit to be separated into 2 independent single-device circuits and provides footprints that can be populated with additional passive components to allow for testing of customized designs.

More detailed information about the default EVM configuration can be found in the [Parallel Configuration Schematic](#) and the [Parallel Configuration Bill of Materials](#).

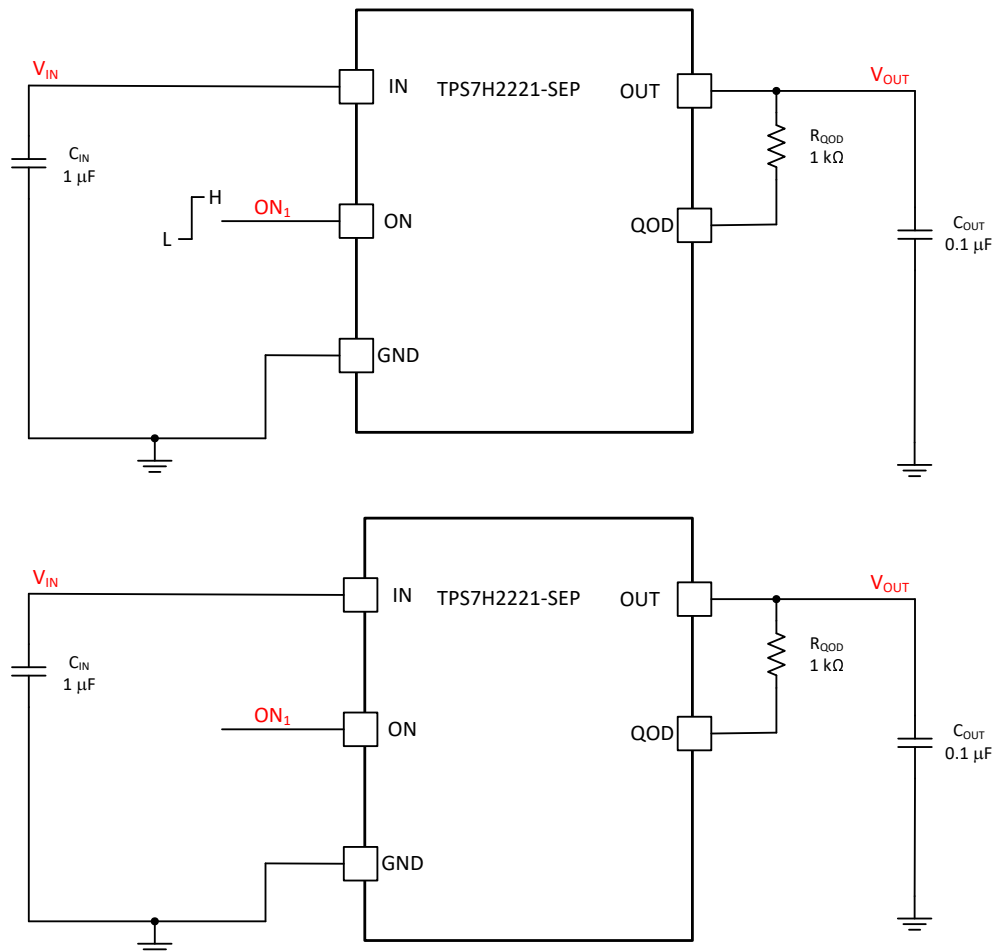


Figure 1-1. Parallel-device Configuration Simplified Schematic

Table 1-1. TPS7H2221EVM Parallel-device Configuration

Specification	Value	Description
Input Voltage (V_{IN})	3.3 V	Falls within the recommended device input voltage range of 1.6 V to 5.5 V.
Output Current (I_{OUT})	0 to 2.5 A	Does not exceed maximum device continuous switch current of 1.25 A per device.
ON pin Input High ($V_{IH,ON}$)	1 to 5.5 V	High and Low inputs to the ON pin. ON ₁ and ON ₂ tied together by R17.
ON pin Input Low ($V_{IH,ON}$)	0 to 0.35 V	
Output Discharge Time (t_{FALL})	~0.22 ms	Typical output discharge time. Set by: <ul style="list-style-type: none"> R4 and R16 (R_{QOD}) = 1 kΩ JP5 and JP10 shunted

1.2 Alternate Board Configurations

If a custom configuration is desired, users should refer to the [TPS7H2221-SEP data sheet](#) to calculate the values of passive components around the device and note any operational requirements.

In addition to the default EVM configuration, this user's guide provides an example for how the TPS7H2221EVM may be configured for single-device operation. The targeted Output Discharge Time and the ON pin input values for the single-device configuration are the same as the default configuration. However, this configuration provides half the output current compared to the parallel-device configuration.

More detailed information about the example single-device EVM configuration can be found in the [Single-device Configuration Schematic](#) and the [Single-device Configuration Bill of Materials](#).

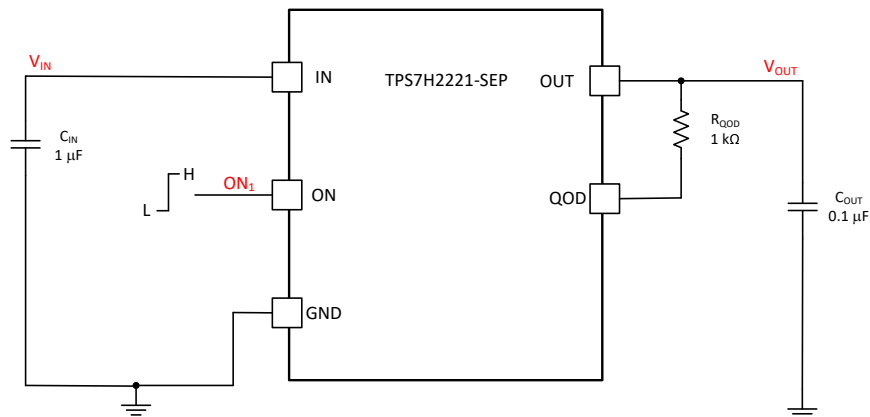


Figure 1-2. Single-device Configuration Simplified Schematic

Table 1-2. TPS7H2221EVM Single-device Configuration

Specification	Value	Description
Input Voltage (V_{IN})	3.3 V	Falls within the recommended device input voltage range of 1.6 V to 5.5 V.
Output Current (I_{OUT})	0 to 1.25 A	Does not exceed maximum device continuous switch current of 1.25 A per device.
ON pin Input High ($V_{IH,ON}$)	1 to 5.5 V	High and Low inputs to the ON pin.
ON pin Input Low ($V_{IH,ON}$)	0 to 0.35 V	
Output Discharge Time (t_{FALL})	~0.22 ms	Typical output discharge time. Set by: R4/R16 (R_{QOD}) = 1 k Ω JP5/JP10 shunted

2 EVM Connectors and Test Points

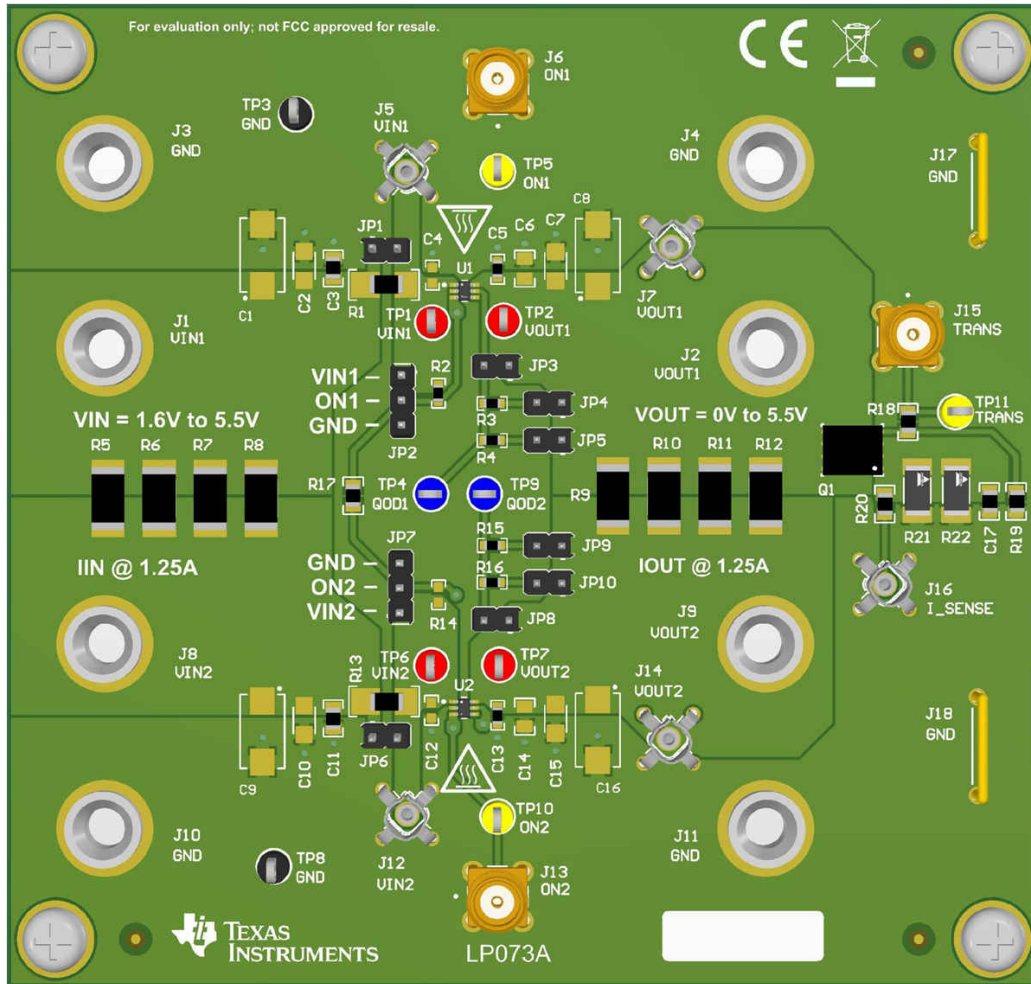


Figure 2-1. TPS7H2221EVM 3D Rendering (Top)

Table 2-1. Summary of Connectors and Test Points

Connector or Jumper	Test Point	Function	
J1	J5, TP1	VIN1	Input Power for Board
J8	J12, TP6	VIN2	
J2	J7, TP2	VOUT1	Output Power for Board
J9	J14, TP7	VOUT2	
J3, J4, J10, J11	J17, J18, TP3, TP8	GND	Ground
J6, JP2	TP5	ON1	ON Pin
J13, JP7	TP10	ON2	
JP3, JP4, JP5	TP4	QOD1	QOD Pin
JP8, JP9, JP10	TP9	QOD2	
J15	TP11	TRANS	Output Transient FET Gate Signal
N/A	J16	I_SENSE	Output Transient Current Sense Test Point

3 Test Results

Test results are shown for the parallel configuration. The following tests were performed:

1. [Startup](#)
2. [Shutdown](#)
3. [Quick Output Discharge \(QOD\) functionality](#)

3.1 Parallel Configuration Results

The results shown in below were observed using the TPS7H2221EVM in its default parallel configuration with $V_{IN} = 3.3\text{ V}$.

Startup Tests

When $V_{ON} < V_{IL}$, the device connects a Smart Pull Down (typically 491 kOhms) to the ON pin to prevent it from floating until system sequencing is complete. Once V_{ON} is driven $> V_{IH}$, the Smart Pull Down is disconnected.

By default, the ON pin is tied to V_{IN} on the EVM via R2 so that the user can utilize the jumpers (JP2 or JP7) without leaving the ON pin floating. If the jumpers are not being utilized, it is typically recommended to remove R2 and enable the device by applying an external signal to the ON pin via J6 or TP5 once V_{IN} is HIGH for cleaner startup.

Figure 3-1 Test Conditions: ON tied to VIN, I_{OUT} = 2A

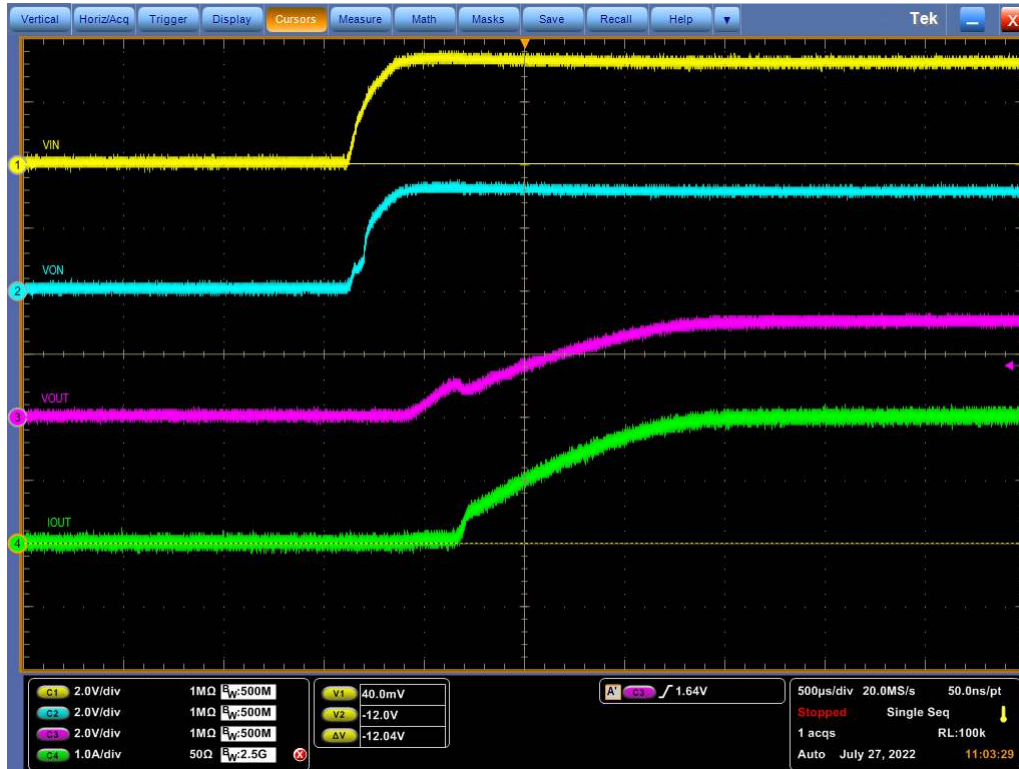


Figure 3-1. Startup

Figure 3-2 Test Conditions: External signal applied to ON, I_{OUT} = 2A

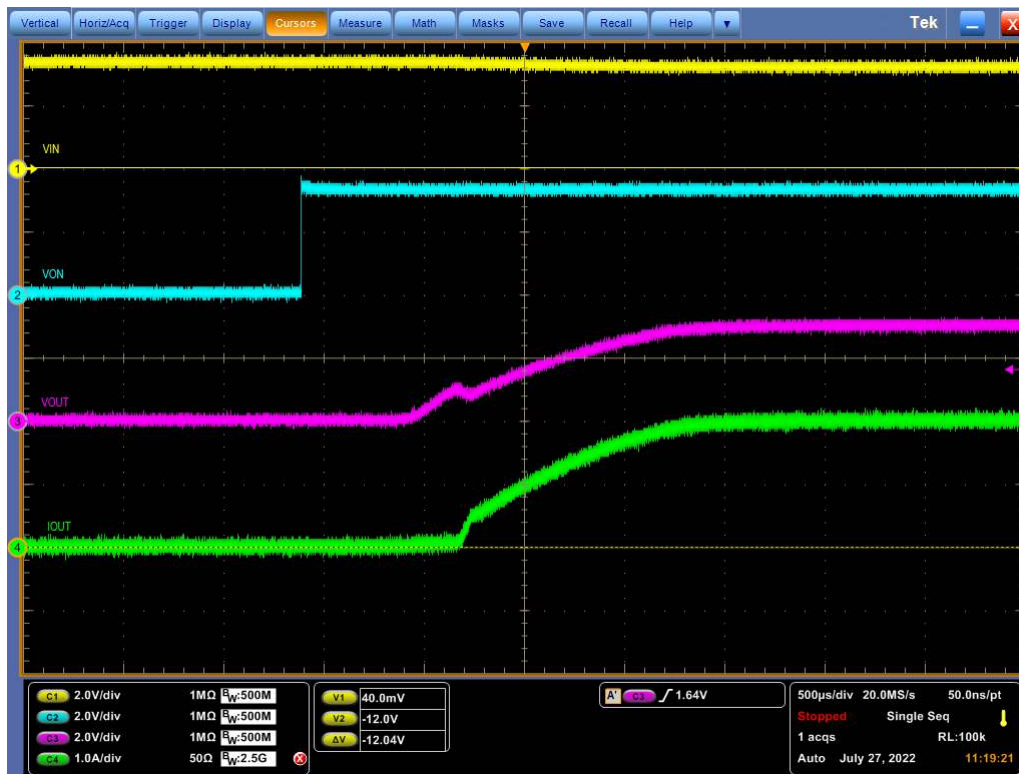


Figure 3-2. ON - Low to High

Shutdown Tests

Figure 3-3 Test Conditions: ON tied to VIN, $I_{OUT} = 2A$

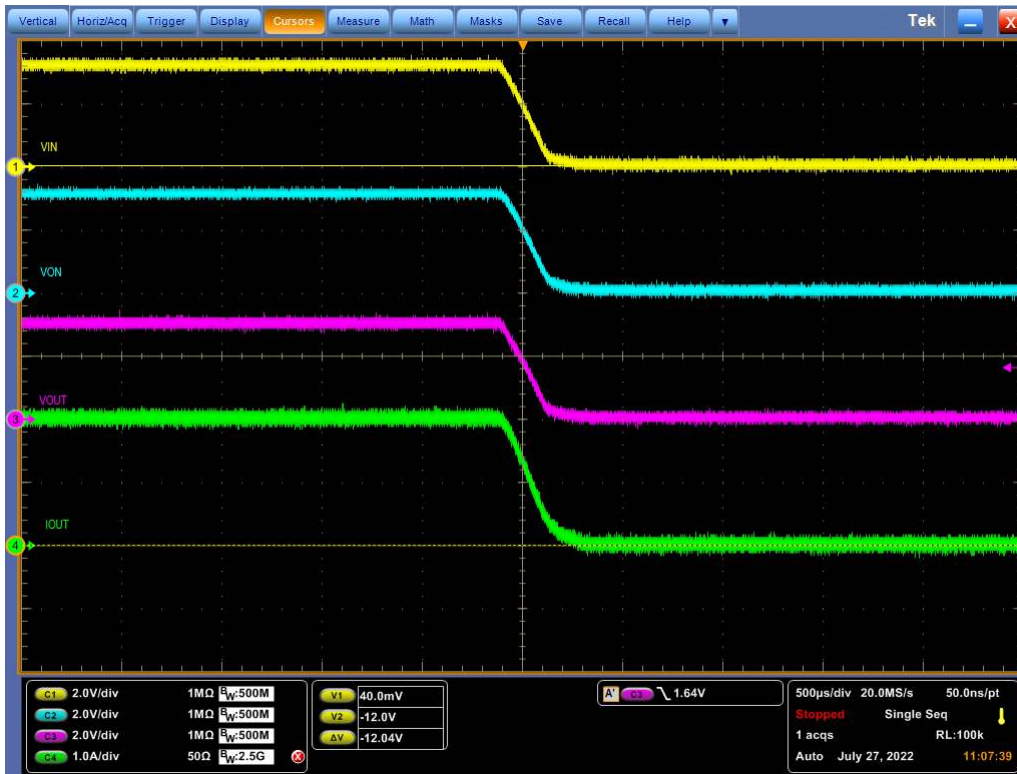


Figure 3-3. Shutdown

Figure 3-4 Test Conditions: External signal applied to ON, $I_{OUT} = 2A$

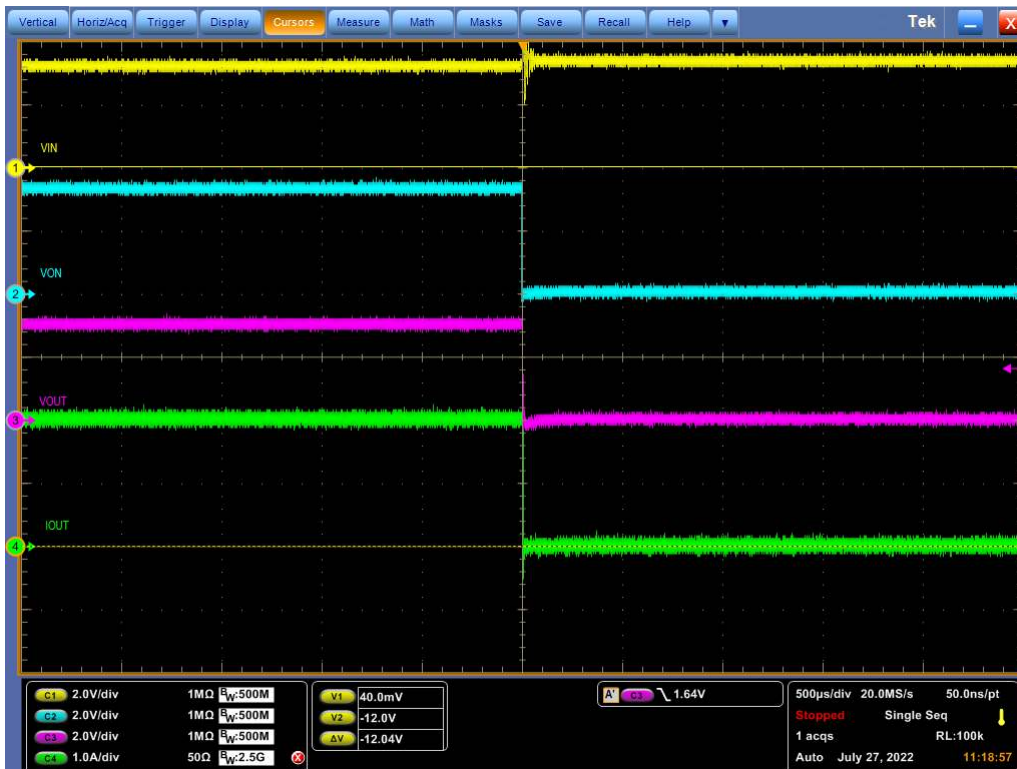


Figure 3-4. ON - High to Low

Quick Output Discharge (QOD) Tests

The Quick Output Discharge (QOD) feature of the TPS7H2221-SEP is controlled by the voltage sensed at the ON pin. When $V_{ON} > V_{IH}$, V_{OUT} follows V_{IN} . When $V_{ON} < V_{IL}$, the output is discharged to GND via the QOD pin and R_{QOD} (if desired). If the QOD pin is left open, then V_{OUT} will be left floating when $V_{ON} < V_{IL}$ and it will discharge through the load or board parasitics.

In the [Shutdown Tests](#) section above, the scope shots show the difference in V_{OUT} behavior when V_{ON} is tied to V_{IN} versus when it is set LOW using an external signal. In the first case, V_{OUT} simply follows V_{IN} as it falls because $V_{ON} > V_{IH}$. In the second case, V_{OUT} is quickly discharged by the load and QOD because $V_{ON} < V_{IL}$, which is preferred.

The results shown in this section focus on configurations where $I_{OUT} = 0A$ so that the impact of different QOD resistances on V_{OUT} fall time can be more easily observed. If a higher load is present, it will typically be the dominant factor in V_{OUT} fall time.

To calculate V_{OUT} fall time for devices in parallel configuration, the total R_{QOD} will be $R_{QOD1} || R_{QOD2}$ and the total C_{OUT} will be $C_{OUT1} + C_{OUT2}$.

Figure 3-5 Test Conditions: External signal applied to ON, $I_{OUT} = 0A$, all QOD jumpers left open

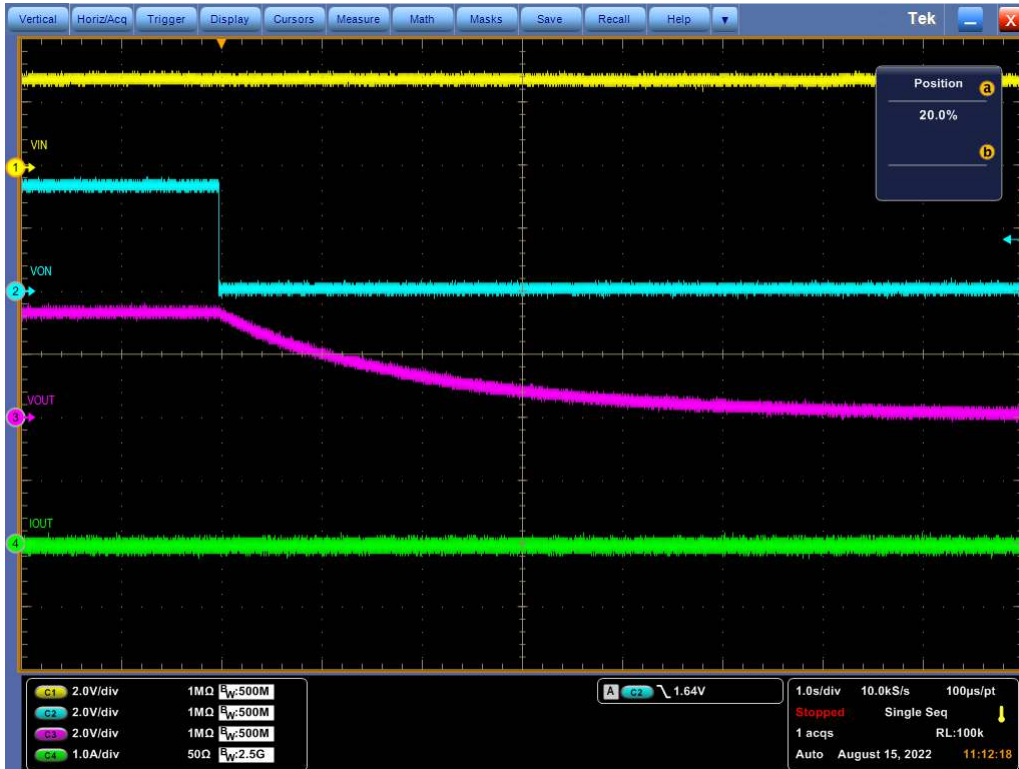


Figure 3-5. V_{OUT} Fall Time: $R_{QOD}=OPEN$

Figure 3-6 Test Conditions: External signal applied to ON, $I_{OUT} = 0A$, JP4 and JP9 shunted

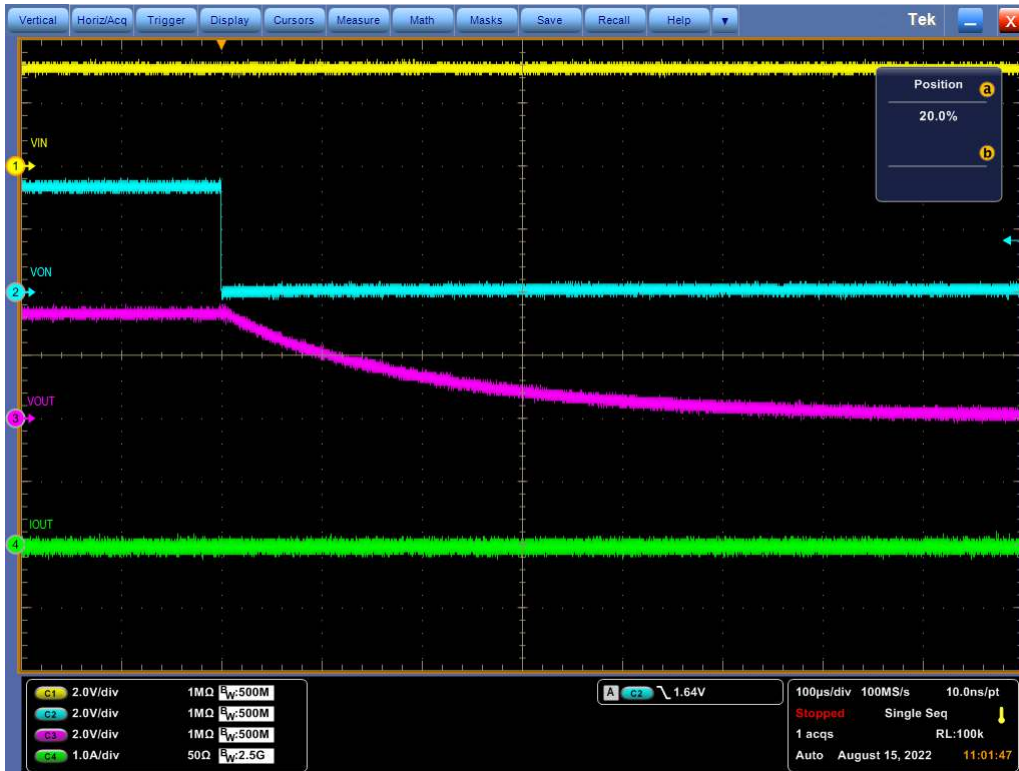


Figure 3-6. V_{OUT} Fall Time: $R_{QOD}=1\text{ kOhms}$

Figure 3-7 Test Conditions: External signal applied to ON, $I_{OUT} = 0A$, JP5 and JP10 shunted

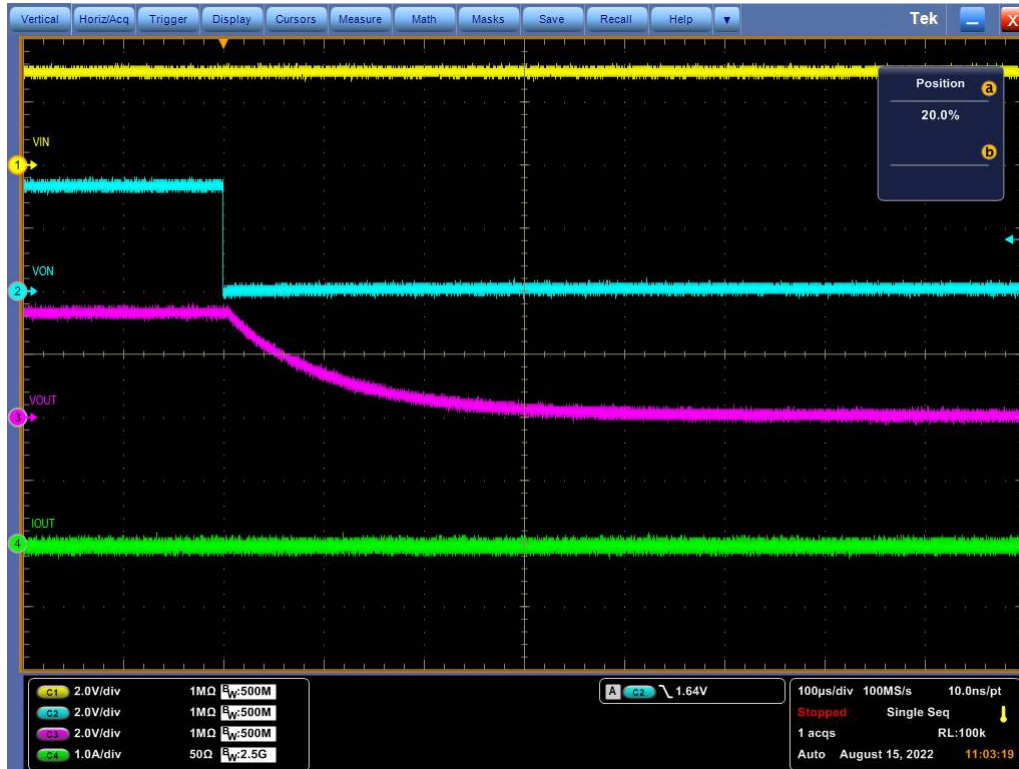


Figure 3-7. V_{OUT} Fall Time: $R_{QOD}=500$ Ohms

Figure 3-8 Test Conditions: External signal applied to ON, $I_{OUT} = 0A$, JP3 and JP8 shunted

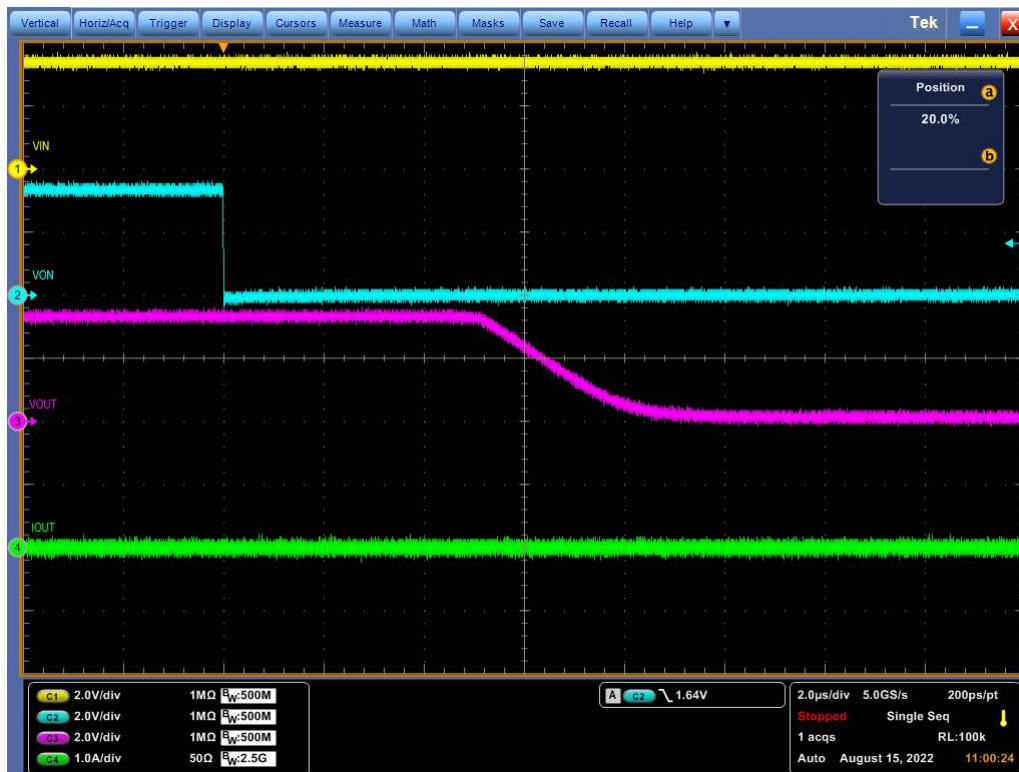


Figure 3-8. V_{OUT} Fall Time: QOD tied to V_{OUT}

4 Load Transient Circuitry

The TPS7H2221EVM contains a sub-circuit which enables the user to test how the TPS7H2221-SEP responds to a load transient. In many cases an electronic load (e-load) will suffice. However, in some scenarios the inductance introduced by the wire leads to an e-load can cause issues that interfere with testing. This problem is resolved through the use of the load transient sub-circuit that is provided on the EVM.

Figure 4-1 shows the schematic for this transient circuit. A power MOSFET provided by Texas Instruments at Q1 is used to momentarily press the regulated VOUT voltage across power resistors R21 and R22 by modulating the gate of Q1 at JP15 with low duty cycle square wave.

The default EVM components are configured for output short-circuit testing.

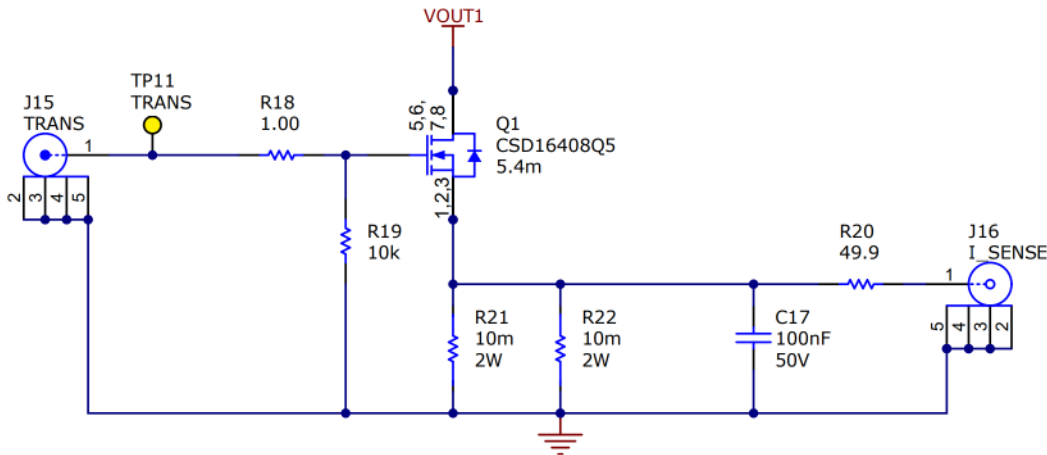


Figure 4-1. TPS7H2221EVM Load Transient Sub-circuit

By changing the value of the power resistor(s) and the initial current set by the e-load, any desired current step size is achievable. The transient current step size is determined by:

$$I_{\text{TRANS}} = \frac{V_{\text{OUT}}}{R_{\text{DS}_{\text{ON}_Q1}} + (R_{21} || R_{22})} \quad (1)$$

Eliminating the uncertainty of $R_{\text{DS}_{\text{ON}_Q1}}$ in the calculation of the transient current is possible by capturing the actual voltage at probe testpoint J16 and dividing by $(R_{21} || R_{22})$.

$$I_{\text{TRANS}} = \frac{V_{\text{J16}}}{(R_{21} || R_{22})} \quad (2)$$

The key to a successful measurement (i.e. one without a smoking resistor), is to determine the duty cycle to apply to the gate of Q1 to allow the right amount of current through so as to not exceed the power rating of R21 and R22.

$$P_{\text{TRANS}} = V_{\text{J16}} \times I_{\text{TRANS}} \quad (3)$$

R21 and R22 have a power rating of 2 W. The maximum duty cycle of the square wave applied to the gate of Q1 is:

$$D_{\text{J15}} = \frac{P_{\text{RATED}}}{P_{\text{TRANS}}} \quad (4)$$

It is a good idea to leaving some margin for error by using a duty cycle lower than the maximum value calculated above.

The resistors on the gate of the FET can be used to control the turn-on and turn-off times of the transient. The voltage amplitude of the low duty cycle square wave applied to the gate of the FET via J15 will also impact the $R_{DS(ON)}$ of the FET.

Output Short-Circuit Testing

If desired, the user is also able to test device behavior under output short-circuit conditions by using low resistances for R21 and R22. This trips the short-circuit protection features of the device, which limit the maximum value of the transient. Faster transients will typically result in higher peak current values.

One must take caution during such tests as they typically exceed the recommended operating conditions of the device, which can lead to damage or degradation of the part.

5 Board Layout

Figure 5-1 through Figure 5-5 show the layout of the TPS7H2221EVM.

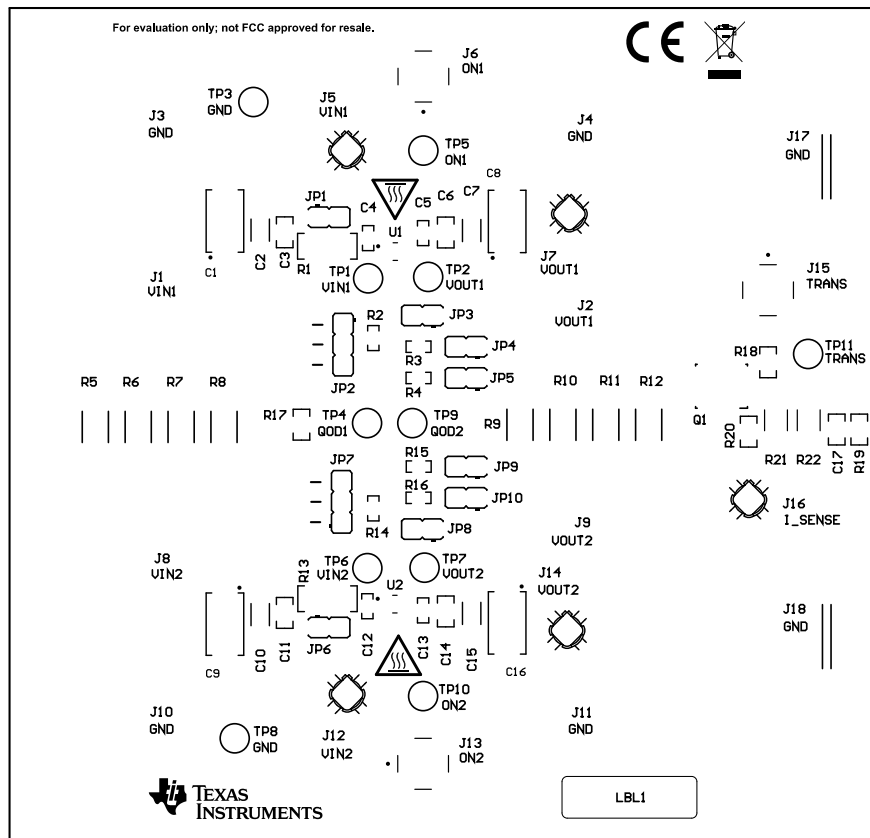


Figure 5-1. Top Silkscreen

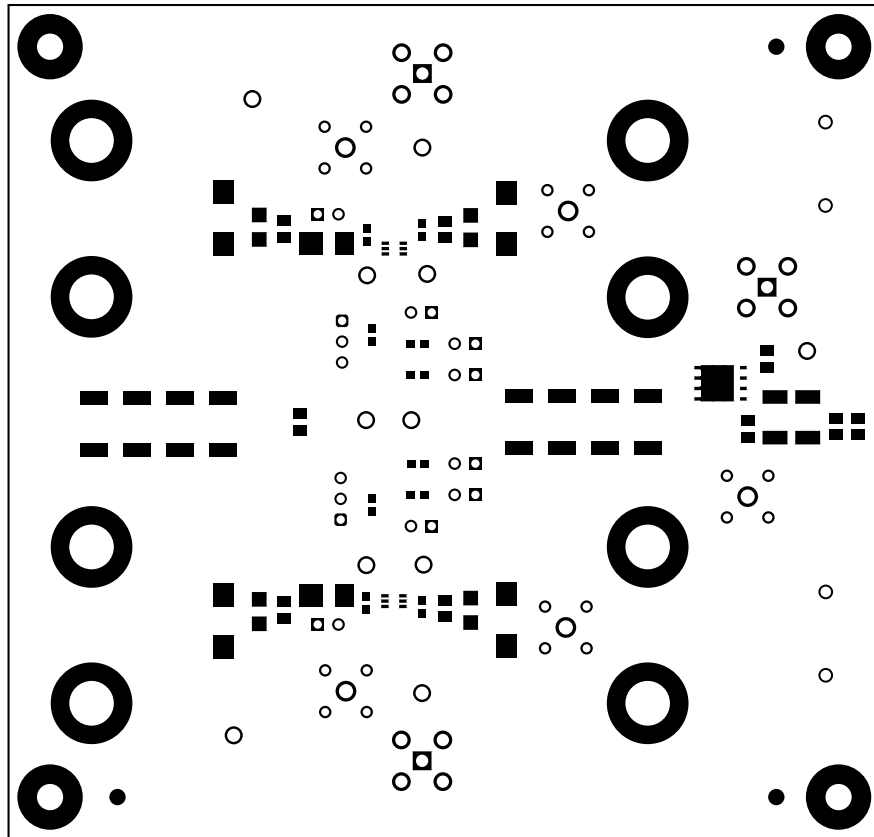


Figure 5-2. Top Solder

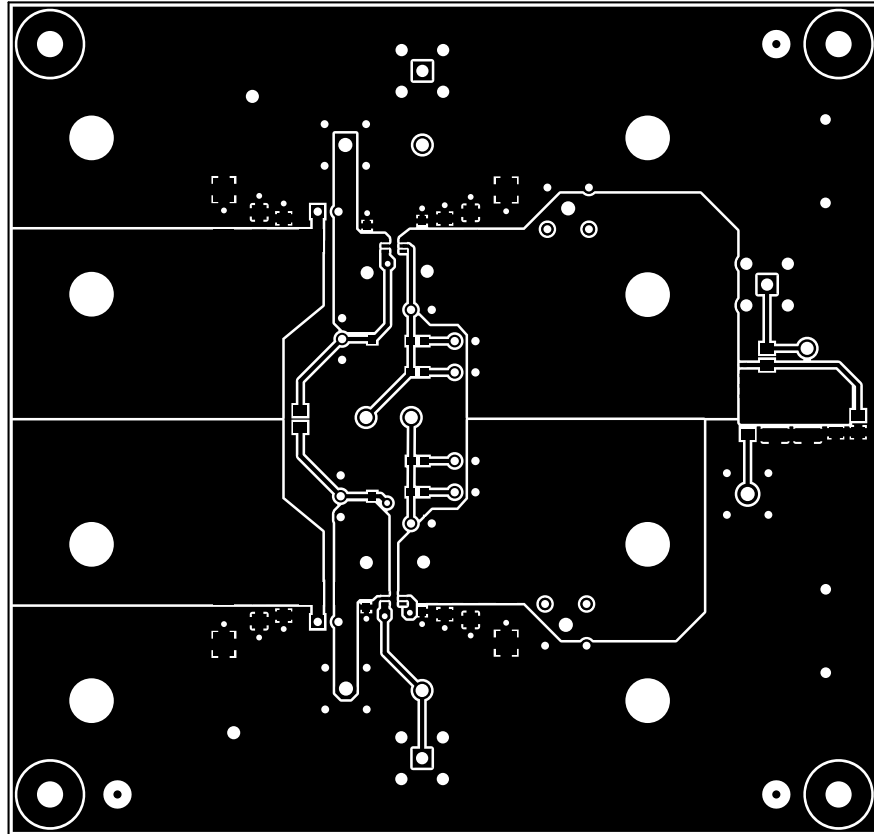


Figure 5-3. Top Layer

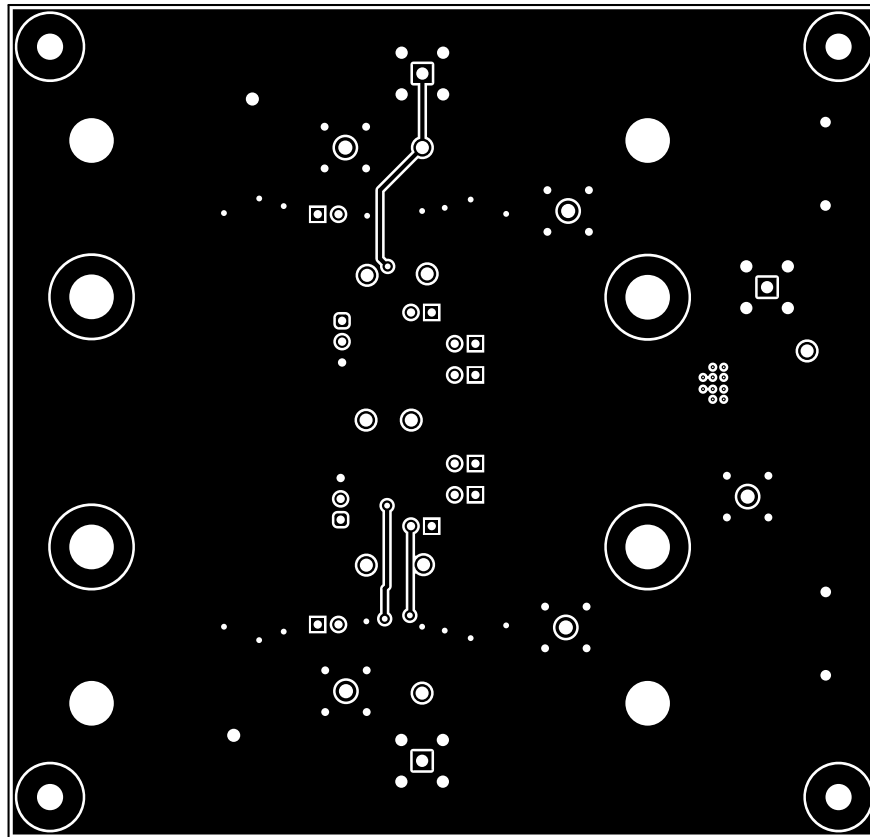


Figure 5-4. Bottom Layer

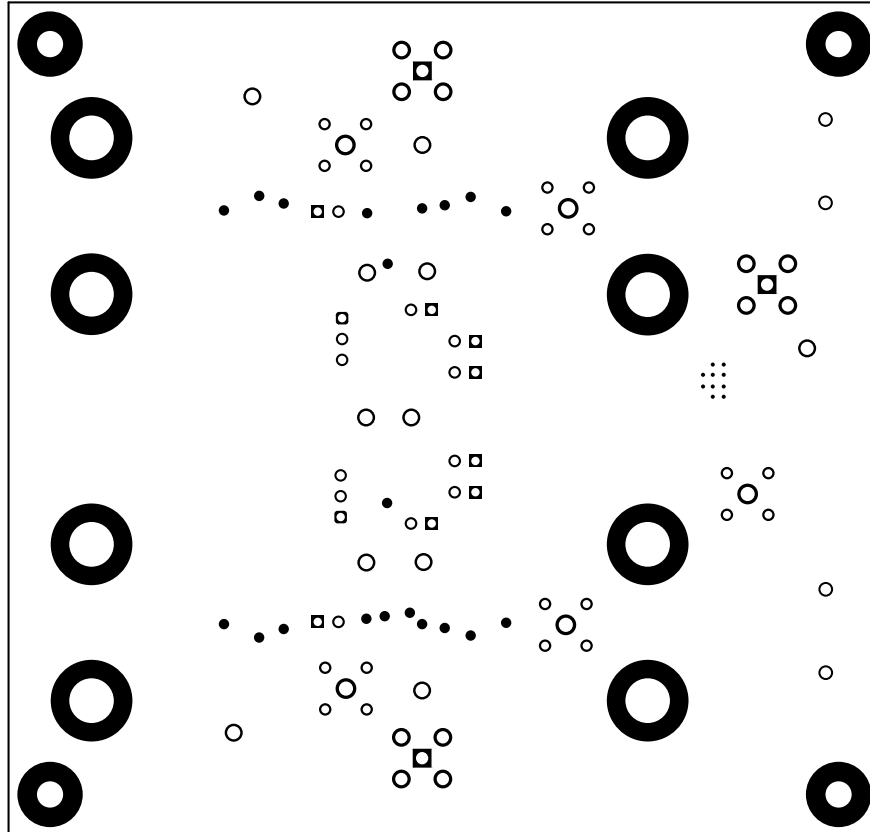


Figure 5-5. Bottom Solder

6 Schematic

Parallel Configuration Schematic shows the default parallel-device TPS7H2221EVM schematic. Single Configuration Schematic is an example schematic of the EVM configured for two separate single-device circuits.

6.1 Parallel Configuration Schematic

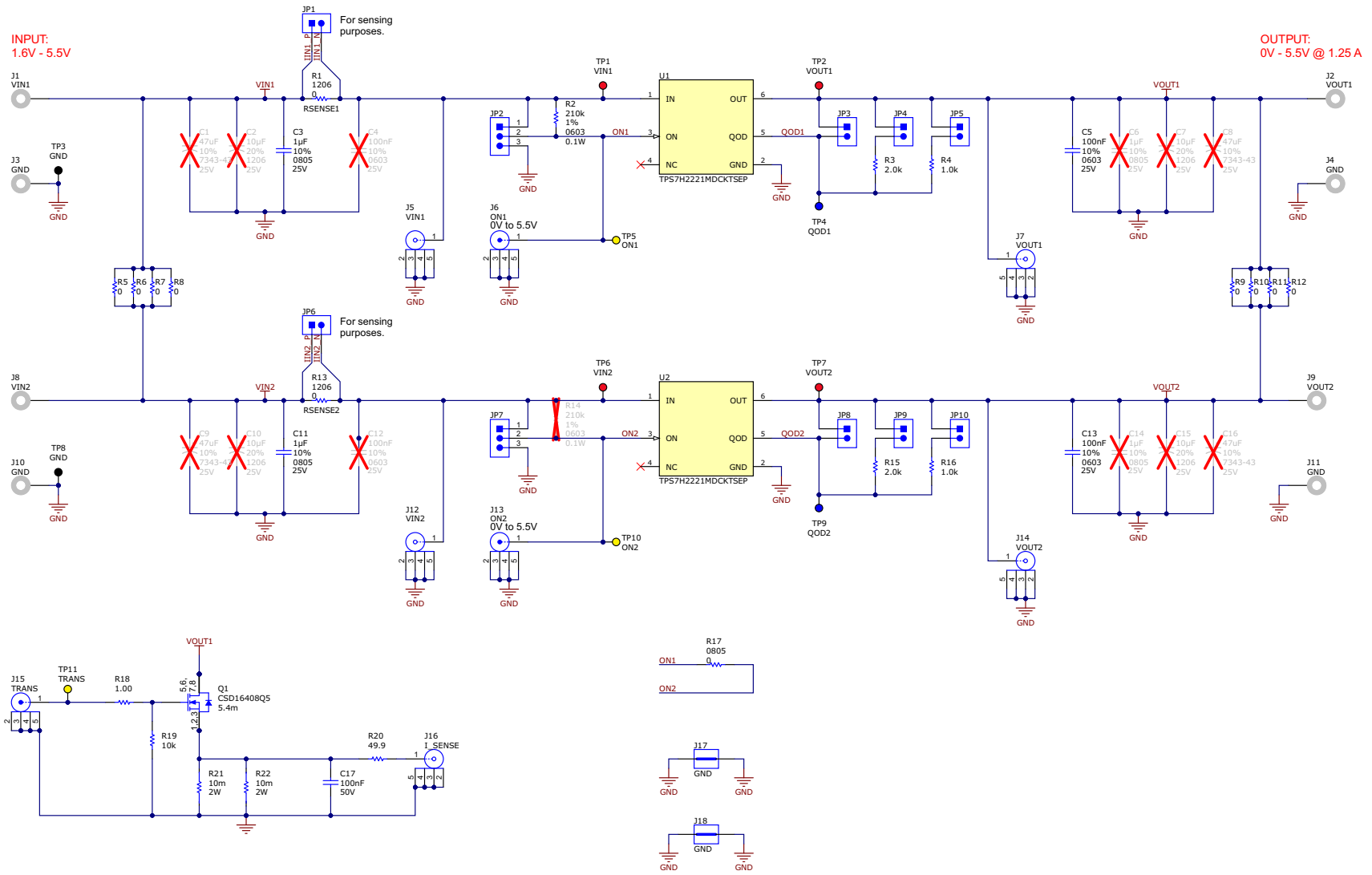
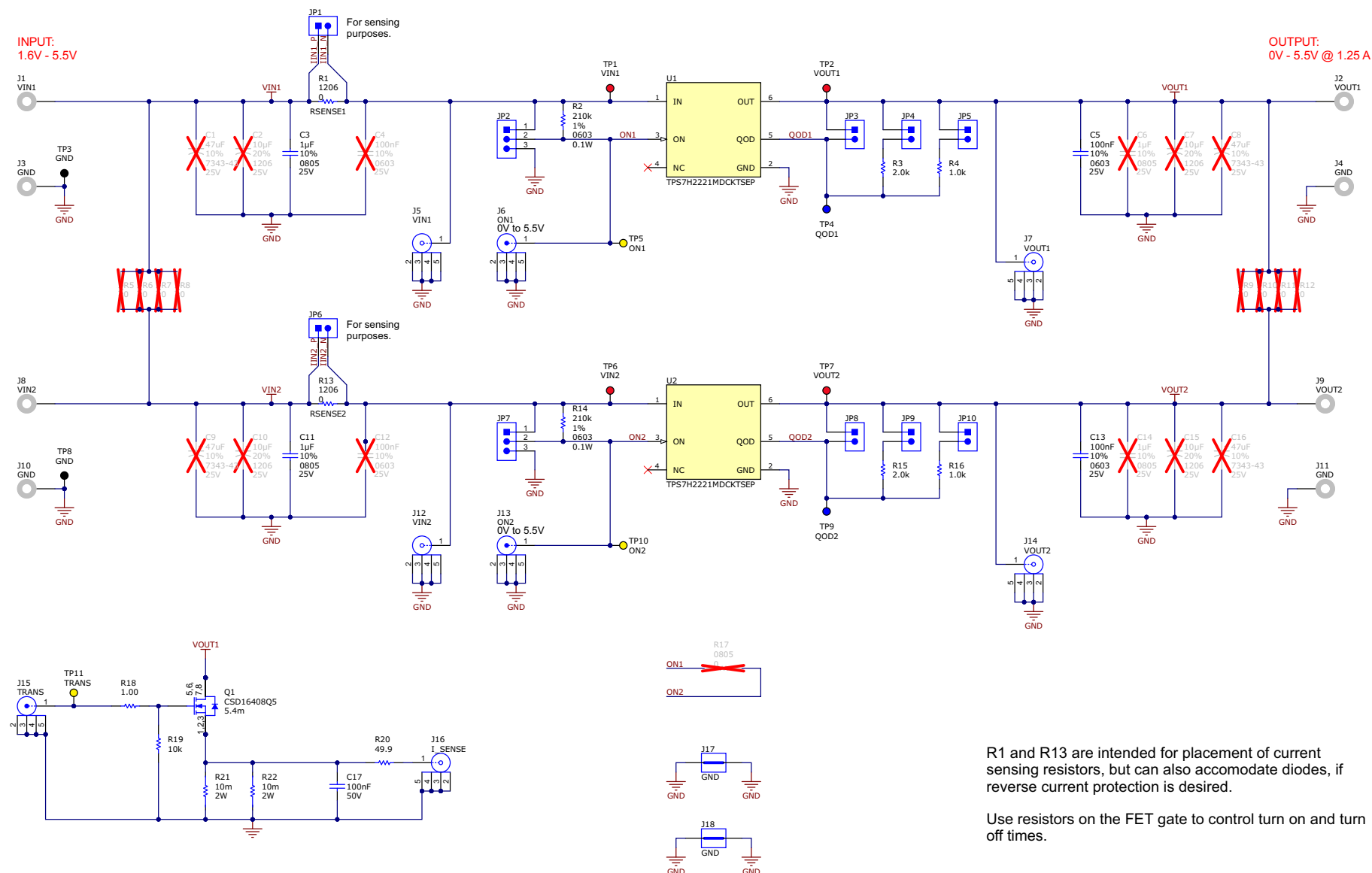


Figure 6-1. TPS7H2221EVM Parallel-Device Schematic

6.2 Single Configuration Schematic



R1 and R13 are intended for placement of current sensing resistors, but can also accommodate diodes, if reverse current protection is desired.

Use resistors on the FET gate to control turn on and turn off times.

Figure 6-2. TPS7H2221EVM Single-Device Schematic

7 Bill of Materials (BOM)

[Parallel Configuration BOM](#) lists the BOM for the default parallel-device TPS7H2221EVM configuration. [Single Configuration BOM](#) lists an example BOM for the EVM configured for two separate single-device circuits.

7.1 Parallel Configuration BOM

Table 7-1. TPS7H2221EVM Parallel BOM

Designator	Quantity	Description	Part Number	Manufacturer
!PCB1	1	Printed Circuit Board	LP073	Any
C3, C11	2	CAP, CERM, 1 uF, 25 V, +/- 10%, X7R, 0805	TMK212B7105KG-T	Taiyo Yuden
C5, C13	2	CAP, CERM, 0.1 uF, 25 V, +/- 10%, X7R, 0603	885012206071	Wurth Elektronik
C17	1	CAP, CERM, 0.1 uF, 50 V, +/- 10%, X7R, 0805	C0805C104K5RACTU	Kemet
FID1, FID2, FID3	3	Fiducial mark. There is nothing to buy or mount.	N/A	N/A
H1, H2, H3, H4	4	Machine Screw, Round, #4-40 x 1/4, Nylon, Philips panhead	NY PMS 440 0025 PH	B&F Fastener Supply
H5, H6, H7, H8	4	Standoff, Hex, 0.5"L #4-40 Nylon	1902C	Keystone Electronics
J1, J2, J3, J4, J8, J9, J10, J11	8	Standard Banana Jack, Uninsulated, 5.5mm	575-4	Keystone Electronics
J5, J7, J12, J14, J16	5	Compact Probe Tip Circuit Board Test Points, TH, 25 per	131-5031-00	Tektronix
J6, J13, J15	3	SMA Connector Receptacle, Female Socket 50Ohm Through Hole Solder	733910060	Molex
J17, J18	2	1mm Un-insulated Shorting Plug, 10.16mm spacing, TH	D3082-05	Harwin
JP1, JP3, JP4, JP5, JP6, JP8, JP9, JP10	8	Header, 2.54mm, 2x1, Tin, TH	22284023	Molex
JP2, JP7	2	Header, 2.54mm, 3x1, Tin, TH	22284030	Molex
LBL1	1	Thermal Transfer Printable Labels, 0.650" W x 0.200" H - 10,000 per roll	THT-14-423-10	Brady
Q1	1	MOSFET, N-CH, 25 V, 113 A, DQH0008A (VSON-CLIP-8)	CSD16408Q5	Texas Instruments
R1, R13	2	RES, 0, 0.75 W, AEC-Q200 Grade 0, 1206	CRCW12060000Z0EAHP	Vishay-Dale
R2	1	RES, 210 k, 1%, 0.1 W, 0603	RC0603FR-07210KL	Yageo
R3, R15	2	RES, 2.0 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW06032K00JNEA	Vishay-Dale
R4, R16	2	RES, 1.0 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW06031K00JNEA	Vishay-Dale
R5, R6, R7, R8, R9, R10, R11, R12	8	RES, 0, 5%, 1 W, 2512	RC6432J000CS	Samsung
R17	1	RES, 0, 5%, 0.125 W, 0805	CRCW08050000Z0EA	Vishay-Dale
R18	1	RES, 1.00, 1%, 0.125 W, 0805	RC0805FR-071RL	Yageo
R19	1	RES, 10 k, 5%, 0.125 W, AEC-Q200 Grade 0, 0805	CRCW080510K0JNEA	Vishay-Dale
R20	1	RES, 49.9, 0.1%, 0.125 W, 0805	RT0805BRD0749R9L	Yageo

Table 7-1. TPS7H2221EVM Parallel BOM (continued)

Designator	Quantity	Description	Part Number	Manufacturer
R21, R22	2	10 mOhms \pm 1% 2W Chip Resistor 2010 (5025 Metric) Anti-Sulfur, Automotive AEC-Q200, Current Sense, Moisture Resistant, Pulse Withstanding Metal Element	WSLP2010R0100FEA	Vishay-Dale
TP1, TP2, TP6, TP7	4	Test Point, Multipurpose, Red, TH	5010	Keystone Electronics
TP3, TP8	2	Test Point, Multipurpose, Black, TH	5011	Keystone Electronics
TP4, TP9	2	Test Point, Multipurpose, Blue, TH	5127	Keystone Electronics
TP5, TP10, TP11	3	Test Point, Multipurpose, Yellow, TH	5014	Keystone Electronics
U1, U2	2	TPS7H2221-SEP Radiation Tolerant 5.5-V, 1.25-A, 115-m Ω Load Switch	TPS7H2221MDCKTSEP	Texas Instruments
C1, C8, C9, C16	0	CAP, TA, 47 μ F, 25 V, +/- 10%, 0.08 ohm, SMD	T495X476K025ATE080	Kemet
C2, C7, C10, C15	0	CAP, Tantalum Polymer, 10 μ F, 25 V, +/- 20%, 0.15 ohm, 3216-18 SMD	TCJA106M025R0150	AVX
C4, C12	0	CAP, CERM, 0.1 μ F, 25 V, +/- 10%, X7R, 0603	885012206071	Wurth Elektronik
C6, C14	0	CAP, CERM, 1 μ F, 25 V, +/- 10%, X7R, 0805	TMK212B7105KG-T	Taiyo Yuden
R14	0	RES, 210 k, 1%, 0.1 W, 0603	RC0603FR-07210KL	Yageo

7.2 Single Configuration BOM

Table 7-2. TPS7H2221EVM Single BOM

Designator	Quantity	Description	Part Number	Manufacturer
!PCB1	1	Printed Circuit Board	LP073	Any
C3, C11	2	CAP, CERM, 1 uF, 25 V, +/- 10%, X7R, 0805	TMK212B7105KG-T	Taiyo Yuden
C5, C13	2	CAP, CERM, 0.1 uF, 25 V, +/- 10%, X7R, 0603	885012206071	Würth Elektronik
C17	1	CAP, CERM, 0.1 uF, 50 V, +/- 10%, X7R, 0805	C0805C104K5RACTU	Kemet
FID1, FID2, FID3	3	Fiducial mark. There is nothing to buy or mount.	N/A	N/A
H1, H2, H3, H4	4	Machine Screw, Round, #4-40 x 1/4, Nylon, Philips panhead	NY PMS 440 0025 PH	B&F Fastener Supply
H5, H6, H7, H8	4	Standoff, Hex, 0.5"L #4-40 Nylon	1902C	Keystone Electronics
J1, J2, J3, J4, J8, J9, J10, J11	8	Standard Banana Jack, Uninsulated, 5.5mm	575-4	Keystone Electronics
J5, J7, J12, J14, J16	5	Compact Probe Tip Circuit Board Test Points, TH, 25 per	131-5031-00	Tektronix
J6, J13, J15	3	SMA Connector Receptacle, Female Socket 50Ohm Through Hole Solder	733910060	Molex
J17, J18	2	1mm Un-insulated Shorting Plug, 10.16mm spacing, TH	D3082-05	Harwin
JP1, JP3, JP4, JP5, JP6, JP8, JP9, JP10	8	Header, 2.54mm, 2x1, Tin, TH	22284023	Molex
JP2, JP7	2	Header, 2.54mm, 3x1, Tin, TH	22284030	Molex
LBL1	1	Thermal Transfer Printable Labels, 0.650" W x 0.200" H - 10,000 per roll	THT-14-423-10	Brady
Q1	1	MOSFET, N-CH, 25 V, 113 A, DQH0008A (VSON-CLIP-8)	CSD16408Q5	Texas Instruments
R1, R13	2	RES, 0, 0.75 W, AEC-Q200 Grade 0, 1206	CRCW12060000Z0EAHP	Vishay-Dale
R2, R14	2	RES, 210 k, 1%, 0.1 W, 0603	RC0603FR-07210KL	Yageo
R3, R15	2	RES, 2.0 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW06032K00JNEA	Vishay-Dale
R4, R16	2	RES, 1.0 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW06031K00JNEA	Vishay-Dale
R18	1	RES, 1.00, 1%, 0.125 W, 0805	RC0805FR-071RL	Yageo
R19	1	RES, 10 k, 5%, 0.125 W, AEC-Q200 Grade 0, 0805	CRCW080510K0JNEA	Vishay-Dale
R20	1	RES, 49.9, 0.1%, 0.125 W, 0805	RT0805BRD0749R9L	Yageo
R21, R22	2	10 mOhms ±1% 2W Chip Resistor 2010 (5025 Metric) Anti-Sulfur, Automotive AEC-Q200, Current Sense, Moisture Resistant, Pulse Withstanding Metal Element	WSLP2010R0100FEA	Vishay-Dale
TP1, TP2, TP6, TP7	4	Test Point, Multipurpose, Red, TH	5010	Keystone Electronics

Table 7-2. TPS7H2221EVM Single BOM (continued)

Designator	Quantity	Description	Part Number	Manufacturer
TP3, TP8	2	Test Point, Multipurpose, Black, TH	5011	Keystone Electronics
TP4, TP9	2	Test Point, Multipurpose, Blue, TH	5127	Keystone Electronics
TP5, TP10, TP11	3	Test Point, Multipurpose, Yellow, TH	5014	Keystone Electronics
U1, U2	2	TPS7H2221-SEP Radiation Tolerant 5.5-V, 1.25-A, 115-mΩ Load Switch	TPS7H2221MDCKTSEP	Texas Instruments
C1, C8, C9, C16	0	CAP, TA, 47 uF, 25 V, +/- 10%, 0.08 ohm, SMD	T495X476K025ATE080	Kemet
C2, C7, C10, C15	0	CAP, Tantalum Polymer, 10 μF, 25 V, +/- 20%, 0.15 ohm, 3216-18 SMD	TCJA106M025R0150	AVX
C4, C12	0	CAP, CERM, 0.1 uF, 25 V, +/- 10%, X7R, 0603	885012206071	Wurth Elektronik
C6, C14	0	CAP, CERM, 1 uF, 25 V, +/- 10%, X7R, 0805	TMK212B7105KG-T	Taiyo Yuden
R5, R6, R7, R8, R9, R10, R11, R12	0	RES, 0, 5%, 1 W, 2512	RC6432J000CS	Samsung
R17	0	RES, 0, 5%, 0.125 W, 0805	CRCW08050000Z0EA	Vishay-Dale

8 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
August 2022	*	Initial release

9 Related Documentation

- Texas Instruments, [Standard Terms for Evaluation Modules](#)

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2022, Texas Instruments Incorporated