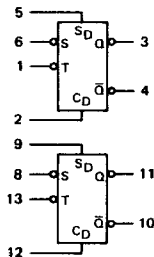


MC978 • MC878



Available in TO-86 Flat Package, Add F Suffix.

The type "D" Flip-Flop is a storage element that stores the state of the S input during negative transitions of the T input. The flip-flop state is not affected by changes in the S input during either the low or the high state of the T input. S_D and C_D inputs may be used for asynchronous operation.



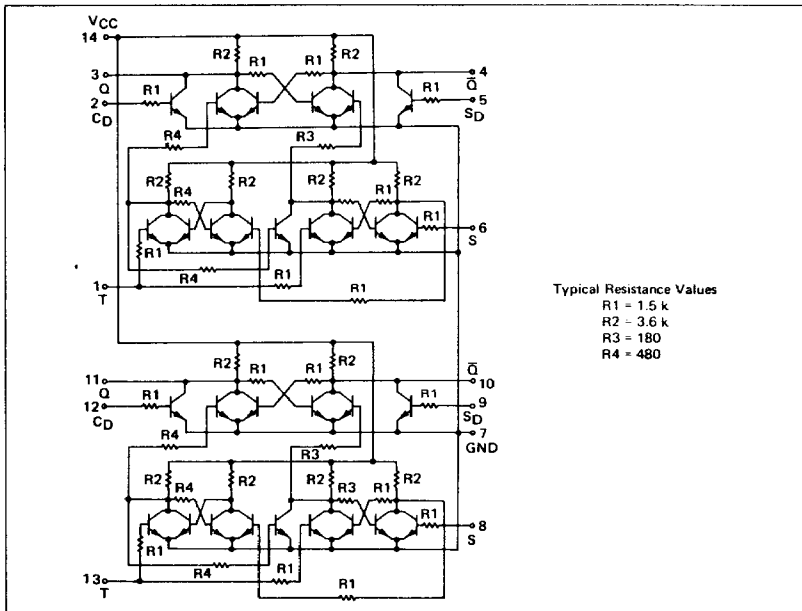
DIRECT INPUT OPERATION \oplus

S_D	C_D	Q	\bar{Q}
0	0	0	1
1	0	1	0
0	1	0	1
1	1	0	0

CLOCKED INPUT OPERATION \ominus

t_n	t_{n+1}	S	Q
1	0	0	0
1	1	0	0
0	0	1	1

1. Clock (T input) must be high.
2. The output state will not change when the input state goes from $S_D = \bar{C}_D$ to $S_C = C_C = 0$. The output state cannot be predetermined in the case when the input goes from $S_D = C_D = 1$ to $S_D = C_D = 0$.
3. Direct inputs (S_D and C_D) must be low.
4. The time period prior to the negative transition of the clock pulse is denoted t_n and the time period subsequent to this transition is denoted t_{n+1} .



Typical Resistance Values
 R1 = 1.5 k
 R2 = 3.6 k
 R3 = 180
 R4 = 480

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MC978, MC878 (continued)

ELECTRICAL CHARACTERISTICS

Test procedures are shown for one flip-flop only. The other flip-flop is tested in the same manner.

Characteristic	Symbol	Pin Under Test	TEST VOLTAGE VALUES (Volts)												
			@Test Temperature						TEST VOLTAGE APPLIED TO PINS LISTED BELOW						
			V _{in}	V _{em}	V _{BOT}	V _{eff}	V _{CC}	V _{LL}	V _{in}	V _{em}	V _{BOT}	V _{eff}	V _{CC}	V _{LL}	
Input Current	1.8 I _{in}	1	MC978												
	1.8 I _{in}	2*	MC878												
	I _{in}	5*	MC978												
	I _{in}	6*	MC878												
	Output Current	I _{A3}	3	MC978											
	Output Current	I _{A3}	3*	MC878											
Output Voltage	V _{out}	3	MC978												
	V _{out}	4	MC878												
	V _{CE(sat)}	3	MC978												
	V _{CE(sat)}	4	MC878												
Saturation Voltage	V _{CE(sat)}	3	MC978												
	V _{CE(sat)}	3*	MC878												
	V _{CE(sat)}	3†	MC978												
	V _{CE(sat)}	3†	MC878												
	V _{CE(sat)}	4	MC978												
	V _{CE(sat)}	4†	MC878												
Current Leakage	I _L	14	MC978												
	I _L	14	MC878												

Ground inputs of flip-flop not under test. Other pins not listed are left open.

* = Pin 5 Data Pulse a
 † = Pin 5 Data Pulse b
 ‡ = Pin 1 Clock Pulse a
 § = Pin 1 Clock Pulse b
 ¶ = Pin 2 Data Pulse a
 See Figure 4

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MC978, MC878 (continued)

FIGURE 1 - CLOCK PULSE DEFINITION

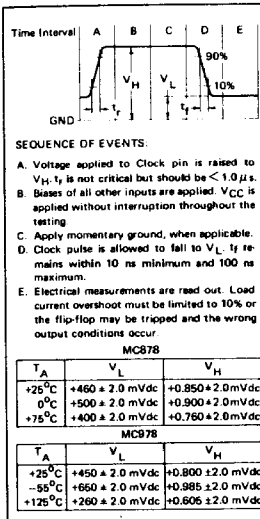


FIGURE 2 - SWITCHING TIMES TEST AND WAVEFORMS

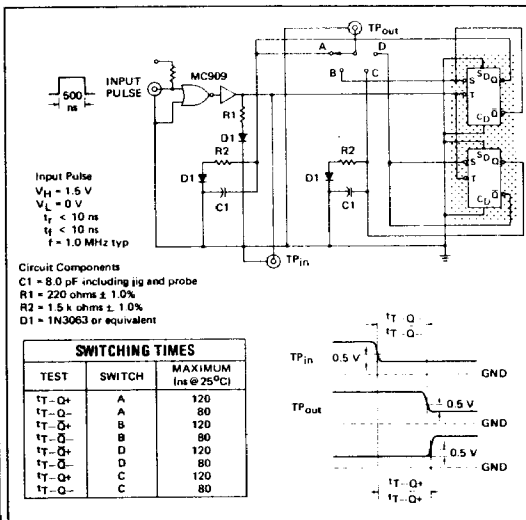


FIGURE 3A - SET UP AND RELEASE TIMES TEST CIRCUIT

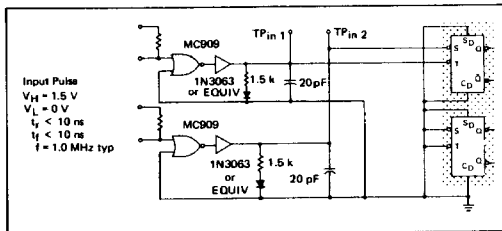


FIGURE 3B - INPUT PULSE WIDTHS FOR SET UP AND RELEASE TIMES

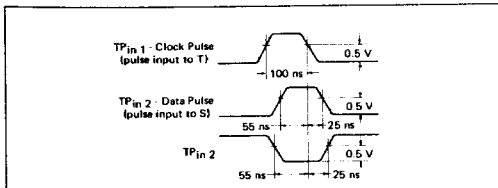
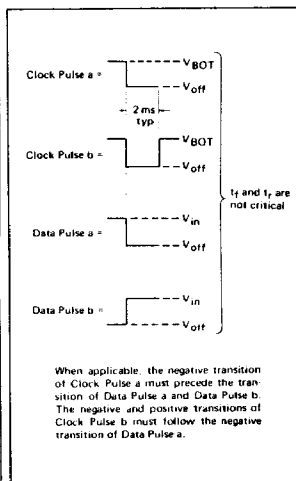


FIGURE 4 - CORRELATION OF CLOCK PULSE a & b AND DATA PULSE a & b



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Specifications

External Memory Expansion Port (Port A)

Table 2-13 DRAM Out-of-Page and Refresh Timings, Four Wait States^{1, 2} (Continued)

No.	Characteristics ³	Symbol	Expression	20 MHz ⁴		30 MHz ⁴		Unit
				Min	Max	Min	Max	
162	$\overline{\text{RAS}}$ deassertion to $\overline{\text{RAS}}$ assertion	t_{RP}	$1.75 \times T_C - 4.0$	83.5	—	54.3	—	ns
163	$\overline{\text{RAS}}$ assertion pulse width	t_{RAS}	$3.25 \times T_C - 4.0$	158.5	—	104.3	—	ns
164	$\overline{\text{CAS}}$ assertion to $\overline{\text{RAS}}$ deassertion	t_{RSH}	$1.75 \times T_C - 4.0$	83.5	—	54.3	—	ns
165	$\overline{\text{RAS}}$ assertion to $\overline{\text{CAS}}$ deassertion	t_{CSH}	$2.75 \times T_C - 4.0$	133.5	—	87.7	—	ns
166	$\overline{\text{CAS}}$ assertion pulse width	t_{CAS}	$1.25 \times T_C - 4.0$	58.5	—	37.7	—	ns
167	$\overline{\text{RAS}}$ assertion to $\overline{\text{CAS}}$ assertion	t_{RCD}	$1.5 \times T_C \pm 2$	73.0	77.0	48.0	52.0	ns
168	$\overline{\text{RAS}}$ assertion to column address valid	t_{RAD}	$1.25 \times T_C \pm 2$	60.5	64.5	39.7	43.7	ns
169	$\overline{\text{CAS}}$ deassertion to $\overline{\text{RAS}}$ assertion	t_{CRP}	$2.25 \times T_C - 4.0$	108.5	—	71.0	—	ns
170	$\overline{\text{CAS}}$ deassertion pulse width	t_{CP}	$1.75 \times T_C - 4.0$	83.5	—	54.3	—	ns
171	Row address valid to $\overline{\text{RAS}}$ assertion	t_{ASR}	$1.75 \times T_C - 4.0$	83.5	—	54.3	—	ns
172	$\overline{\text{RAS}}$ assertion to row address not valid	t_{RAH}	$1.25 \times T_C - 4.0$	58.5	—	37.7	—	ns
173	Column address valid to $\overline{\text{CAS}}$ assertion	t_{ASC}	$0.25 \times T_C - 4.0$	8.5	—	4.3	—	ns
174	$\overline{\text{CAS}}$ assertion to column address not valid	t_{CAH}	$1.75 \times T_C - 4.0$	83.5	—	54.3	—	ns
175	$\overline{\text{RAS}}$ assertion to column address not valid	t_{AR}	$3.25 \times T_C - 4.0$	158.5	—	104.3	—	ns
176	Column address valid to $\overline{\text{RAS}}$ deassertion	t_{RAL}	$2 \times T_C - 4.0$	96.0	—	62.7	—	ns
177	$\overline{\text{WR}}$ deassertion to $\overline{\text{CAS}}$ assertion	t_{RCS}	$1.5 \times T_C - 3.8$	71.2	—	46.2	—	ns
178	$\overline{\text{CAS}}$ deassertion to $\overline{\text{WR}}$ assertion	t_{RCH}	$0.75 \times T_C - 3.7$	33.8	—	21.3	—	ns
179	$\overline{\text{RAS}}$ deassertion to $\overline{\text{WR}}$ assertion	t_{RRH}	$0.25 \times T_C - 3.7$	8.8	—	4.6	—	ns

Preliminary Data