



74BCT373

Octal Transparent Latch with TRI-STATE® Outputs

General Description

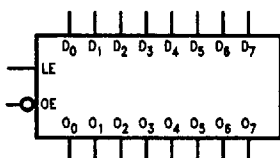
The 74BCT373 consists of eight latches with TRI-STATE outputs for bus oriented applications. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup times is latched. Data appears on the bus when the Output Enable (\overline{OE}) is LOW. When \overline{OE} is HIGH the bus output is in the high impedance state.

Features

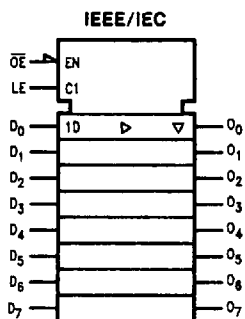
- Eight latches in a single package
- TRI-STATE outputs for bus interfacing
- Nondestructive hot insertion capability
- High impedance in power down (I_{ZZ} and V_{ID})
- Guaranteed 4000V minimum ESD protection
- Guaranteed output skew
- Guaranteed multiple output switching specifications
- Guaranteed latchup protection
- Low I_{CCZ} through BiCMOS techniques

Ordering Code: See Section 11

Logic Symbols



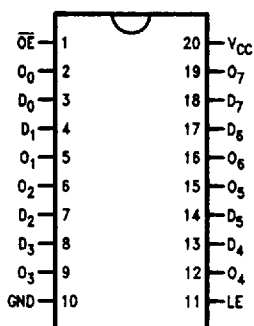
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Connection Diagram

Pin Assignment for DIP and SOIC



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| Pin Names | Description |
|--------------------------------|----------------------------------|
| D ₀ -D ₇ | Data Inputs |
| LE | Latch Enable Input (Active HIGH) |
| \overline{OE} | Output Enable Input (Active LOW) |
| O ₀ -O ₇ | TRI-STATE Latch Outputs |

Functional Description

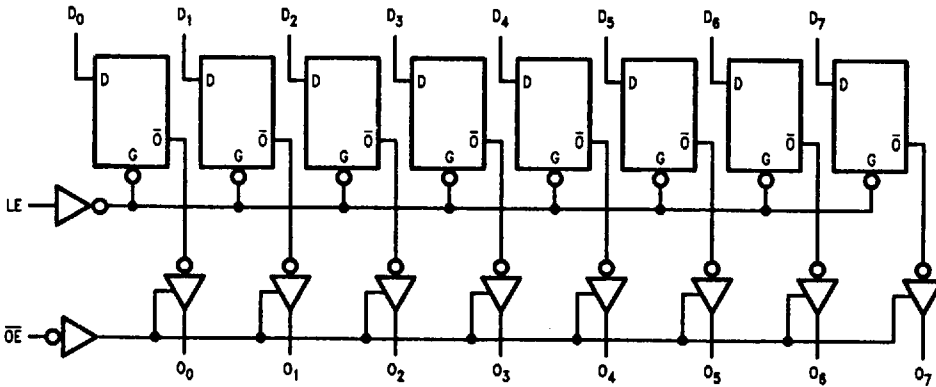
The 'BCT373 contains eight D-type latches with TRI-STATE output buffers. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW, the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The TRI-STATE buffers are controlled by the Output Enable (\overline{OE}) input. When \overline{OE} is LOW, the buffers are in the bi-state mode. When \overline{OE} is HIGH the buffers are in the high impedance mode but this does not interfere with entering new data into the latches.

Truth Table

| Inputs | | | Output |
|--------|-----------------|-------|-------------------|
| LE | \overline{OE} | D_n | O_n |
| H | L | H | H |
| H | L | L | L |
| L | L | X | O_n (no change) |
| X | H | X | Z |

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial
 Z = High Impedance State

Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | |
|---|-------------------|
| Storage Temperature | -65°C to +150°C |
| Ambient Temperature under Bias | -55°C to +125°C |
| Junction Temperature under Bias Plastic | -55°C to +150°C |
| V _{CC} Pin Potential to Ground Pin | -0.5V to +7.0V |
| Input Voltage (Note 2) | -0.5V to +7.0V |
| Input Current (Note 2) | -30 mA to +5.0 mA |

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

| | |
|---|--|
| Voltage Applied to Any Output in the Disable or Power-Off State in the High State | -0.5V to +5.5V -0.5V to V _{CC} |
| Current Applied to Output in LOW State (Max) | Twice the Rated I _{OL} (mA) |
| ESD Last Passing Voltage (Min) | 4000V |
| DC Latchup Source Current | 500 mA |
| Over Voltage Latchup | V _{CC} + 4.5V |

Recommended Operating Conditions

| | |
|---|----------------|
| Free Air Ambient Temperature Commercial | 0°C to +70°C |
| Supply Voltage Commercial | +4.5V to +5.5V |

DC Electrical Characteristics

| Symbol | Parameter | 74BCT | | | Units | V _{CC} | Conditions |
|------------------|-----------------------------------|------------|-----|------|-------|-----------------|---|
| | | Min | Typ | Max | | | |
| V _{IH} | Input HIGH Voltage | 2.0 | | | V | | Recognized as a HIGH Signal |
| V _{IL} | Input LOW Voltage | | | 0.8 | V | | Recognized as a LOW Signal |
| V _{CD} | Input Clamp Diode Voltage | | | -1.2 | V | Min | I _{IN} = -18 mA |
| V _{OH} | Output HIGH Voltage | 2.4 2.0 | | | V | Min | I _{OH} = -3 mA I _{OH} = -15 mA |
| V _{OL} | Output LOW Voltage | | | 0.55 | V | Min | I _{OL} = 64 mA |
| I _{IH} | Input HIGH Current | | | 5 | μA | Max | V _{IN} = 2.7V |
| I _{BVI} | Input HIGH Current Breakdown Test | | | 7 | μA | Max | V _{IN} = 7.0V |
| I _{IL} | Input LOW Current | | | -250 | μA | Max | V _{IN} = 0.5V |
| I _{OZH} | Output Leakage Current | | | 20 | μA | Max | V _{OUT} = 2.7V |
| I _{OZL} | Output Leakage Current | | | -20 | μA | Max | V _{OUT} = 0.5V |
| I _{OS} | Output Short-Circuit Current | -100 | | -225 | mA | Max | V _{OUT} = 0V |
| I _{CEx} | Output HIGH Leakage Current | | | 50 | μA | Max | V _{OUT} = V _{CC} |
| V _{ID} | Input Leakage Test | 4.75 | | | V | 0.0 | I _{ID} = 1.9 μA All Other Pins Grounded |
| I _{ZZ} | Bus Drainage Test | | | 100 | μA | 0.0V | V _{OUT} = 5.25V |
| I _{CCH} | Power Supply Current | | | 8 | mA | Max | V _O = HIGH |
| I _{CCL} | Power Supply Current | | | 30 | mA | Max | V _O = LOW |
| I _{CCZ} | Power Supply Current | | | 10 | mA | Max | V _O = HIGH Z |

AC Electrical Characteristics: See Section 8 for Waveforms and Load Configurations

| Symbol | Parameter | 74BCT | | | 74BCT | | Units | Fig. No. |
|--------------------------------------|---|---|-----|------|---|------|-------|----------|
| | | T _A = +25°C V _{CC} = +5.0V C _L = 50 pF | | | T _A = Com V _{CC} = Com C _L = 50 pF | | | |
| | | Min | Typ | Max | Min | Max | | |
| t _{PLH} t _{PHL} | Propagation Delay Data to Output | 2.0 | | 9.3 | 2.0 | 9.3 | ns | 8-3 |
| t _{PLH} t _{PHL} | Propagation Delay LE to O _n | 2.0 | | 10.3 | 2.0 | 10.3 | ns | 8-3 |
| t _{PZH} t _{PZL} | Output Enable Time | 2.0 | | 11.8 | 2.0 | 11.8 | ns | 8-5 |
| t _{PHZ} t _{PLZ} | Output Disable Time | 2.0 | | 6.9 | 2.0 | 6.9 | ns | 8-5 |
| | | 2.0 | | 6.1 | 2.0 | 6.1 | | |

AC Electrical Characteristics: See Section 8 for Waveforms

| Symbol | Parameter | 74BCT | | 74BCT | | Units | Fig. No. | |
|--|---|---|-----|--|-----|-------|----------|-----|
| | | T _A = +25°C V _{CC} = +5.0V | | T _A , V _{CC} = Com | | | | |
| | | Min | Max | Min | Max | | | |
| t _s (H) t _s (L) | Setup Time, HIGH or LOW D _n to LE | 5.9 | | 5.9 | | | ns | 8-6 |
| t _h (H) t _h (L) | Hold Time, HIGH or LOW D _n to LE | 1.5 | | 1.5 | | | | |
| t _w (H) | LE Pulse Width, HIGH | 3.0 | | 3.0 | | | | |

Extended AC Electrical Characteristics: See Section 8

| Symbol | Parameter | 74BCT | | 74BCT | | Units | Fig. No. |
|--------------------------------------|-------------------------------------|--|------|--|------|-------|----------|
| | | T _A = Com V _{CC} = Com C _L = 50 pF 8 Outputs Switching (Note 3) | | T _A = Com V _{CC} = Com C _L = 250 pF (Note 4) | | | |
| | | Min | Max | Min | Max | | |
| t _{PLH} t _{PHL} | Propagation Delay Data to Output | 2.0 | 10.5 | 2.0 | 11.8 | ns | 8-3 |
| | | 2.0 | 13.0 | 2.0 | 14.0 | | |

Note 3: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all low-to-high, high-to-low, etc.).

Note 4: This specification is guaranteed but not tested. The limits represent propagation delays with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load. This specification pertains to single output switching only.

Capacitance

| Symbol | Parameter | Typ | Units | Conditions |
|------------------|------------------------|-----|-------|------------------------|
| C _{IN} | Input Pin Capacitance | 5 | pF | V _{CC} = 5.0V |
| C _{OUT} | Output Pin Capacitance | 8 | pF | V _{CC} = 5.0V |