

## MSM56V16160K

2-Bank×524,288-Word×16-Bit SYNCHRONOUS DYNAMIC RAM

### DESCRIPTION

The MSM56V16160K is a 2-Bank × 524,288-word × 16-bit Synchronous dynamic RAM. The device operates at 3.3V. The inputs and outputs are LVTTL compatible.

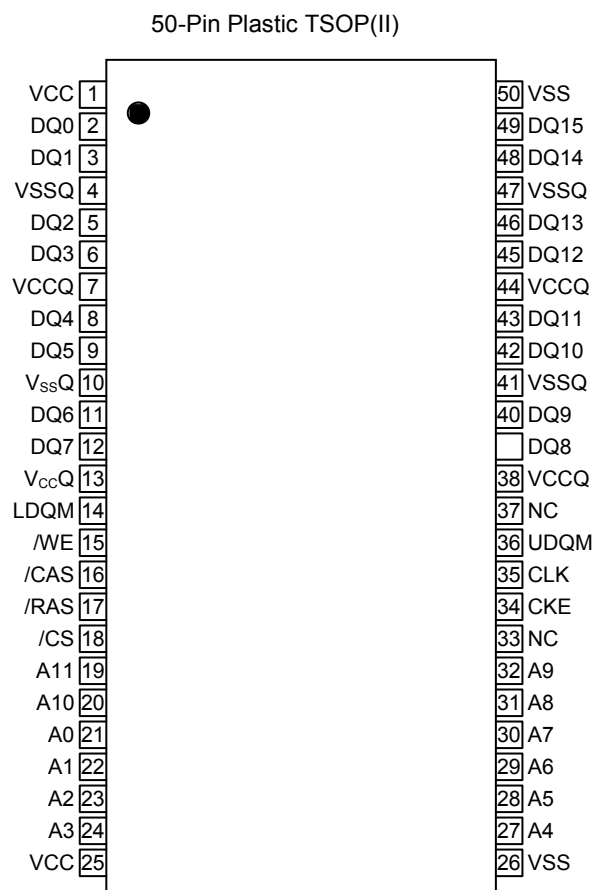
### FEATURES

Product Name	MSM56V16160K
Organization	2Bank x 524,288Word x 16Bit
Address Size	2,048Row x 256Column
Power Supply VCC (Core)	3.3V±0.3V
Power Supply VCCQ (I/O)	3.3V±0.3V
Interface	LVTTL compatible
Operating Frequency	Max. 125MHz (Speed Rank 8)
Operating Temperature	0 to 70°C
/CAS Latency	2, 3
Burst Length	1, 2, 4, 8, Full page
Burst Type	Sequential, Interleave
Write Mode	Burst, Single
Refresh	Auto-Refresh, 4,096cycle/64ms, Self-Refresh
Package	50-Pin Plastic TSOP(II) (Cu frame) (P-TSOP150-P-400-0.80-ZK)

### PRODUCT FAMILY

Family	Max. Frequency	Access Time (Max.)	
		tAC2	tAC3
MSM56V16160K-8	125MHz	6ns	6ns
MSM56V16160K-10	100MHz	6ns	6ns

## PIN CONFIGURATION (TOP VIEW)



Pin Name	Function	Pin Name	Function
CLK	System Clock	UDQM, LDQM	Data Input / Output Mask
/CS	Chip Select	DQi	Data Input / Output
CKE	Clock Enable	VCC	Power Supply (3.3V)
A0–A10	Address	VSS	Ground (0V)
A11	Bank Select Address	VCCQ	Data Output Power Supply (3.3V)
/RAS	Row Address Strobe	VSSQ	Data Output Ground (0V)
/CAS	Column Address Strobe	NC	No Connection
/WE	Write Enable		

Note : The same power supply voltage must be provided to every VCC pin .

The same power supply voltage must be provided to every VCCQ pin.

The same GND voltage level must be provided to every VSS pin and VSSQ pin.

**PIN DESCRIPTION**

CLK	Clock (Input) Fetches all inputs at the "H" edge.
CKE	Clock Enable (Input) Masks system clock to deactivate the subsequent CLK operation. If CKE is deactivated, system clock will be masked so that the subsequent CLK operation is deactivated. CKE should be asserted at least one cycle prior to a new command.
/CS	Chip Select (Input) Disables or enables device operation by asserting or deactivating all inputs except CLK, CKE and UDQM, LDQM.
/RAS	Row Address Strobe (Input) Functionality depends on the combination with other signals. For detail, see the function truth table.
/CAS	Column Address Strobe (Input) Functionality depends on the combination with other signals. For detail, see the function truth table.
/WE	Write Enable (Input) Functionality depends on the combination with other signals. For detail, see the function truth table.
A11	Bank Address (Input) Selects bank to be activated during row address latch time and selects bank for precharge and read/write during column address latch time.
A10 to A0	Row & column multiplexed. (Input) Row address : RA0 – RA10 Column Address : CA0 – CA7
DQ15 to DQ0	3-state Data Bus (Input/Output)
UDQM, LDQM	DQ Mask (Input) Masks the read data of two clocks later when DQM are set "H" at the "H" edge of the clock signal. Masks the write data of the same clock when DQM are set "H" at the "H" edge of the clock signal. UDQM controls DQ15 to DQ8, LDQM controls DQ7 to DQ0.
VCC, VSS	Power Supply (Core), Ground (Core) The same power supply voltage must be provided to every VCC pin. The same GND voltage level must be provided to every VSS pin.
VCCQ, VSSQ	Power Supply (I/O), Ground (I/O) The same power supply voltage must be provided to every VCCQ pin. The same GND voltage level must be provided to every VSSQ pin.
NC	No Connection

**ELECTRICAL CHARACTERISTICS****Absolute Maximum Ratings**

Parameter	Symbol	Value	Unit
Voltage on Input/Output Pin Relative to VSS	VIN, VOUT	-0.5 to VCC+0.5	V
VCC Supply Voltage	VCC	-0.5 to 4.6	V
VCCQ Supply Voltage	VCCQ	-0.5 to 4.6	V
Power Dissipation (Ta=25°C)	PD	1000	mW
Short Circuit Output Current	IOS	50	mA
Storage Temperature	Tstg	-55 to 150	°C
Operating Temperature	Topr	0 to 70	°C

- Notes: 1. Permanent device damage may occur if Absolute Maximum Ratings are exceeded.  
 2. Functional operation should be restricted to recommended operating condition.  
 3. Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

**Recommended Operating Conditions (1/2)**

Voltages referenced to VSS = 0 V

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Power Supply Voltage (Core)	VCC	3.0	3.3	3.6	V	1
Power Supply Voltage (I/O)	VCCQ	3.0	3.3	3.6	V	1
Ground	VSS, VSSQ	0	0	0	V	

- Notes: 1. The voltages are referenced to VSS

**Recommended Operating Conditions (2/2)**

Ta= 0 to 70°C

Parameter	Symbol	Min.	Max.	Unit	Note
Input High Voltage	VIH	2.0	VCC + 0.2	V	1, 2
Input Low Voltage	VIL	-0.3	0.8	V	1, 3

- Notes: 1. The voltages are referenced to VSS.  
 2. The input voltage is VCC + 0.5V when the pulse width is less than 20ns (the pulse width is with respect to the point at which VCC is applied).  
 3. The input voltage is - 0.5V when the pulse width is less than 20ns (the pulse width respect to the point at which VSS and VSSQ are applied).

**Pin Capacitance**

Ta = 25°C, VCC=VCCQ=3.3V, f=1MHz

Parameter	Symbol	Min.	Max.	Unit
Input Capacitance (CLK)	CCLK	—	4	pF
Input Capacitance (A0 – A11, /RAS, /CAS, /WE, /CS, CKE, UDQM, LDQM)	CIN	—	5	pF
Input/Output Capacitance (DQ15 – DQ0)	COUT	—	6.5	pF

**DC Characteristics (Input/Output)**Ta = 0 to 70°C  
VCC = VCCQ = 3.3V±0.3V

Parameter	Symbol	Condition	Min.	Max.	Unit
Output High Voltage	VOH	IOH = -0.2mA	2.4	—	V
Output Low Voltage	VOL	IOL = 0.2mA	—	0.4	V
Input Leakage Current	ILI	0V ≤ VIN ≤ VCCQ	-10	10	μA
Output Leakage Current	ILO	—	-10	10	μA

Note : The voltages are referenced to VSS.

**DC Characteristics (Power Supply Current)**

Ta = 0 to 70°C  
VCC = VCCQ = 3.3V±0.3V

Parameter	Symbol	Condition			MSM56V16160K		Unit	Note
					-8	-10		
		Bank	CKE	Other	Max.	Max.		
Average Power Supply Current (Operating)	ICC1	One Bank Active	CKE ≥ VIH t <sub>CC</sub> = Min. t <sub>RC</sub> = Min. No Burst		80	70	mA	1, 2
Power Supply Current (Standby)	ICC2	Both Banks Precharge	CKE ≥ VIH	t <sub>CC</sub> = Min.	35	30	mA	3
Average Power Supply Current (Clock Suspension)	ICC3S	Both Banks Active	CKE ≤ VIL	t <sub>CC</sub> = Min.	3	3	mA	2
Average Power Supply Current (Active Standby)	ICC3	One Bank Active	CKE ≥ VIH	t <sub>CC</sub> = Min.	40	35	mA	3
Power Supply Current (Burst)	ICC4	Both Banks Active	CKE ≥ VIH	t <sub>CC</sub> = Min.	120	100	mA	1, 2
Power Supply Current (Auto-Refresh)	ICC5	One Bank Active	CKE ≥ VIH	t <sub>CC</sub> = Min. t <sub>RC</sub> = Min.	120	100	mA	2
Average Power Supply Current (Self-Refresh)	ICC6	Both Banks Precharge	CKE ≤ VIL	t <sub>CC</sub> = Min.	2	2	mA	
Average Power Supply Current (Power Down)	ICC7	Both Banks Precharge	CKE ≤ VIL	t <sub>CC</sub> = Min.	2	2	mA	

- Notes: 1. Measured with outputs open.  
2. The address and data can be changed once or left unchanged during one cycle.  
3. The address and data can be changed once or left unchanged during two cycles.

**MSM56V16160K****AC Characteristics (1/4)**

Ta = 0 to 70°C  
VCC = VCCQ = 3.3V±0.3V  
Note1,2

Parameter		Symbol	MSM56V16160K				Unit	Note
			-8		-10			
			Min.	Max.	Min.	Max.		
Clock Cycle Time	CL=3	t <sub>CC3</sub>	8	—	10		ns	
	CL=2	t <sub>CC2</sub>	10	—	10		ns	
Access Time from Clock	CL=3	t <sub>AC3</sub>	—	6	—	6	ns	3, 4
	CL=2	t <sub>AC2</sub>	—	6	—	6	ns	3, 4
Clock High Pulse Time		t <sub>CH</sub>	3	—	3	—	ns	4
Clock Low Pulse Time		t <sub>CL</sub>	3	—	3	—	ns	4
Input Setup Time		t <sub>SI</sub>	2	—	2	—	ns	
Input Hold Time		t <sub>HI</sub>	1	—	1	—	ns	
Output Low Impedance Time from Clock		t <sub>OLZ</sub>	2	—	2	—	ns	
Output High Impedance Time from Clock		t <sub>OHZ</sub>	—	6	—	6	ns	
Output Hold from Clock		t <sub>OH</sub>	2	—	2	—	ns	3
Random Read or Write Cycle Time		t <sub>RC</sub>	70	—	70	—	ns	
RAS Precharge Time		t <sub>RP</sub>	20	—	20	—	ns	
RAS Pulse Width		t <sub>RAS</sub>	50	10 <sup>5</sup>	50	10 <sup>5</sup>	ns	
/RAS to /CAS Delay Time		t <sub>RCD</sub>	20	—	20	—	ns	
Write Recovery Time		t <sub>WR</sub>	2	—	2	—	Cycle	6
/RAS to /RAS Bank Active Delay Time		t <sub>R RD</sub>	20	—	20	—	ns	
Refresh Time		t <sub>REF</sub>	—	64	—	64	ms	5
Power-down Exit setup Time		t <sub>PDE</sub>	t <sub>SI</sub> +1CLK	—	t <sub>SI</sub> +1CLK	—	ns	
Refresh cycle Time		t <sub>RCA</sub>	70	—	70	—	ns	

**MSM56V16160K**

**Refresh Time**

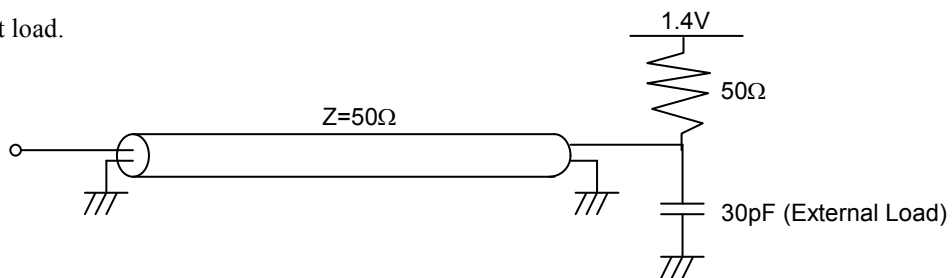
Ta = 0 to 70°C  
 VCC = VCCQ = 3.3V±0.3V  
 Note1,2

Parameter	Symbol	MSM56V16160K		Unit	Note
		-8	-10		
/CAS to /CAS Delay Time (Min.)	t <sub>CCD</sub>	1	1	Cycle	
Clock Disable Time from CKE	t <sub>CKE</sub>	1	1	Cycle	
Data Output High Impedance Time from UDQM, LDQM	t <sub>DOZ</sub>	2	2	Cycle	
Data Input Mask Time from UDQM, LDQM	t <sub>DOD</sub>	0	0	Cycle	
Data Input Mask Time from Write Command	t <sub>DWD</sub>	0	0	Cycle	
Data Output High Impedance Time from Precharge Command	t <sub>ROH</sub>	CL	CL	Cycle	
Active Command Input Time from Mode Register Set Command Input (Min.)	t <sub>MRD</sub>	2	2	Cycle	
Write Command Input Time from Output	t <sub>OWD</sub>	2	2	Cycle	

- Notes: 1. AC measurements assume that t<sub>T</sub> = 1ns.,  
 2. Test condition

Parameter	Test Condition		Unit
Input voltage for AC measurement	2.4	0.4	V
Transition Time for AC measurement	t <sub>T</sub> = 1		ns
Reference level for timing of input signal (t <sub>T</sub> ≤ 1ns)	1.4		V
Reference level for timing of input signal (t <sub>T</sub> > 1ns)	V <sub>IH</sub> Min.	V <sub>IL</sub> Max.	V
Reference level for timing of output signal	1.4		V

3. Output load.



4. If t<sub>T</sub> is longer than 1ns, then the reference level for timing of input signals is V<sub>IH</sub> and V<sub>IL</sub>.  
 5. It is necessary to operate auto-refresh 4096 cycles within t<sub>REF</sub>.  
 6. If t<sub>CC</sub> is longer than 20ns, the spec of t<sub>WR</sub> (min.) is 20ns (1 cycle).



## POWER ON AND INITIALIZE



**Power on Sequence**

1. Apply power and attempt to maintain CKE="H" and other pins are NOP condition at the input.
2. Maintain stable power, stable clock and NOP input condition for a minimum of 200  $\mu$ s.
3. Issue precharge commands for all banks of the devices.
4. Issue 2 or more auto-refresh commands.
5. Issue mode register set command to initialize the mode register.
6. Issue extended mode register set command to initialize the extended mode register.

**Mode Register Set Command (MRS)**

The mode register stores the data for controlling the various operating modes. It programs the /CAS latency, burst type, burst length and write mode. The default value of the mode register is not defined, therefore the mode register must be written after power up to operate the SDRAM. The mode register is written by mode register set command MRS. The state of address pins A10 to A0 in the same cycle as MRS is the data written in the mode register. Refer to the table for specific codes for various /CAS latencies, burst type, burst length and write mode.

MRS

CLK	 n-1	 n
CKE	H	<b>X</b>
/CS	X (Idle)	<b>L</b>
/RAS		<b>L</b>
/CAS		<b>L</b>
/WE		<b>L</b>
A11		<b>L</b>
A10~A0	V	<b>V</b>

V: The value of mode register set

**Mode Register Field Table To Program Mode**

Write Burst Mode		/CAS Latency				Burst Type		Burst Length				
A9	WM	A6	A5	A4	CL	A3	BT	A2	A1	A0	BT = 0	BT = 1
0	Burst	0	0	0	Reserved	0	Sequential	0	0	0	1	1
1	Single	0	0	1	Reserved	1	Interleave	0	0	1	2	2
		0	1	0	2			0	1	0	4	4
		0	1	1	3			0	1	1	8	8
		1	0	0	Reserved			1	0	0	Reserved	Reserved
		1	0	1	Reserved			1	0	1	Reserved	Reserved
		1	1	0	Reserved			1	1	0	Reserved	Reserved
		1	1	1	Reserved			1	1	1	Full Page	Reserved

- Notes:
1. A11 should stay "L" during mode set cycle.
  2. A7, A8 and A10 should stay "L" during mode set cycle.
  3. Don't set address keys of "Reserved".

**Burst Mode**

Burst operation is the operation to continuously increase a column address inputted during read or write command. The upper bits select a column address block,

		Access order in column address block					
		Start Address (Lower bit)		Burst Type			
				BT=Sequential		BT=Interleave	
Burst Length	BL=2			A0			
				0	0, 1	0, 1	
				1	1, 0	1, 0	
	BL=4			A1	A0		
				0	0	0, 1, 2, 3	0, 1, 2, 3
				0	1	1, 2, 3, 0	1, 0, 3, 2
				1	0	2, 3, 0, 1	2, 3, 0, 1
				1	1	3, 0, 1, 2	3, 2, 1, 0
	BL=8	A2	A1	A0			
		0	0	0	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7	
		0	0	1	1, 2, 3, 4, 5, 6, 7, 0	1, 0, 3, 2, 5, 4, 7, 6	
		0	1	0	2, 3, 4, 5, 6, 7, 0, 1	2, 3, 0, 1, 6, 7, 4, 5	
		0	1	1	3, 4, 5, 6, 7, 0, 1, 2	3, 2, 1, 0, 7, 6, 5, 4	
		1	0	0	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3	
		1	0	1	5, 6, 7, 0, 1, 2, 3, 4	5, 4, 7, 6, 1, 0, 3, 2	
		1	1	0	6, 7, 0, 1, 2, 3, 4, 5	6, 7, 4, 5, 2, 3, 0, 1	
		1	1	1	7, 0, 1, 2, 3, 4, 5, 6	7, 6, 5, 4, 3, 2, 1, 0	
	BL=Full Page (256)	A7~A0					
		0			0, 1... 255	Non Support	
		Yn			Yn, Yn+1... 255, 0... ...Yn-1		

**READ / WRITE OPERATION**

**Bank**

This SDRAM is organized as four independent banks of 524,288 words x 16 bits memory arrays. The A11 input is latched at the time of assertion of /RAS and /CAS to select the bank to be used for operation. The bank address A11 is latched at bank active, read, write, mode register set and precharge operations.

Bank Address

A11	Bank
0	A
1	B

**Activate**

The bank activate command is used to select a random row in an idle bank. By asserting low on /RAS and /CS with desired row and bank address, a row access is initiated. The read or write operation can occur after a time delay of tRCD(min) from the time of bank activation.

ACT

CLK	$\overline{\uparrow}_{n-1}$	$\overline{\uparrow}_n$
CKE	H	X
/CS	X (Idle)	L
/RAS		L
/CAS		H
/WE		H
A11	X	BA
A10~A0	X	RA

BA: Bank Address

RA: Row Address (Page)

**Precharge**

The precharge operation is performed on an active bank by precharge command (PRE) with valid A11 of the bank to be precharged. The precharge command can be asserted anytime after tRAS(min) is satisfied from the bank active command in the desired bank. All bank can precharged at the same time by using precharge all command (PALL). Asserting low on /CS, /RAS and /WE with high on A10

PRE

CLK	$\overline{\uparrow}_{n-1}$	$\overline{\uparrow}_n$
CKE	H	X
/CS	X (Page Open)	L
/RAS		L
/CAS		H
/WE		L
A11	X	BA
A10	X	0
A9~A0	X	X

BA: Bank Address

PALL

CLK	$\overline{\uparrow}_{n-1}$	$\overline{\uparrow}_n$
CKE	H	X
/CS	X (Page Open)	L
/RAS		L
/CAS		H
/WE		L
A11	X	X
A10	X	1
A9~A0	X	X

after all banks have satisfied tRAS(min) requirement, performs precharge on al banks. At the end of tRP after performing precharge to all banks, all banks are in idle state.

### Write / Write with Auto-Precharge

The write command is used to write data into the SDRAM on consecutive clock cycles in adjacent address depending on burst length and burst sequence. By asserting low on /CS, /CAS and /WE with valid column address, a write burst is initiated. The data inputs are provided for the initial address in the same clock cycle as the burst write command. The input buffer is deselected at the end of the burst length, even through the internal writing can be completed yet. The writing can be completed by issuing a burst read and DQM for blocking data inputs or burst write in the same or another active bank. The burst stop command is valid at every burst length.

**WRT**

CLK	$\uparrow_{n-1}$	$\uparrow_n$
CKE	H	X
/CS	X (Page Open)	L
/RAS		H
/CAS		L
/WE		L
A11	X	BA
A10	X	0
A9, A8	X	X
A7~A0	X	CA
DQ	X	D-in

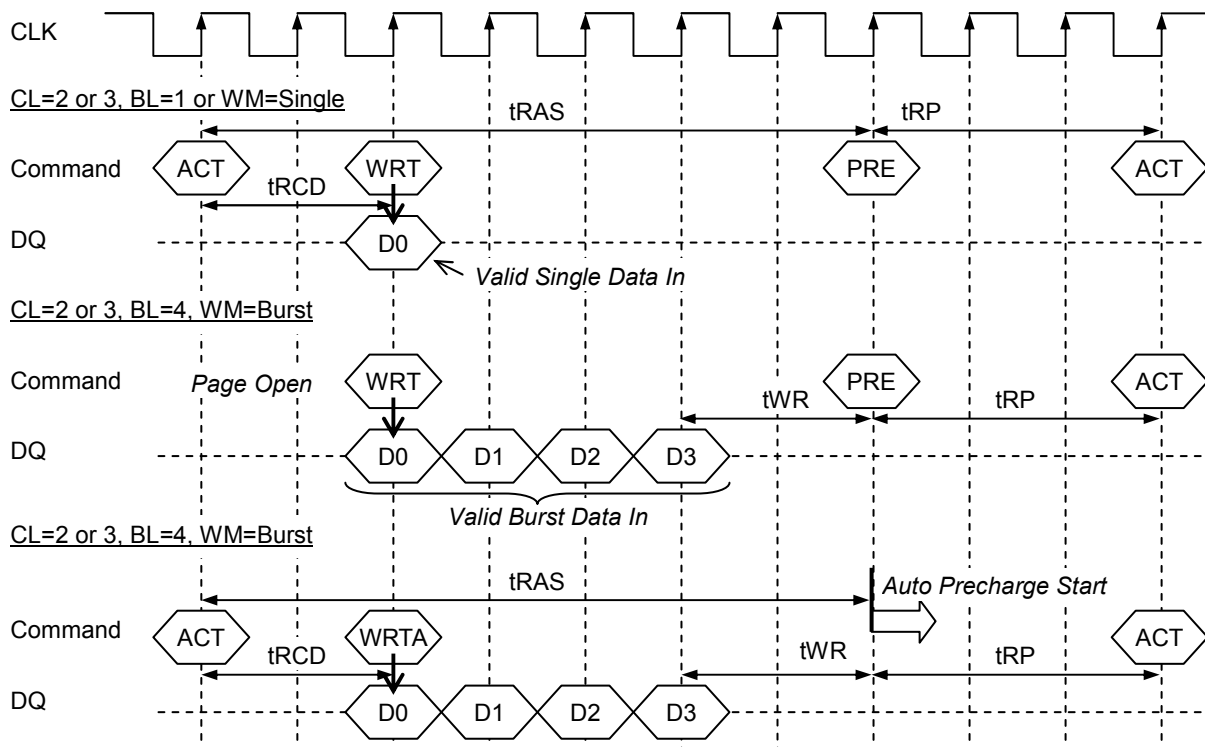
BA: Bank Address  
CA: Column Address  
D-in: Data inputs

**WRTA**

CLK	$\uparrow_{n-1}$	$\uparrow_n$
CKE	H	X
/CS	X (Page Open)	L
/RAS		H
/CAS		L
/WE		L
A11	X	BA
A10	X	1
A9, A8	X	X
A7~A0	X	CA
DQ	X	D-in

BA: Bank Address  
CA: Column Address  
D-in: Data inputs

### Write Cycle



**Read / Read with Auto-Precharge**

The read command is used to access burst of data on consecutive clock cycles from an active row in an active bank. The read command is issued by asserting low on /CS and /CAS with /WE being high on the positive edge of the clock. The bank must be active for at least tRCD(min) before the read command is issued. The first output appears in /CAS latency number of clock cycles after the issue of read command. The burst length, burst sequence and latency from the read command are determined by the mode register that is already programmed.

**RD**

CLK	$\uparrow_{n-1}$	$\uparrow_n$
CKE	H	X
/CS	X	L
/RAS	X (Page Open)	H
/CAS	X	L
/WE	X	H
A11	X	BA
A10	X	0
A9, A8	X	X
A7~A0	X	CA
DQ	X	X

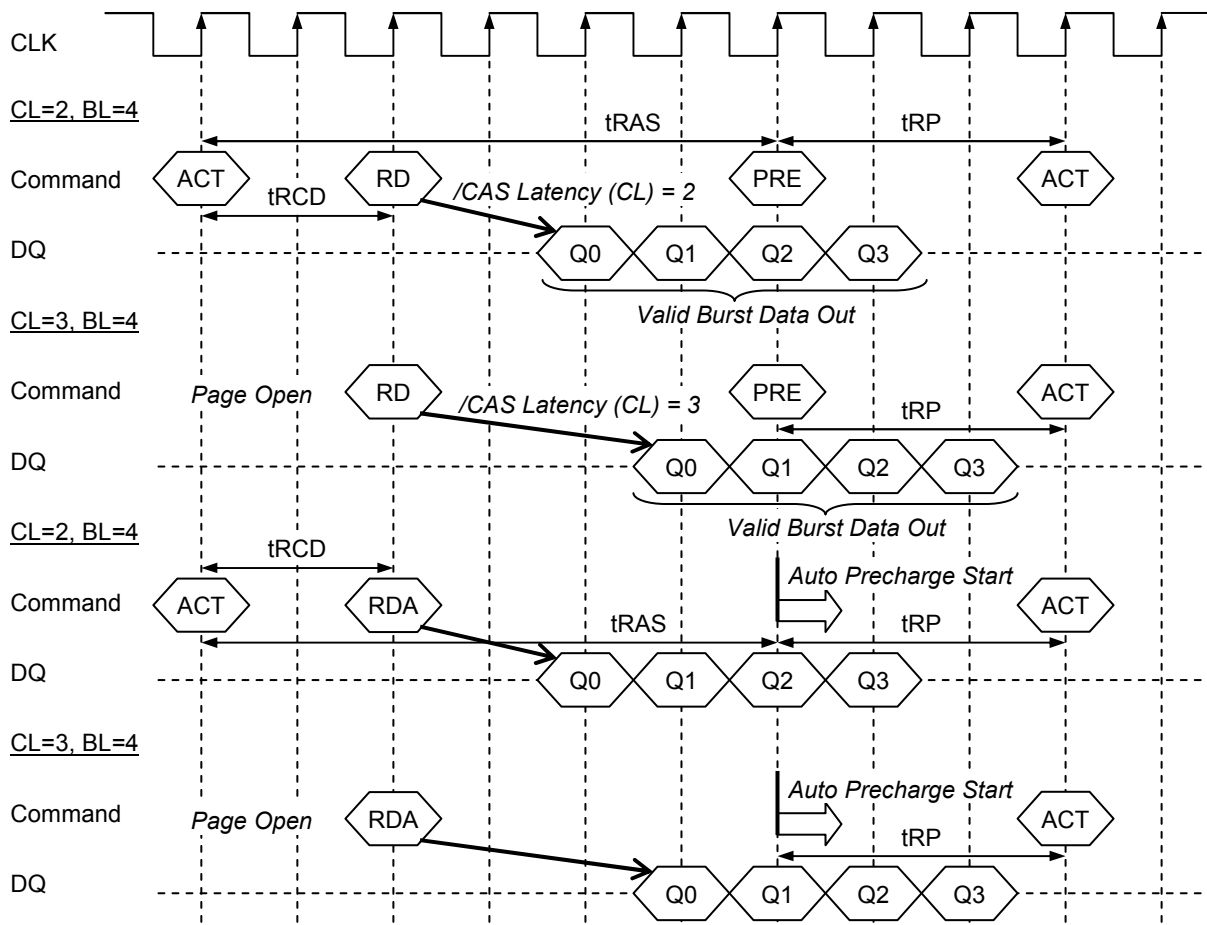
BA: Bank Address  
CA: Column Address

**RDA**

CLK	$\uparrow_{n-1}$	$\uparrow_n$
CKE	H	X
/CS	X	L
/RAS	X (Page Open)	H
/CAS	X	L
/WE	X	H
A11	X	BA
A10	X	1
A9, A8	X	X
A7~A0	X	CA
DQ	X	X

BA: Bank Address  
CA: Column Address

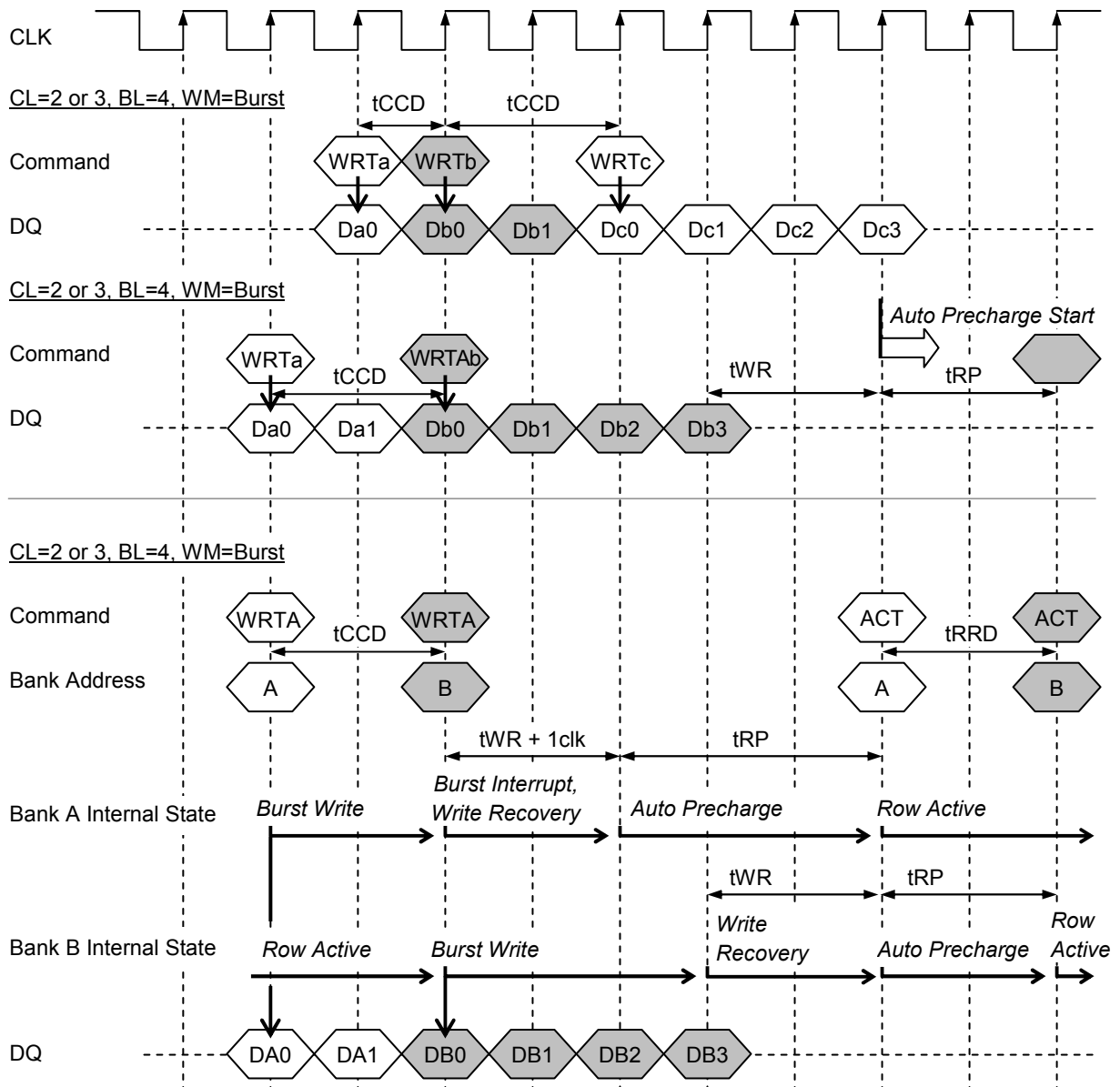
Read Cycle



**Write / Write interrupt**

When a new write command is issued to same bank during write cycle or another active bank, current burst write is terminated and new burst write start. When a new write command is issued to another bank during a write with auto-precharge cycle, current burst is terminated and a new write command start. Then, current bank is precharged after specified time. Don't issue a new write command to same bank during write with auto-precharge cycle.

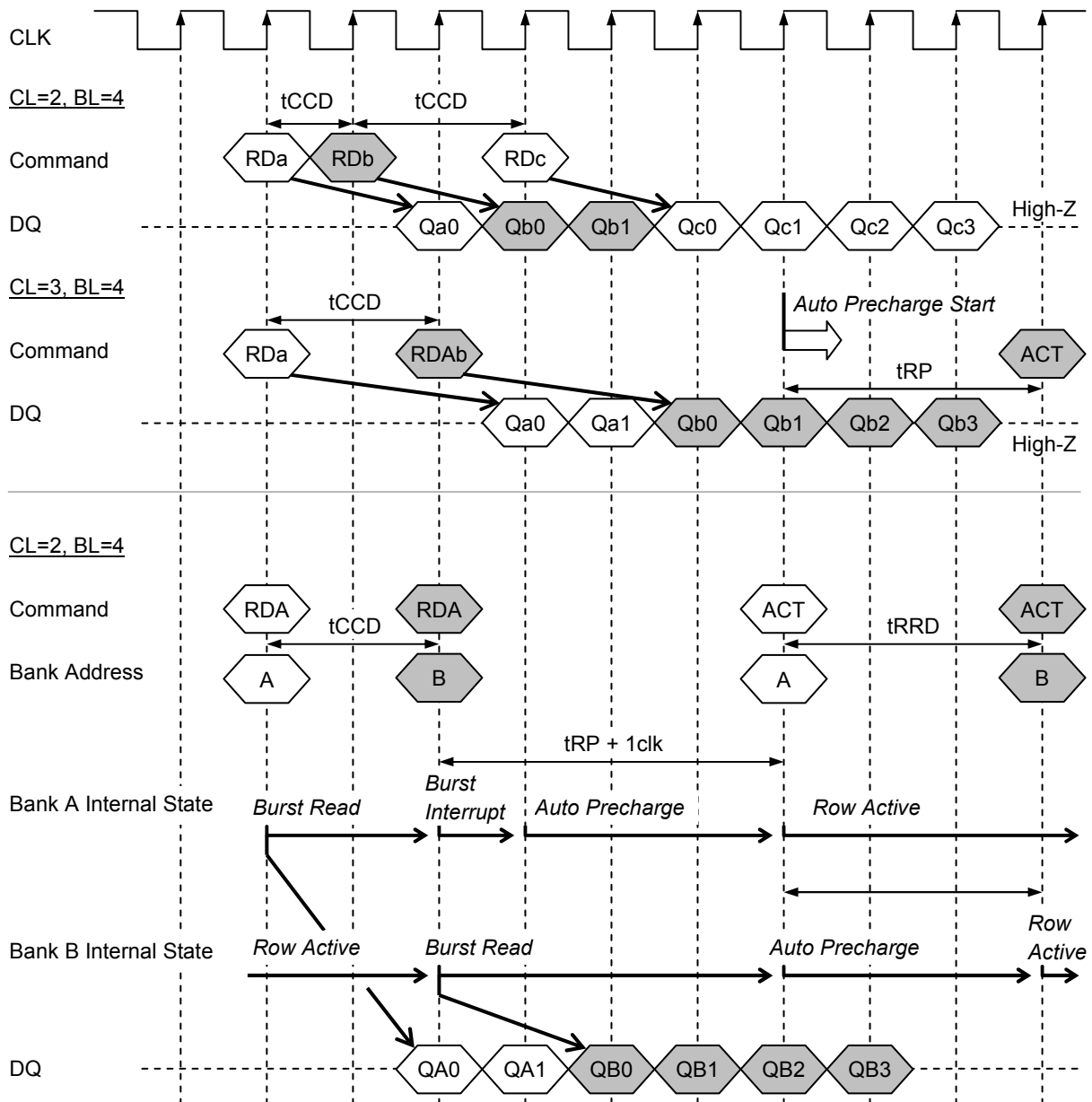
Write / Write interrupt cycle



**Read / Read interrupt**

When a new read command is issued to same bank during read cycle or another active bank, current burst read is terminated after the cycle same as /CAS latency and new burst read start. When a new read command is issued to another bank during a read with auto-precharge cycle, current burst is terminated after the cycle same as /CAS latency and a new read command start. Then, current bank is precharged after specified time. Don't issue a new read command to same bank during read with auto-precharge cycle.

Read / Read interrupt cycle

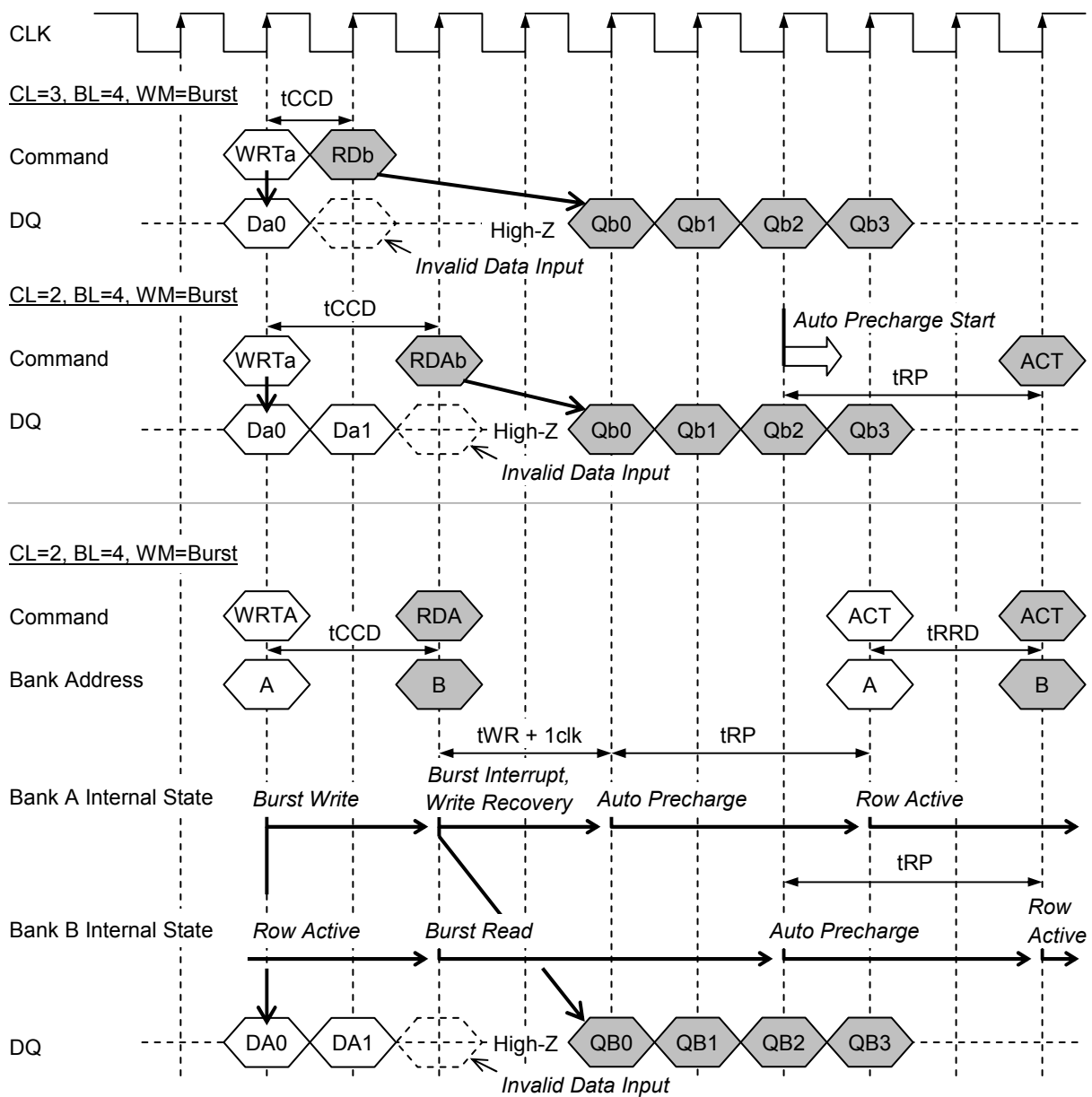




**Write / Read interrupt**

When a new read command is issued to same bank during write cycle or another active bank, current burst write is terminated and new burst read start. When a new read command is issued to another bank during a write with auto-precharge cycle, current burst is terminated and a new read command start. Then, current bank is precharged after specified time. Don't issue a new read command to same bank during write with auto-precharge cycle. DQ must be hi-Z till 1 or more clock from first read data.

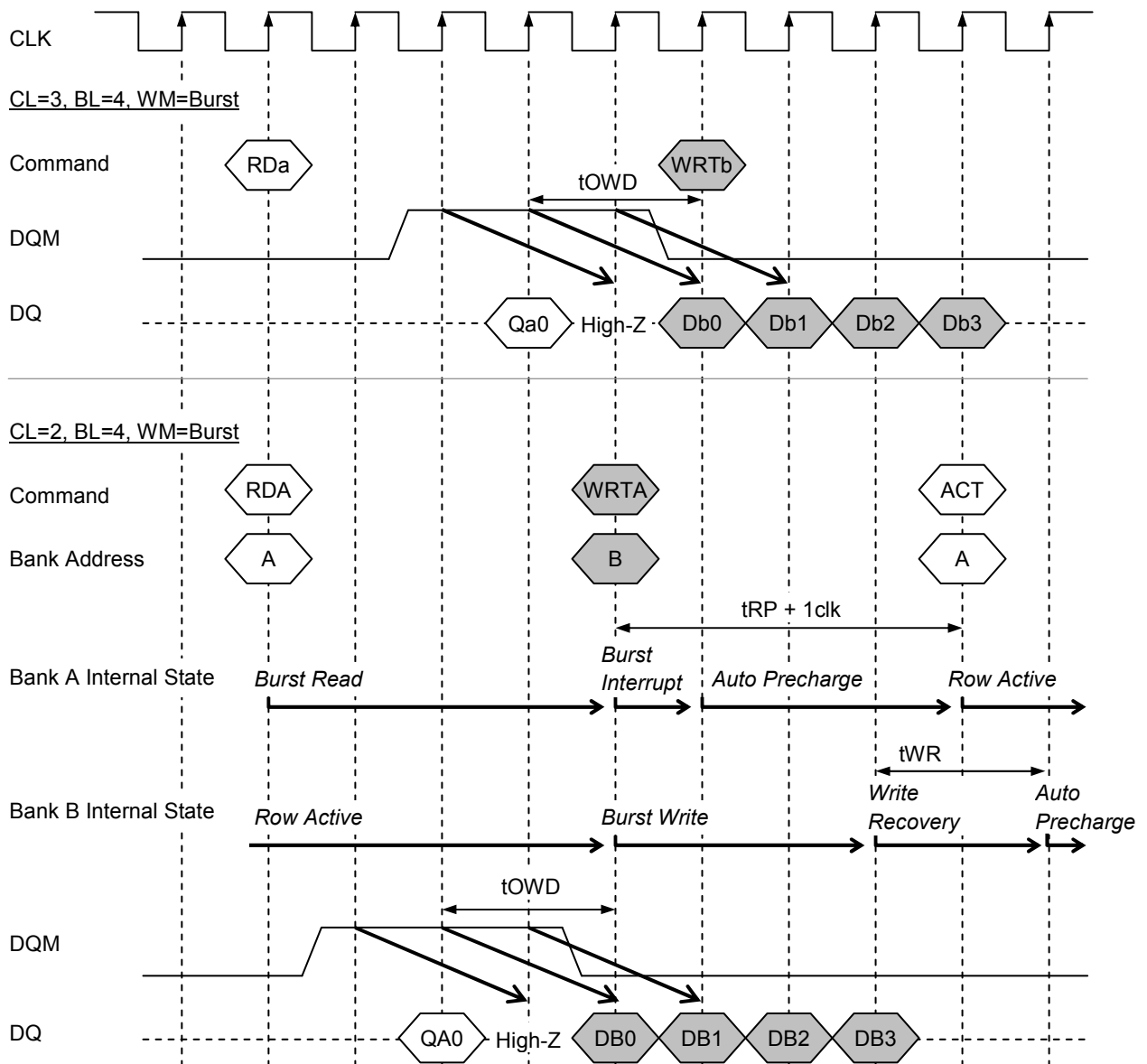
Write / Read interrupt cycle



**Read / Write interrupt**

When a new write command is issued to same bank during read cycle or another active bank, current burst read is terminated and new burst write start. When a new write command is issued to another bank during a read with auto-precharge cycle, current burst is terminated and a new write command start. Then, current bank is precharged after specified time. Don't issue a new write command to same bank during read with auto-precharge cycle. DQ must be Hi-Z till 1 or more clock from new write command. Therefore, DQM must be high till 3 clocks from new write command.

Read / Write interrupt cycle



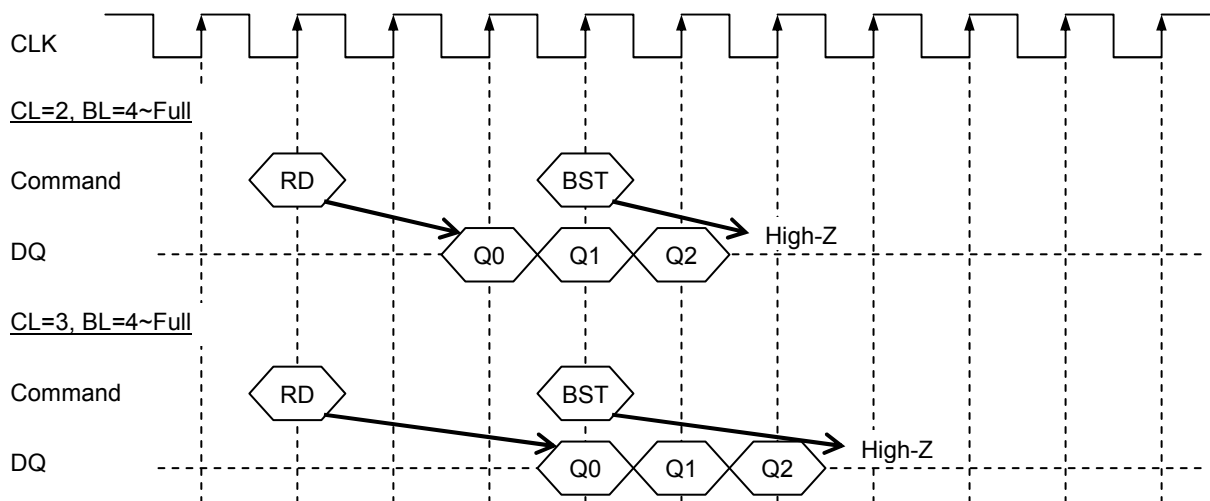
**Burst Stop**

When a burst stop command is issued during read cycle, current burst read is terminated. The DQ is to Hi-Z after the cycle same as /CAS latency and page keep open. When a burst stop command is issued during write cycle, current burst write is terminated. The input data is ignored after burst stop command. Don't issue burst stop command during read with auto-precharge cycle or write with auto-precharge cycle.

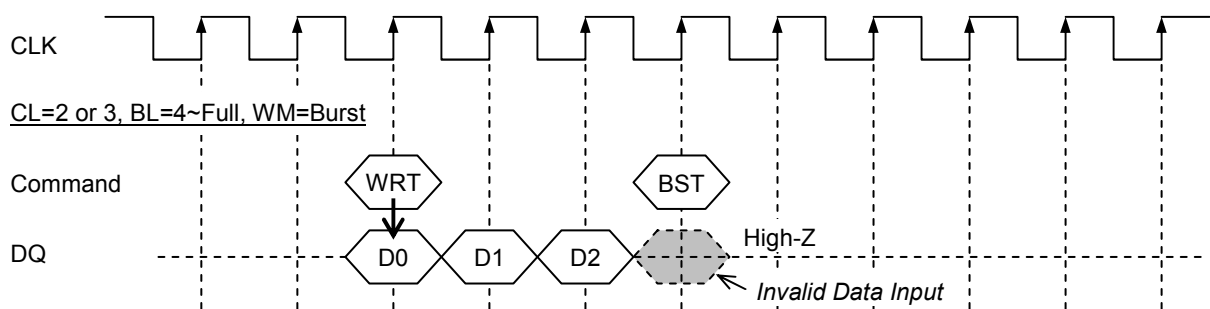
**BST**

CLK	$\uparrow$ n-1	$\uparrow$ n
CKE	H	H
/CS	X (Burst)	L
/RAS		H
/CAS		H
/WE		L
A11		X
A10~A0	X	X

Read / Burst Stop cycle



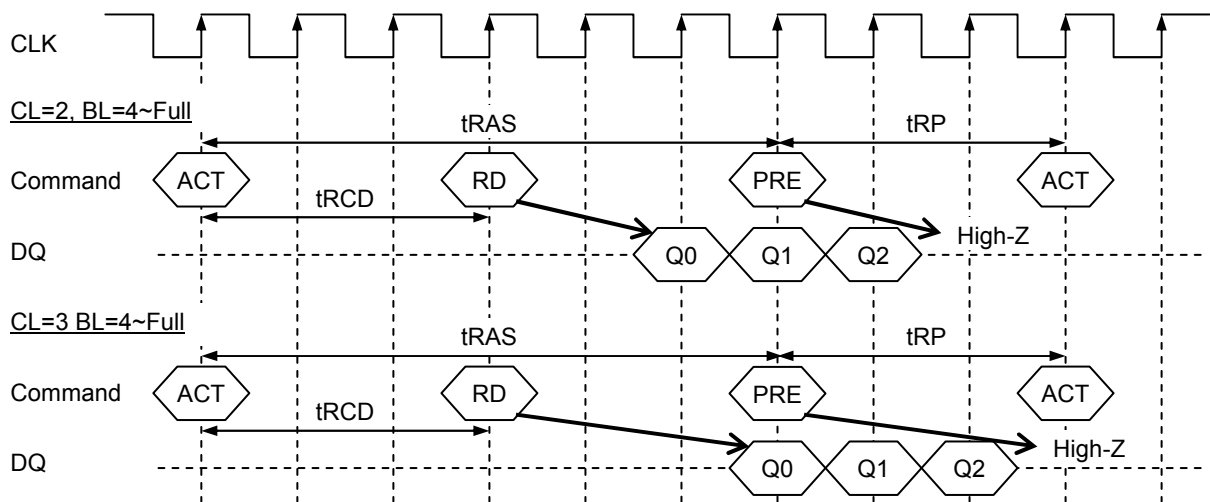
Write / Burst Stop cycle



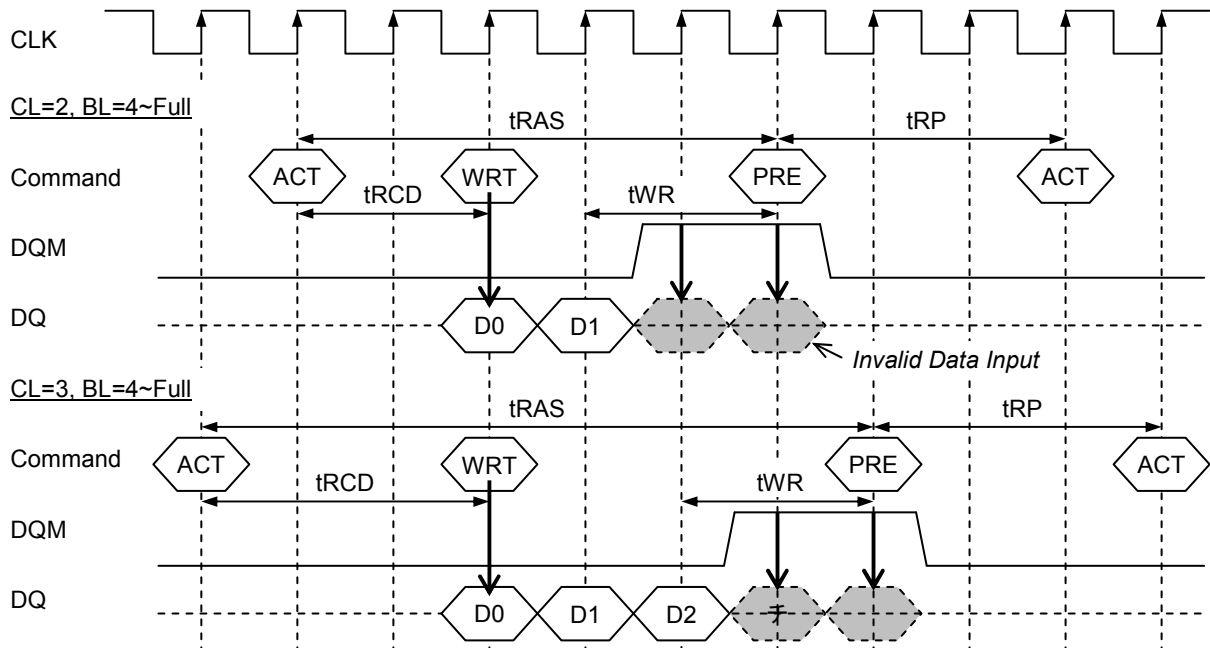
**Precharge Break**

When a precharge command is issued to the same bank during read cycle or precharge all command is issued, current burst read is terminated and DQ is to Hi-Z after the cycle same as /CAS latency. The objected bank is precharged. When a precharge command is issued to the same bank during write cycle or precharge all command is issued, current burst write is terminated and the objected bank is precharged. The input data after precharge command is ignored.

Read / Precharge Break cycle



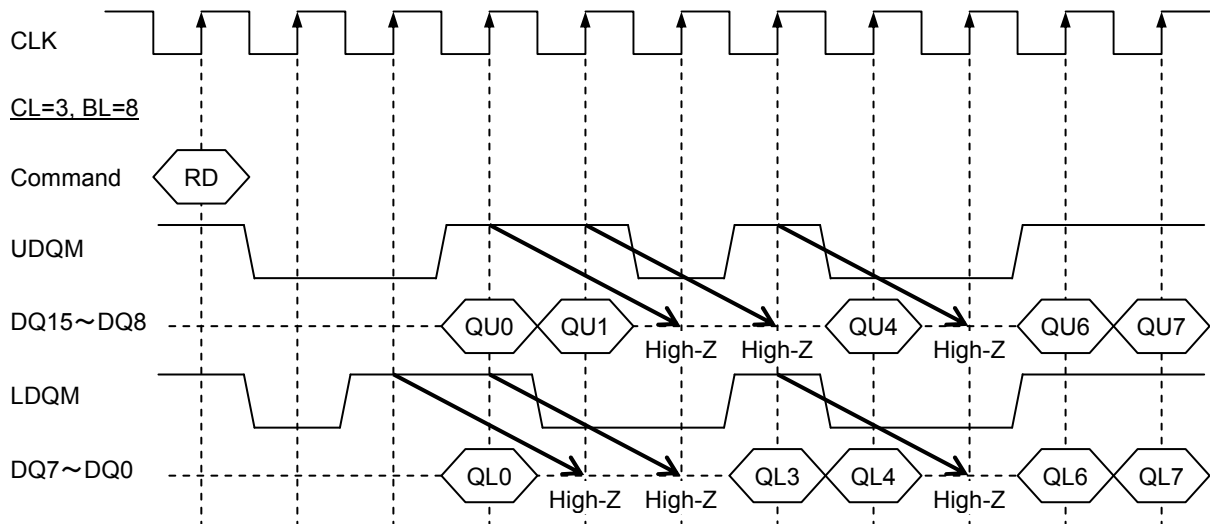
Write / Precharge Break cycle



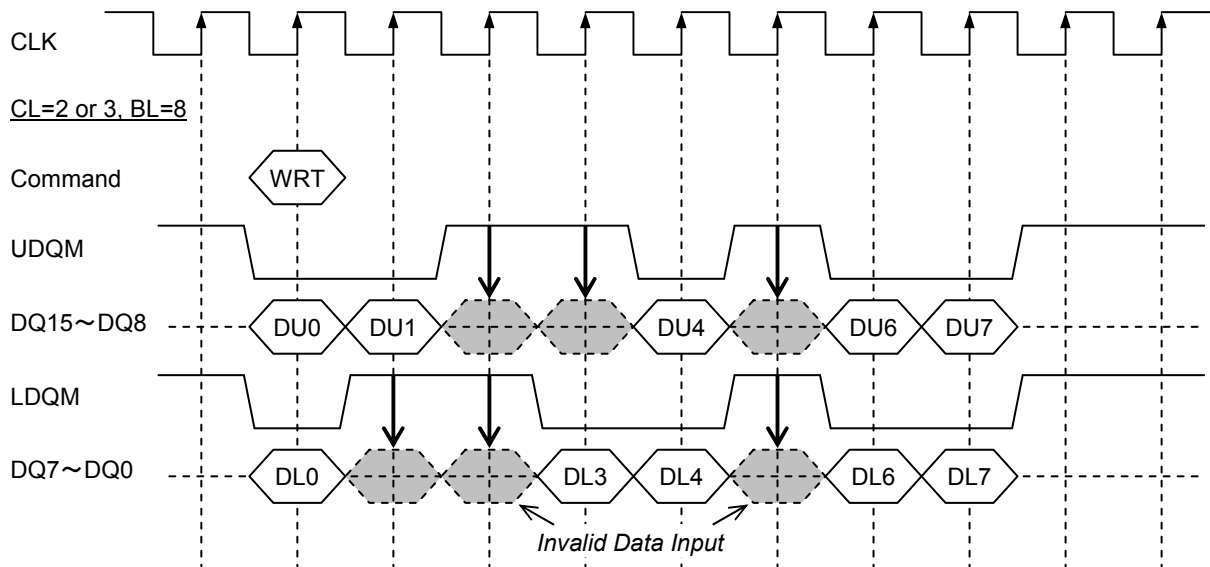
**DQM Function**

DQM masks input / output data at every byte. UDQM controls DQ15 to DQ8 and LDQM controls DQ7 to DQ0. During read cycle, DQM mask output data after 2 clocks. During write cycle, DQM mask input data at same clock.

Read / DQM Function



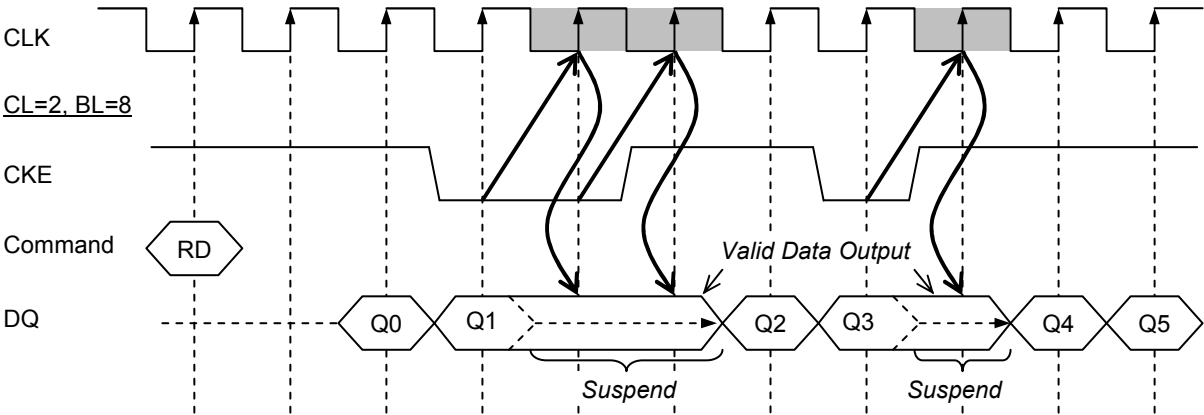
Write / DQM Function



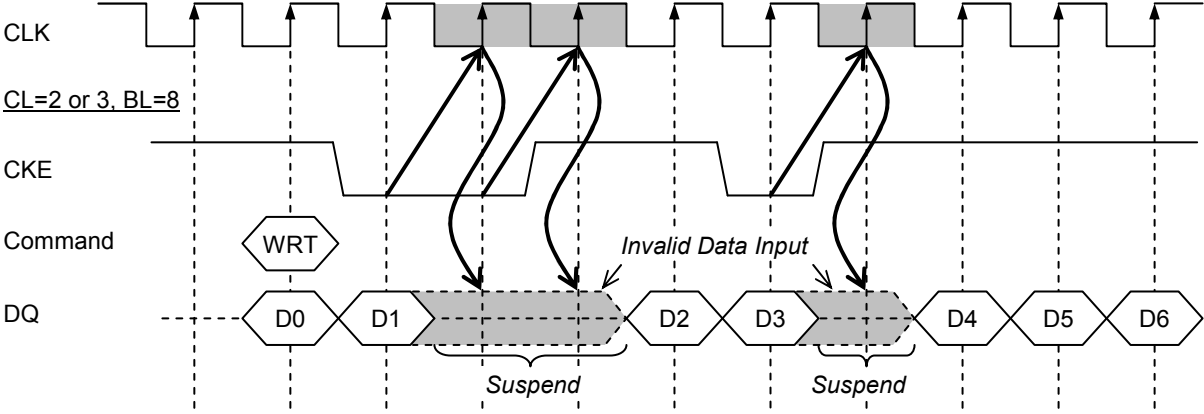
**Clock Suspend**

The read / write operation can be stopped by CKE temporarily. When CKE is set low, the next clock is ignored. When CKE is set low during read cycle, the burst read is stopped temporarily and the current output data is kept. When CKE is set high, burst read is resumed. When CKE is set low during write cycle, the burst write is stopped temporarily. When CKE is set high, burst write is resumed.

Read / Clock Suspend



Write / Clock Suspend



## REFRESH

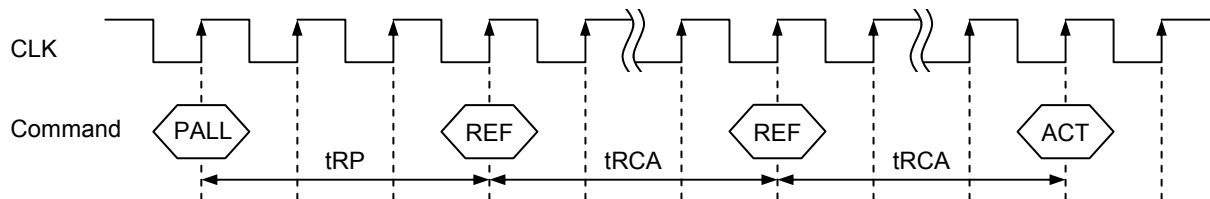
The data of memory cells are maintained by refresh operation. The refresh operation is to activate all row addresses within a refresh time. The method that row addresses are activated by activate and precharge command is called RAS only refresh cycle. This method needs to input row address with activate command. But, auto-refresh and self refresh don't need to input address. Because, row addresses are generated in SDRAM automatically.

### Auto Refresh

All memory area is refreshed by 4,096 times refresh command REF. The refresh command REF can be entered only when all the banks are in an idle state. SDRAM is in idle state after refresh cycle time  $t_{RCA}$ .

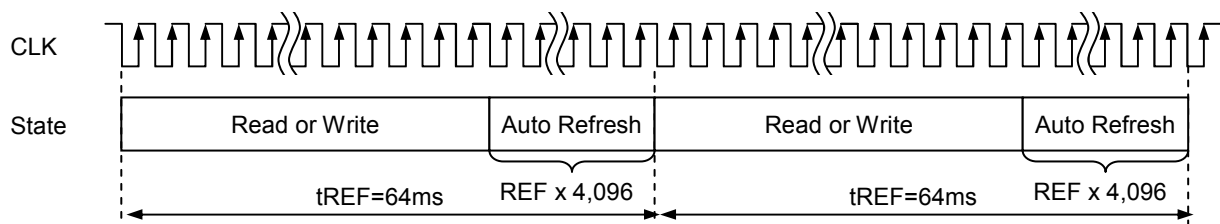
REF		
CLK	$\overline{n-1}$	$\overline{n}$
CKE	H	H
/CS		L
/RAS	X	L
/CAS	(Idle)	L
/WE		H
A11	X	X
A10~A0	X	X

#### Auto-Refresh Cycle



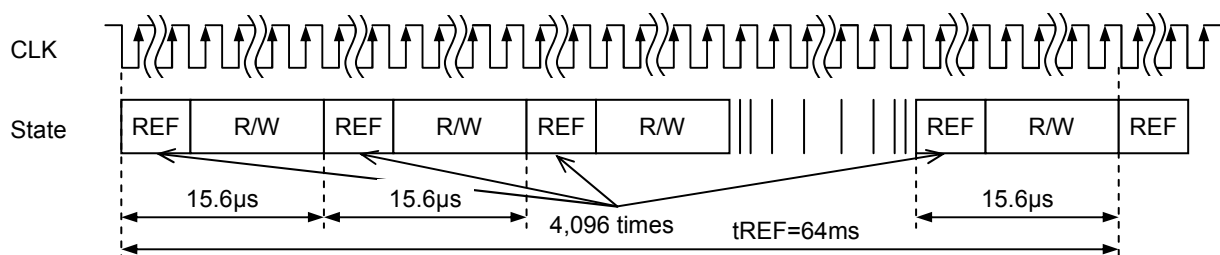
#### Intensive Refresh

4,096 times refresh command can be entered every refresh time  $t_{REF}$ .



#### Dispersed Refresh

Refresh command can be entered every 15.6 $\mu$ s ( $t_{REF}$  64ms / 4,096 cycles).



**Self Refresh**

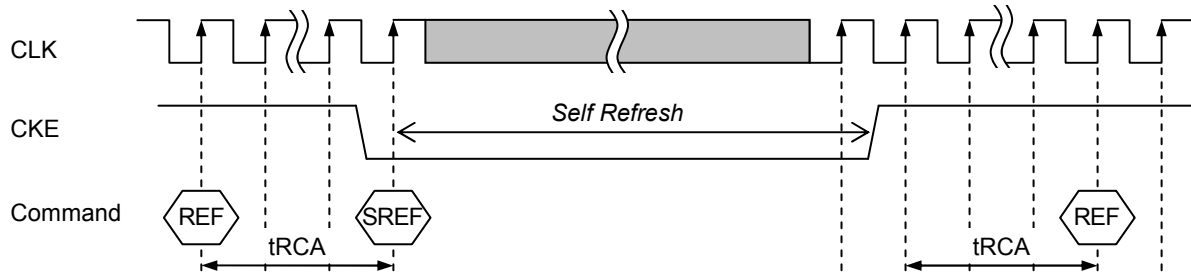
When read or write is not operated in the long period, self refresh can reduce power consumption for refresh operation. Refresh operation is controlled automatically by refresh timer and row address counter during self refresh mode. All signals except CKE are ignored and data bus DQ is set Hi-Z during self refresh mode.

When CKE is set to high level, self refresh mode is finished. Then, CLK must be operated before 1 clock or more. And, maintain NOP condition within a period of tRCA(Min.) after CKE is set to be high level.

**SREF**

CLK	$\uparrow_{n-1}$	$\uparrow_n$
CKE	H	L
/CS	X (Idle)	L
/RAS		L
/CAS		L
/WE		H
A11	X	X
A10~A0	X	X

Self Refresh Cycle



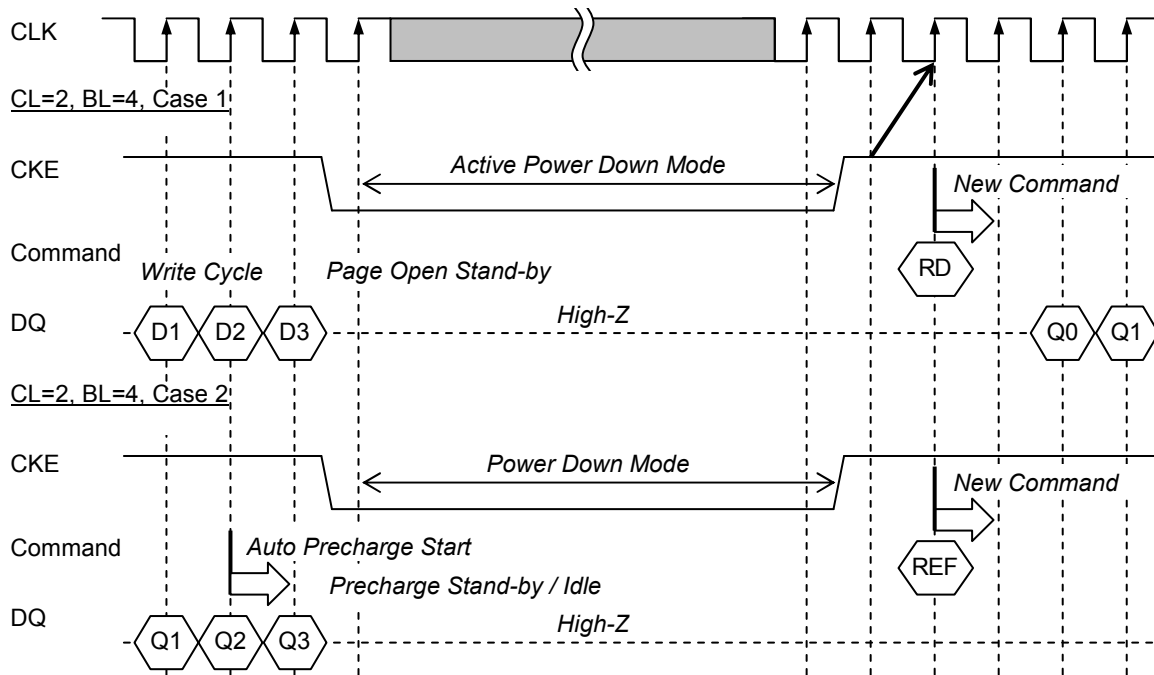
Notes : 1. When intensive refresh is used, 4,096 times refresh must be issued before and after the self refresh.



**Power Down**

SDRAM can be set to low power consumption condition with CKE function. CKE is reflected at 2 clocks later regardless /CAS latency. When CKE is set to low level, SDRAM go into power down mode. All signals except CKE are ignored and DQ is set to High impedance in this state. When CKE is set to high level, SDRAM exit power down mode. Then, Clock must be resumed before 2 or more clocks.

Power Down



**Signal Condition in Power Down Mode**

Signal	Input to SDRAM	Output from SDRAM
CLK	Don't Care	—
CKE	"L" level	—
/CS,/RAS, /CAS, /WE	Don't Care	—
A11, A10~A0	Don't Care	—
DQ15~DQ0	Don't Care	High-Z
UDQM,LDQM	Don't Care	—
VCC,VCCQ,VSS,VSSQ	Power Supply	—

Notes : 1. "Don't Care" means high or low level input.

FUNCTION TRUTH TABLE (Table 1) (1/3)

Current State *1	/CS	/RAS	/CAS	/WE	ADDR	Command	Action
Idle	H	X	X	X	X	NOP	NOP
	L	H	H	X	X	NOP/BST	NOP
	L	H	L	H	BA, CA, A10	RD/RDA	ILLEGAL *2
	L	H	L	L	BA, CA, A10	WRT/WRTA	ILLEGAL *2
	L	L	H	H	BA, RA	ACT	Row Active
	L	L	H	L	BA, A10	PRE/PALL	NOP *3
	L	L	L	H	X	REF	Auto-Refresh or Self-Refresh *4
	L	L	L	L	V, BA1=0	MRS	Mode Register Set *4
	L	L	L	L	V, BA1=0	EMRS	ILLEGAL *4,10
Row Active	H	X	X	X	X	NOP	NOP
	L	H	H	X	X	NOP/BST	NOP
	L	H	L	H	BA, CA, A10	RD/RDA	Read
	L	H	L	L	BA, CA, A10	WRT/WRTA	Write
	L	L	H	H	BA, RA	ACT	ILLEGAL *6
	L	L	H	L	BA, A10	PRE/PALL	Precharge
	L	L	L	H	X	REF	ILLEGAL
	L	L	L	L	X	MRS/EMRS	ILLEGAL
Read	H	X	X	X	X	NOP	Continue Row Active after Burst ends
	L	H	H	H	X	NOP	Continue Row Active after Burst ends
	L	H	H	L	X	BST	Term Burst --> Row Active
	L	H	L	H	BA, CA, A10	RD/RDA	Term Burst, start new Burst Read
	L	H	L	L	BA, CA, A10	WRT/WRTA	Term Burst, start new Burst Write
	L	L	H	H	BA, RA	ACT	ILLEGAL *6
	L	L	H	L	BA, A10	PRE/PALL	Term Burst, execute Row Precharge
	L	L	L	H	X	REF	ILLEGAL
Write	H	X	X	X	X	X	Continue Row Active after Burst ends
	L	H	H	H	X	X	Continue Row Active after Burst ends
	L	H	H	L	X	X	Term Burst --> Row Active
	L	H	L	H	BA, CA, A10	CA, A10	Term Burst, start new Burst Read
	L	H	L	L	BA, CA, A10	CA, A10	Term Burst, start new Burst Write
	L	L	H	H	BA, RA	RA	ILLEGAL *6
	L	L	H	L	BA, A10	A10	Term Burst, execute Row Precharge
	L	L	L	H	X	REF	ILLEGAL
L	L	L	L	X	MRS/EMRS	ILLEGAL	

FUNCTION TRUTH TABLE (Table 1) (2/3)

Current State <sup>*1</sup>	/CS	/RAS	/CAS	/WE	ADDR	Command	Action
Read with Auto Precharge	H	X	X	X	X	NOP	Continue Burst to End and enter Row Precharge
	L	H	H	H	X	NOP	Continue Burst to End and enter Row Precharge
	L	H	H	L	X	BST	ILLEGAL
	L	H	L	H	BA, CA, A10	RD/RDA	ILLEGAL <sup>*7</sup>
	L	H	L	L	BA, CA, A10	WRT/WRTA	ILLEGAL <sup>*7</sup>
	L	L	H	H	BA, RA	ACT	ILLEGAL <sup>*6</sup>
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL <sup>*8</sup>
	L	L	L	H	X	REF	ILLEGAL
	L	L	L	L	X	MRS/EMRS	ILLEGAL
Write with Auto Precharge	H	X	X	X	X	NOP	Continue Burst to End and enter Row Precharge
	L	H	H	H	X	NOP	Continue Burst to End and enter Row Precharge
	L	H	H	L	X	BST	ILLEGAL
	L	H	L	H	BA, CA, A10	RD/RDA	ILLEGAL <sup>*7</sup>
	L	H	L	L	BA, CA, A10	WRT/WRTA	ILLEGAL <sup>*7</sup>
	L	L	H	H	BA, RA	ACT	ILLEGAL <sup>*6</sup>
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL <sup>*8</sup>
	L	L	L	H	X	REF	ILLEGAL
	L	L	L	L	X	MRS/EMRS	ILLEGAL
Precharge	H	X	X	X	X	NOP	Idle after t <sub>RP</sub>
	L	H	H	H	X	NOP	Idle after t <sub>RP</sub>
	L	H	H	L	X	BST	ILLEGAL
	L	H	L	H	BA, CA, A10	RD/RDA	ILLEGAL <sup>*2</sup>
	L	H	L	L	BA, CA, A10	WRT/WRTA	ILLEGAL <sup>*2</sup>
	L	L	H	H	BA, RA	ACT	ILLEGAL <sup>*6</sup>
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL <sup>*3</sup>
	L	L	L	H	X	REF	ILLEGAL
	L	L	L	L	X	MRS/EMRS	ILLEGAL
Write Recovery <sup>*9</sup>	H	X	X	X	X	NOP	Row Active after t <sub>WR</sub>
	L	H	H	H	X	NOP	Row Active after t <sub>WR</sub>
	L	H	H	L	X	BST	ILLEGAL
	L	H	L	H	BA, CA, A10	RD/RDA	ILLEGAL <sup>*2</sup>
	L	H	L	L	BA, CA, A10	WRT/WRTA	ILLEGAL <sup>*2</sup>
	L	L	H	H	BA, RA	ACT	ILLEGAL <sup>*6</sup>
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL <sup>*8</sup>
	L	L	L	H	X	REF	ILLEGAL
	L	L	L	L	X	MRS/EMRS	ILLEGAL

FUNCTION TRUTH TABLE (Table 1) (3/3)

Current State <sup>*1</sup>	/CS	/RAS	/CAS	/WE	ADDR	Command	Action
Write Recovery in Auto Precharge <sup>*9</sup>	H	X	X	X	X	NOP	enter Row Precharge after t <sub>WR</sub>
	L	H	H	H	X	NOP	enter Row Precharge after t <sub>WR</sub>
	L	H	H	L	X	BST	ILLEGAL
	L	H	L	H	BA, CA, A10	RD/RDA	ILLEGAL <sup>*7</sup>
	L	H	L	L	BA, CA, A10	WRT/WRTA	ILLEGAL <sup>*7</sup>
	L	L	H	H	BA, RA	ACT	ILLEGAL <sup>*6</sup>
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL <sup>*8</sup>
	L	L	L	H	X	REF	ILLEGAL
	L	L	L	L	X	MRS/EMRS	ILLEGAL
Auto Refresh	H	X	X	X	X	NOP	Idle after t <sub>RCA</sub>
	L	H	H	H	X	NOP	Idle after t <sub>RCA</sub>
	L	H	H	L	X	BST	ILLEGAL
	L	H	L	H	BA, CA, A10	RD/RDA	ILLEGAL
	L	H	L	L	BA, CA, A10	WRT/WRTA	ILLEGAL
	L	L	H	H	BA, RA	ACT	ILLEGAL
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL
	L	L	L	H	X	REF	ILLEGAL
	L	L	L	L	X	MRS/EMRS	ILLEGAL
Mode Register Access	H	X	X	X	X	NOP	Idle after t <sub>MRD</sub>
	L	H	H	H	X	NOP	Idle after t <sub>MRD</sub>
	L	H	H	L	X	BST	ILLEGAL
	L	H	L	H	BA, CA, A10	RD/RDA	ILLEGAL
	L	H	L	L	BA, CA, A10	WRT/WRTA	ILLEGAL
	L	L	H	H	BA, RA	ACT	ILLEGAL
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL
	L	L	L	H	X	REF	ILLEGAL
	L	L	L	L	X	MRS/EMRS	ILLEGAL

## ABBREVIATIONS

ADDR = Address      RA = Row Address      BA = Bank Address      CA = Column Address  
 NOP = No OPERATION command      V = Value of Mode Register Set

- \*Notes : 1. All inputs are enabled when CKE is set high for at least 1 cycle prior to the inputs.  
 2. RD/RDA or WRT/WRTA command to same bank is forbidden. But RD/RDA or WRT/WRTA command to activated page in another bank is valid.  
 3. PRE command to another activated bank is valid. PALL command is valid to only activated bank.  
 4. Illegal if any bank is not idle.  
 5. RD/RDA or WRT/WRTA command to activated bank is valid after t<sub>RCD</sub>(min.) from ACT command.  
 6. Activate command to the same bank is forbidden. But activate command to another bank in idle state is valid.  
 7. RD/RDA or WRT/WRTA command to same bank is forbidden. But RD/RDA or WRT/WRTA command to activated page in another bank is valid.  
 8. PRE to same bank is forbidden. PRE to another bank must be issued after t<sub>RAS</sub>(min.). PALL command is forbidden.  
 9. Write recovery states means a period from last data to the time that t<sub>WR</sub>(min.) passed.  
 10. Extended Mode Register Set Command (EMRS) is illegal.

FUNCTION TRUTH TABLE for CKE (Table 2)

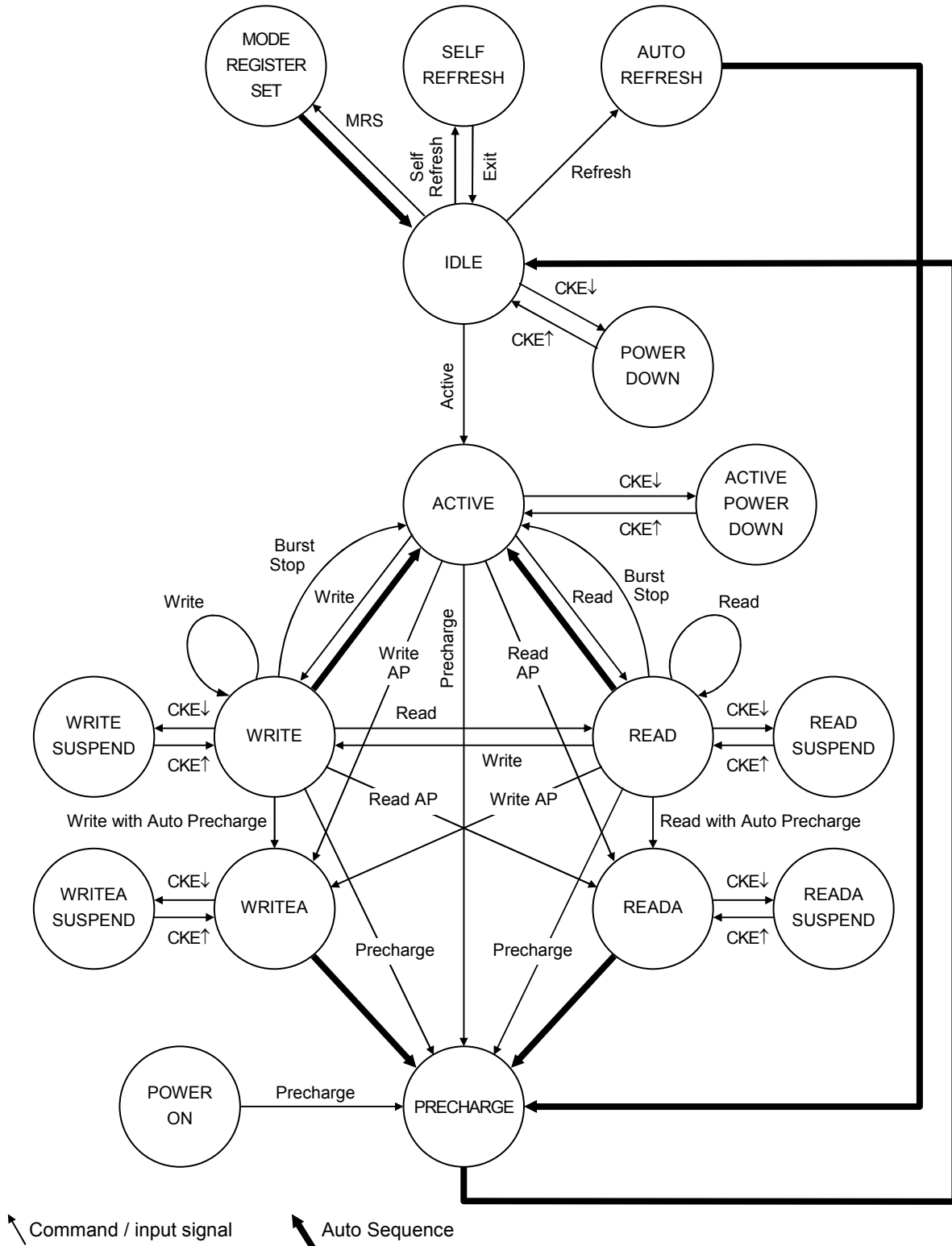
Current State n-1	CKE n-1	CKE n	/CS n	/RAS n	/CAS n	/WE n	ADDR n	Action
All Banks Idle (ABI)	H	H	X	X	X	X	X	Refer to Table 1
	H	L	H	X	X	X	X	Enter Power Down
	H	L	L	H	H	H	X	Enter Power Down
	H	L	L	H	H	L	X	ILLEGAL
	H	L	L	H	L	X	X	ILLEGAL
	H	L	L	L	H	H	BA, RA	Enter Active Power Down after Activate
	H	L	L	L	H	L	X	ILLEGAL
	H	L	L	L	L	H	X	Enter Self Refresh <sup>*2</sup>
	H	L	L	L	L	L	BA, V	Enter Power Down after MRS
	L	X	X	X	X	X	X	INVALID
Self Refresh	H	X	X	X	X	X	X	INVALID
	L	H	H	X	X	X	X	Exit Self Refresh --> ABI <sup>*3</sup>
	L	H	L	H	H	H	X	Exit Self Refresh --> ABI <sup>*3</sup>
	L	H	L	H	H	L	X	ILLEGAL
	L	H	L	H	L	X	X	ILLEGAL
	L	H	L	L	X	X	X	ILLEGAL
	L	L	X	X	X	X	X	NOP (Maintain Self Refresh)
Power Down	H	X	X	X	X	X	X	INVALID
	L	H	X	X	X	X	X	Exit Power Down --> ABI <sup>*4</sup>
	L	L	X	X	X	X	X	NOP (Continue Power Down)
Active Power Down	H	X	X	X	X	X	X	INVALID
	L	H	X	X	X	X	X	Exit Active Power Down --> Row Active <sup>*4</sup>
	L	L	X	X	X	X	X	NOP (Continue Active Power Down)
Row Active	H	H	X	X	X	X	X	Refer to Table 1
	H	L	H	X	X	X	X	Enter Active Power Down
	H	L	L	H	H	H	X	Enter Active Power Down
	H	L	L	H	H	L	X	ILLEGAL
	H	L	L	H	L	X	X	Clock Suspension (Refer to Table 1)
	H	L	L	L	H	X	X	Clock Suspension (Refer to Table 1)
	H	L	L	L	L	X	X	ILLEGAL
	L	X	X	X	X	X	X	INVALID
Any State Other than Listed Above	H	H	X	X	X	X	X	Refer to Table 1
	H	L	X	X	X	X	X	Begin Clock Suspend Next Cycle
	L	H	X	X	X	X	X	Enable Clock of Next Cycle
	L	L	X	X	X	X	X	Continue Clock Suspension

## ABBREVIATIONS

ADDR = Address      RA = Row Address      BA = Bank Address      NOP = No Operation command  
V = Value of Mode Register Set      ABI = All Banks Idle

- \*Notes : 1. Deep Power Down can be entered only when all the banks are in an idle state.  
2. Self Refresh can be entered only when all the banks are in an idle state.  
3. tRCA must be set after exit self refresh.  
4. New command is enabled in the next clock.

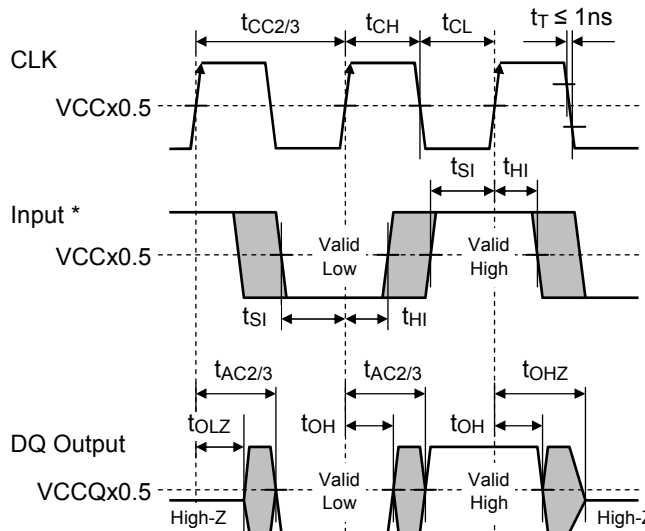
**SIMPLIFIED STATE DIAGRAM**



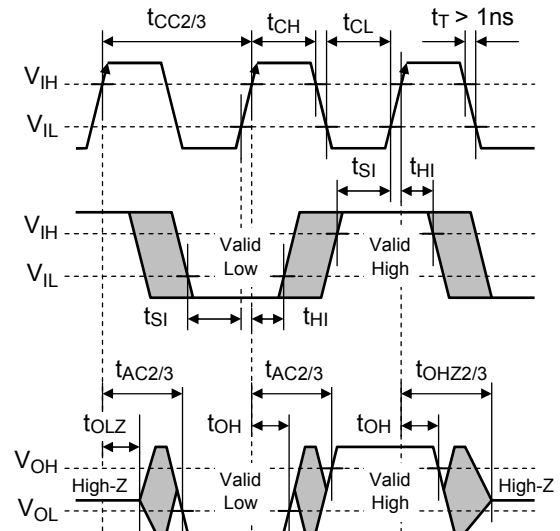
## TIMING CHART

### Synchronous Characteristics

Transition Time  $t_T \leq 1\text{ns}$

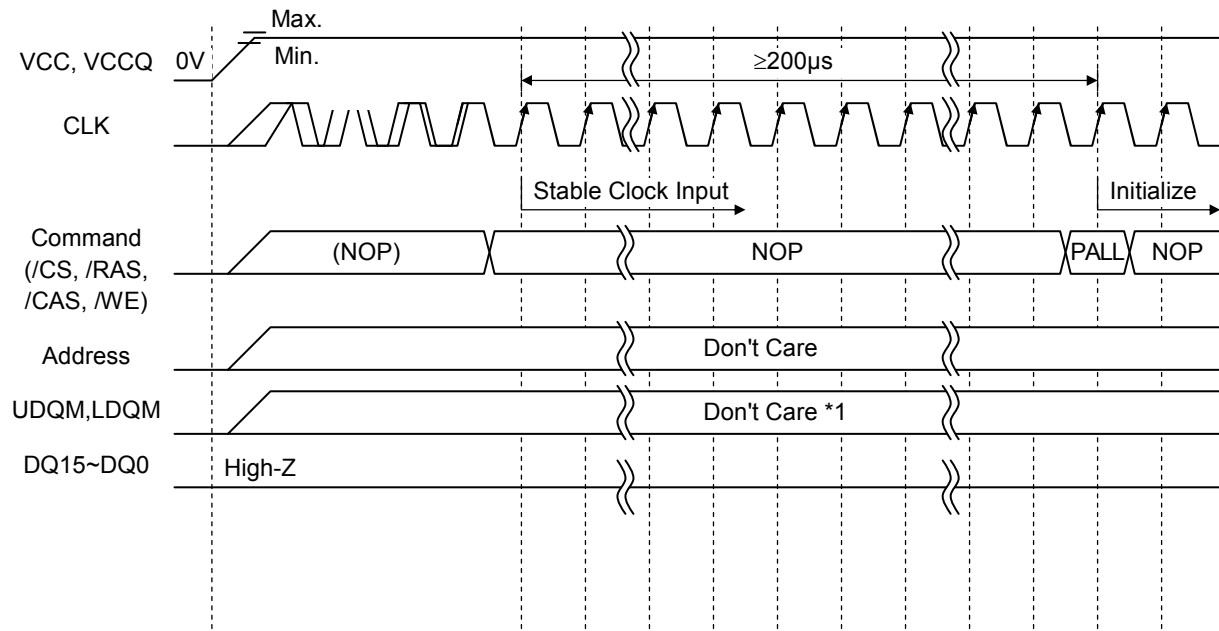


Transition Time  $t_T > 1\text{ns}$



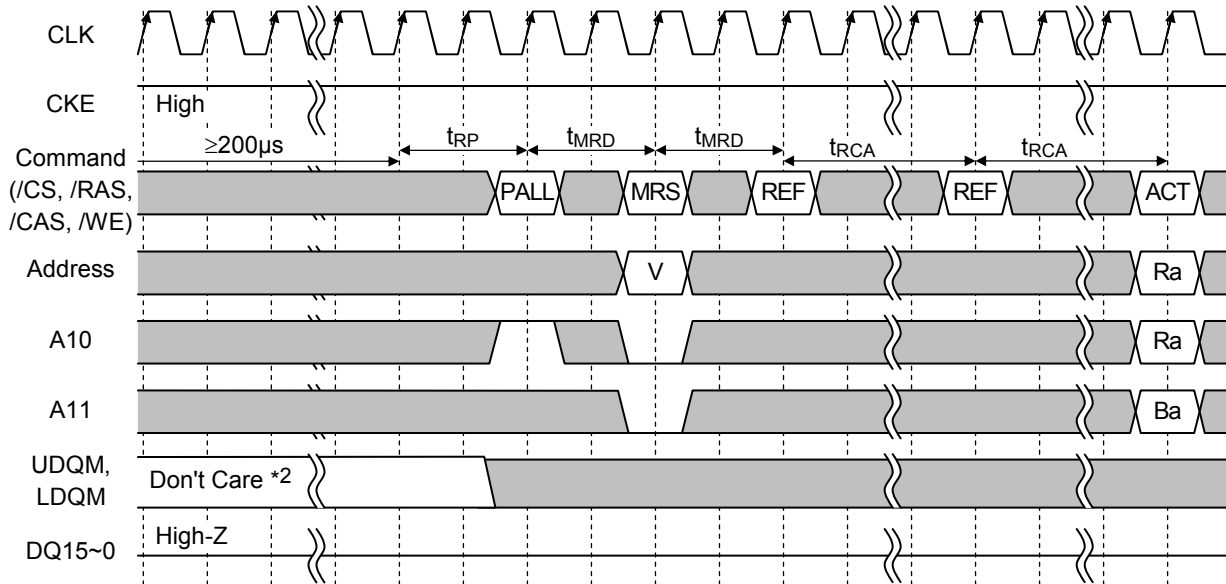
Note : The object of input are CKE, A11, A10 to A0, /CS, /RAS, /CAS, /WE, UDQM to LDQM and DQ15 to DQ0 (input).

### Power on Sequence



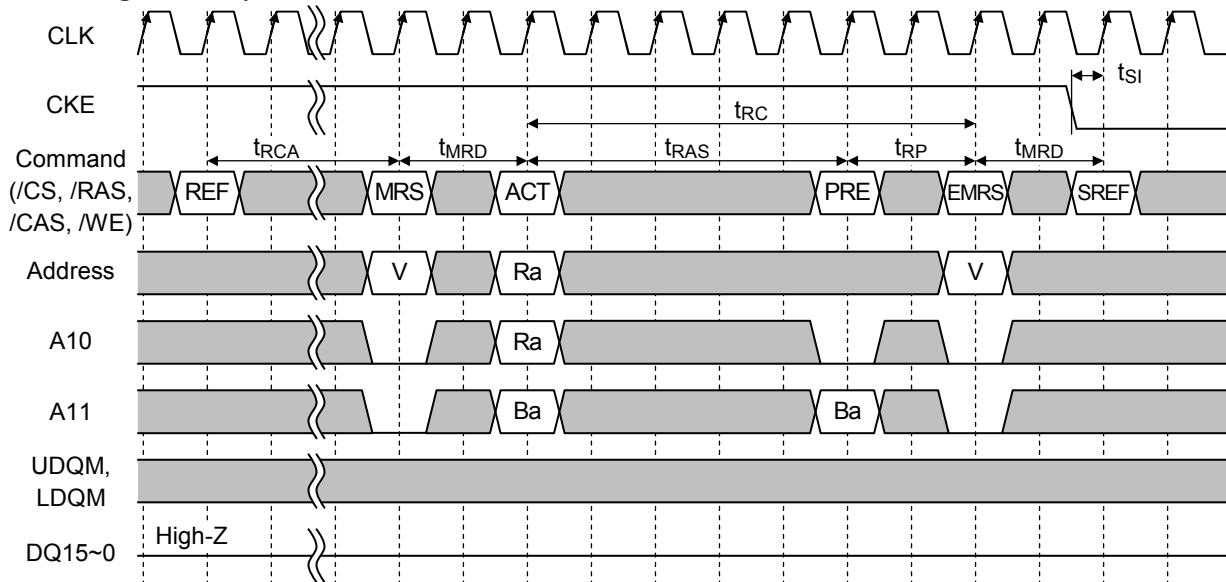
Notes : 1. It is advisable that UDQM and LDQM are set to high for set DQ to high impedance during power on sequence.

**Initialization**



- Notes :
1. V = Value of mode register, Rx = Row Address, Bx = Bank Address  
 = NOP command or High or Low
  2. It is advisable that UDQM to LDQM are set to be high level for setting DQ to high impedance during power on sequence.

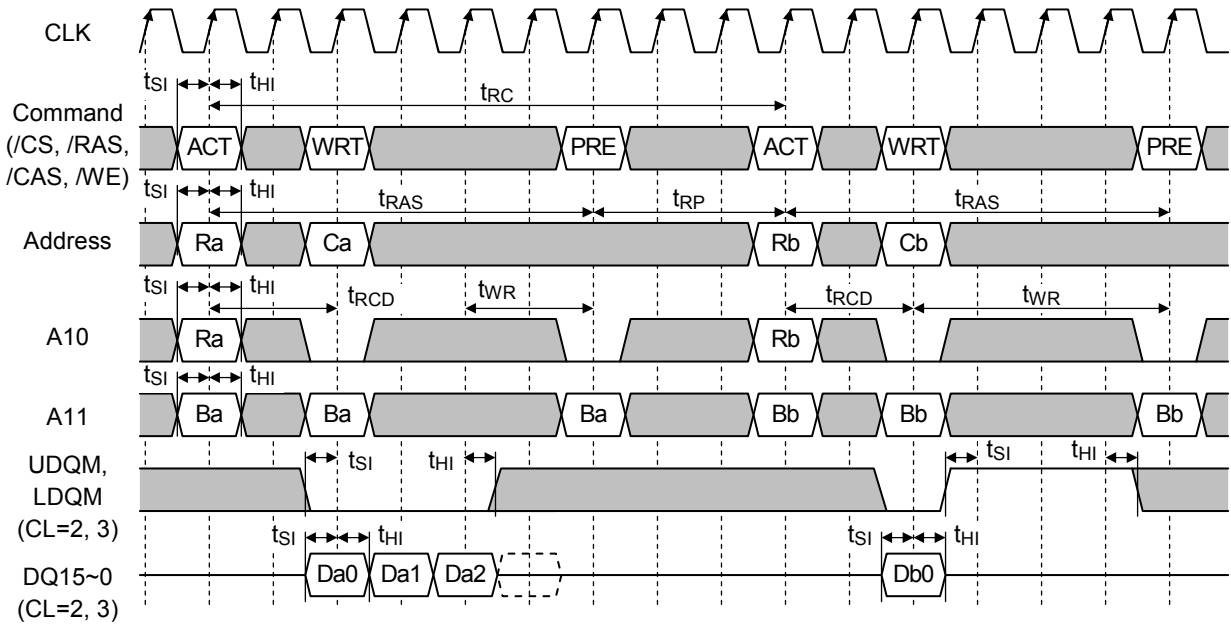
**Mode Register Set cycle**



- Notes :
1. V = Value of mode register, Rx = Row Address, Bx = Bank Address  
 = NOP command or High or Low

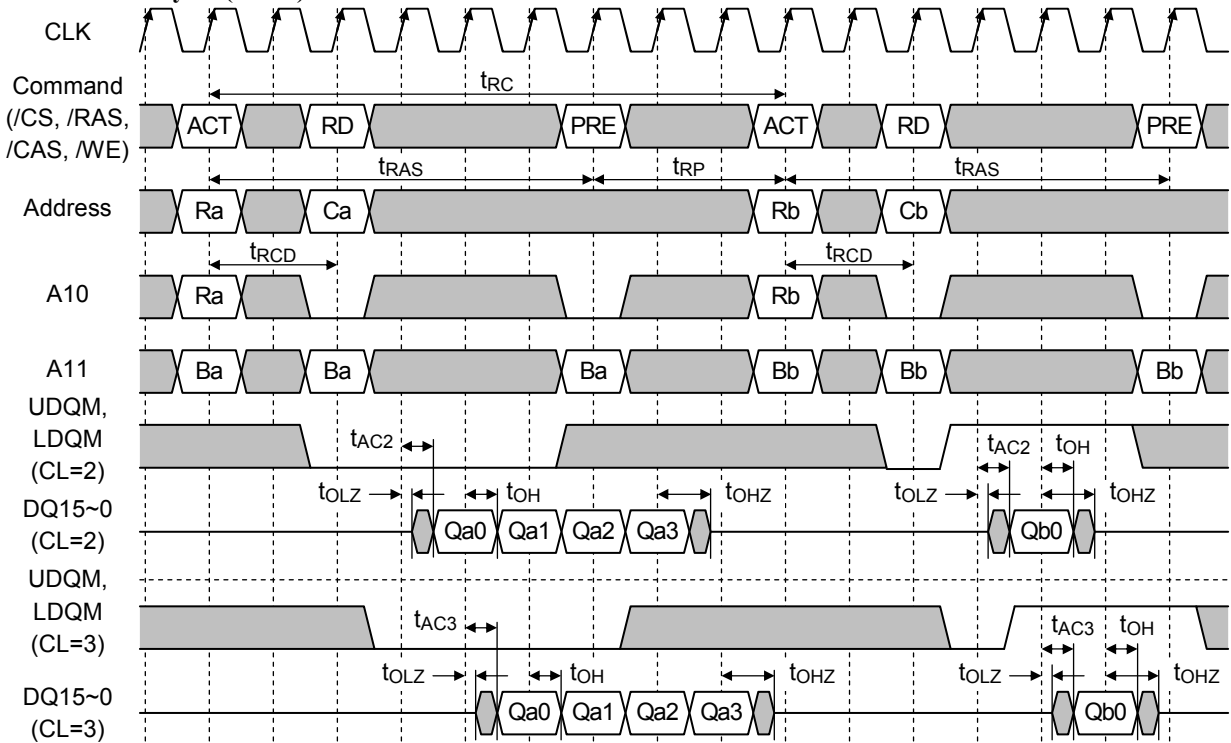


**Burst Write Cycle (BL=4, WM=Burst)**



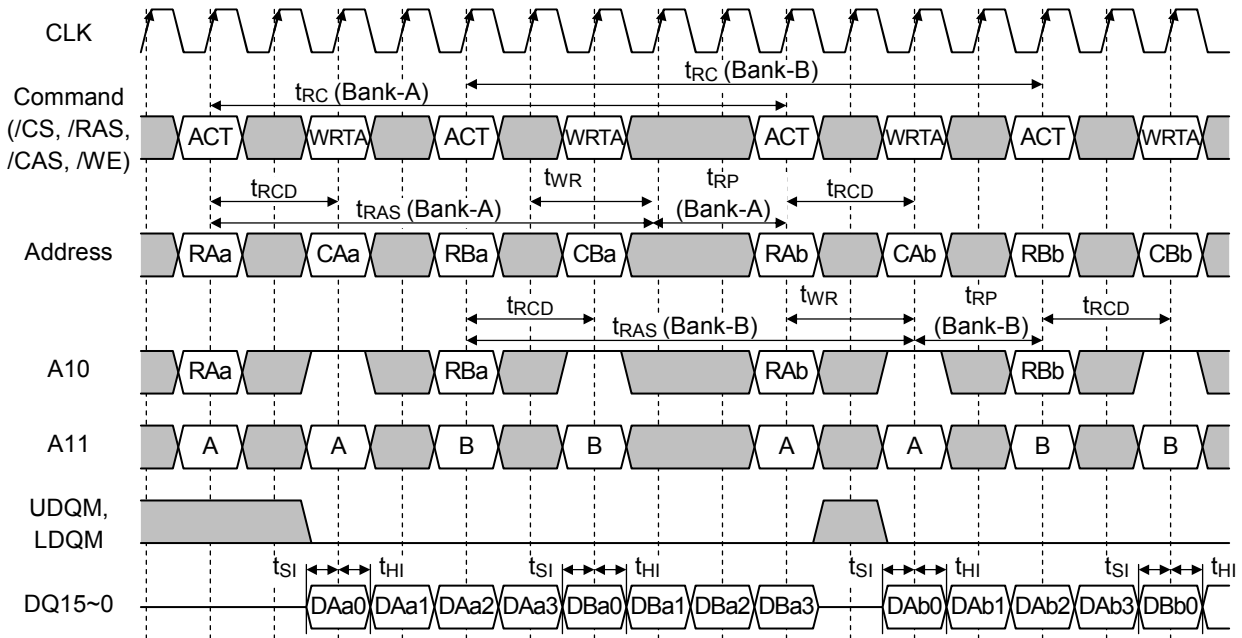
Notes : 1. Rx = Row Address, Cx = Column Address, Bx = Bank Address  
 [Grey Box] = NOP command or High or Low level, CKE = High level

**Burst Read Cycle (BL=4)**



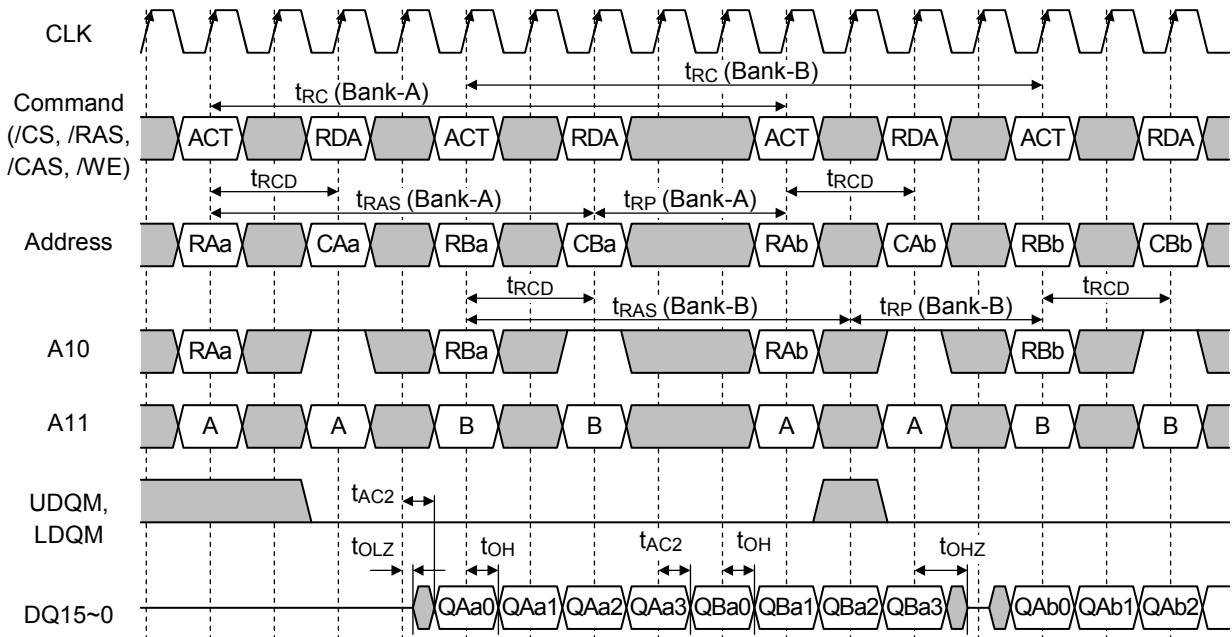
Notes : 1. Rx = Row Address, Cx = Column Address, Bx = Bank Address  
 [Grey Box] = NOP command or High or Low level, CKE = High level

**Bank Interleave • Write with Auto Precharge Cycle (CL=2, BL=4)**



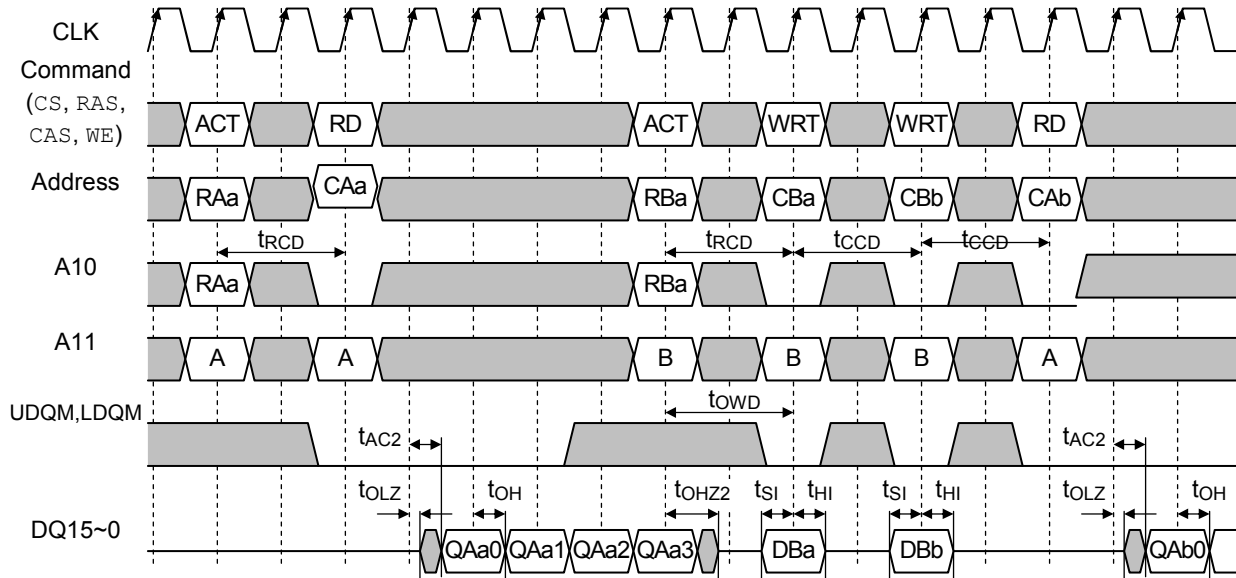
Notes : 1. RXX = Row Address, CXx = Column Address, X = Bank, x = Address  
 [Grey Box] = NOP command or High or Low level, CKE = High level

**Bank Interleave • Read with Auto Precharge Cycle (CL=2, BL=4)**



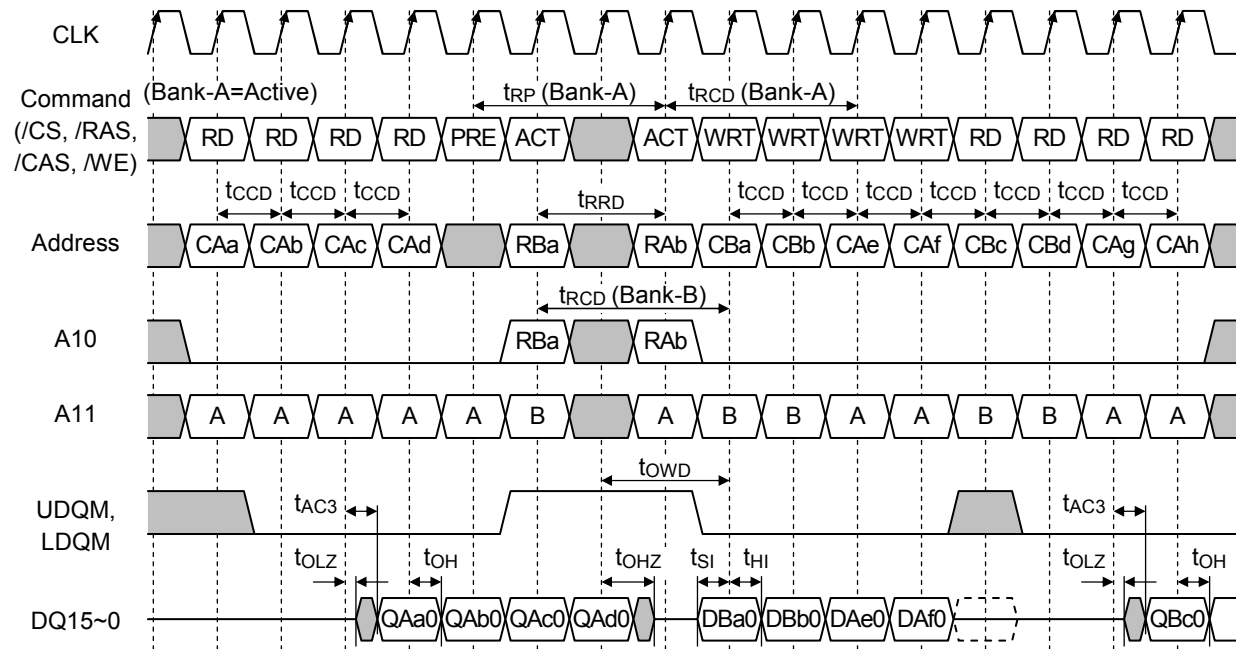
Notes : 1. RXX = Row Address, CXx = Column Address, X = Bank, x = Address  
 [Grey Box] = NOP command or High or Low level, CKE = High level

**Burst Read • Single Write Cycle (CL=2, BL=4, WM=Single)**



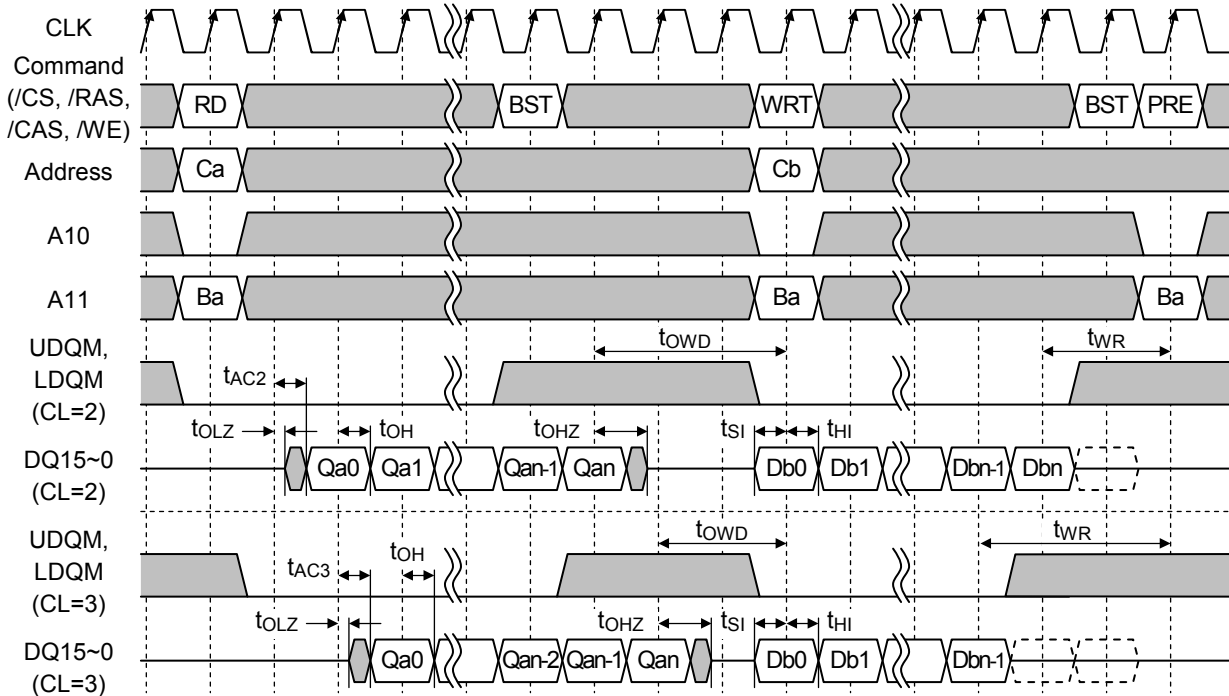
Notes : 1. Rxx = Row Address, Cxx = Column Address, X = Bank, x = Address  
 [█] = NOP command or High or Low level, CKE = High level, [---] = Invalid Data Input

**Random Column • Read / Write Cycle (CL=3, BL=2, 4, 8, Full Page)**



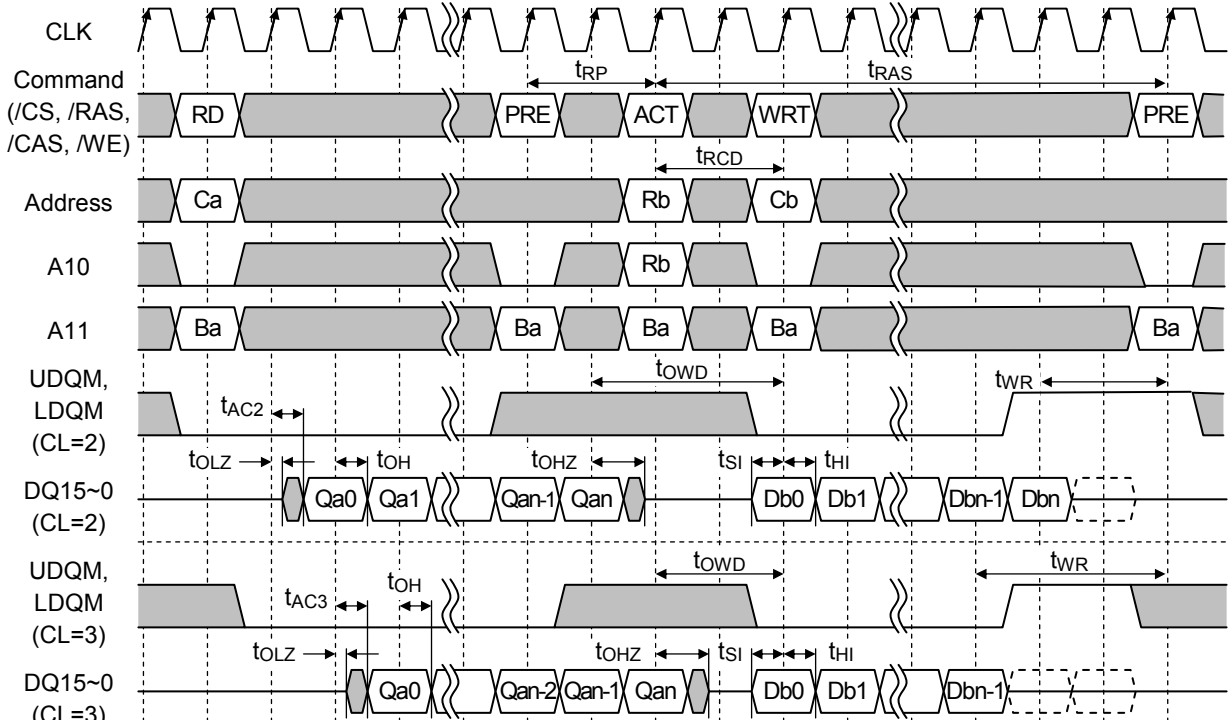
Notes : 1. Rxx = Row Address, Cxx = Column Address, X = Bank, x = Address  
 [█] = NOP command or High or Low level, CKE = High level, [---] = Invalid Data Input

**Burst Stop • Read / Write Cycle (BL=Full Page)**



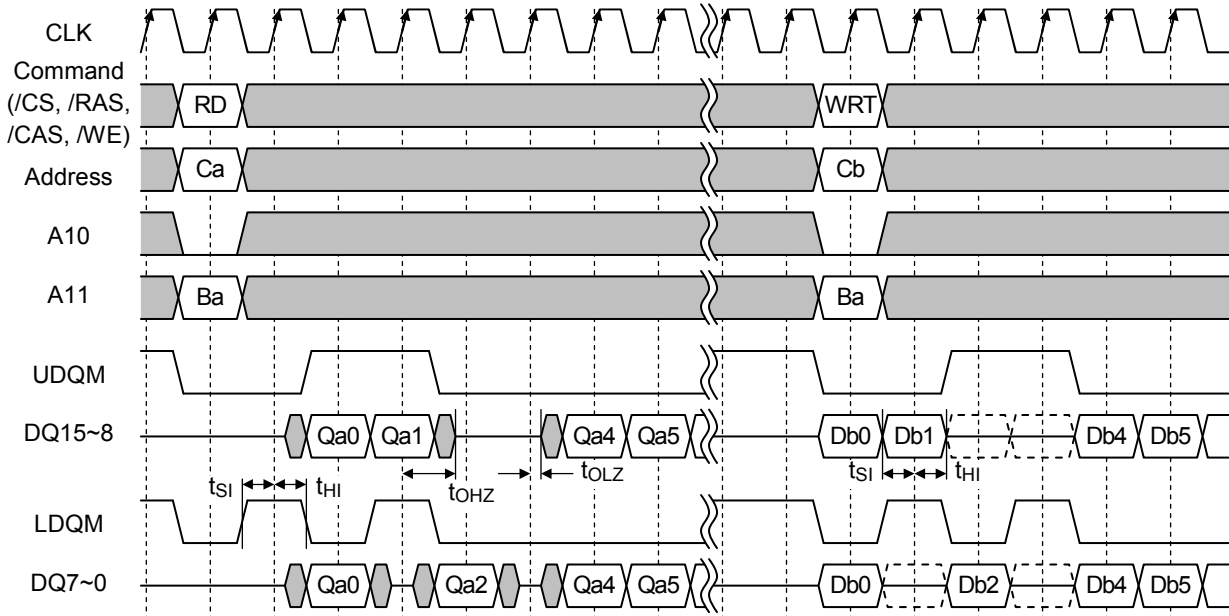
Notes : 1. Cx = Column Address, Bx = Bank Address  
 [Grey Box] = NOP command or High or Low level, CKE = High level, [Dashed Box] = Invalid Data Input

**Precharge Break • Read / Write Cycle (BL=Full Page)**



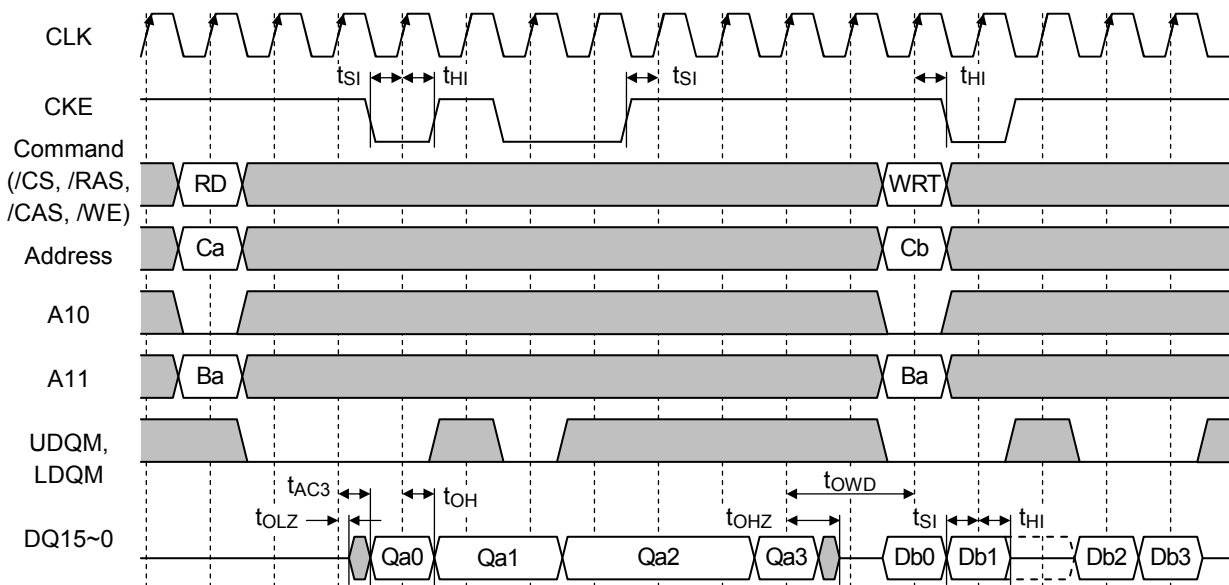
Notes : 1. Rxx = Row Address, Cxx = Column Address, X = Bank, x = Address  
 [Grey Box] = NOP command or High or Low level, CKE = High level, [Dashed Box] = Invalid Data Input

**Byte Read / Byte Write Cycle (CL=2, BL=8)**



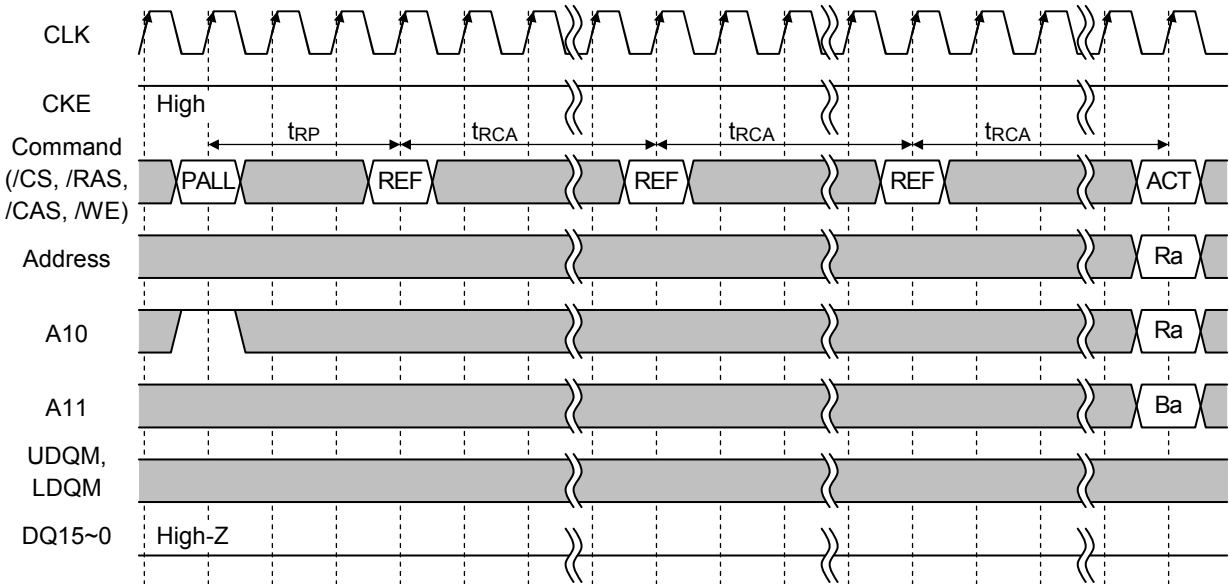
Notes : 1. Cx = Column Address, Bx = Bank Address  
 [█] = NOP command or High or Low level, CKE = High level, [---] = Invalid Data Input

**Clock Suspend • Read / Write Cycle (CL=3, BL=4)**



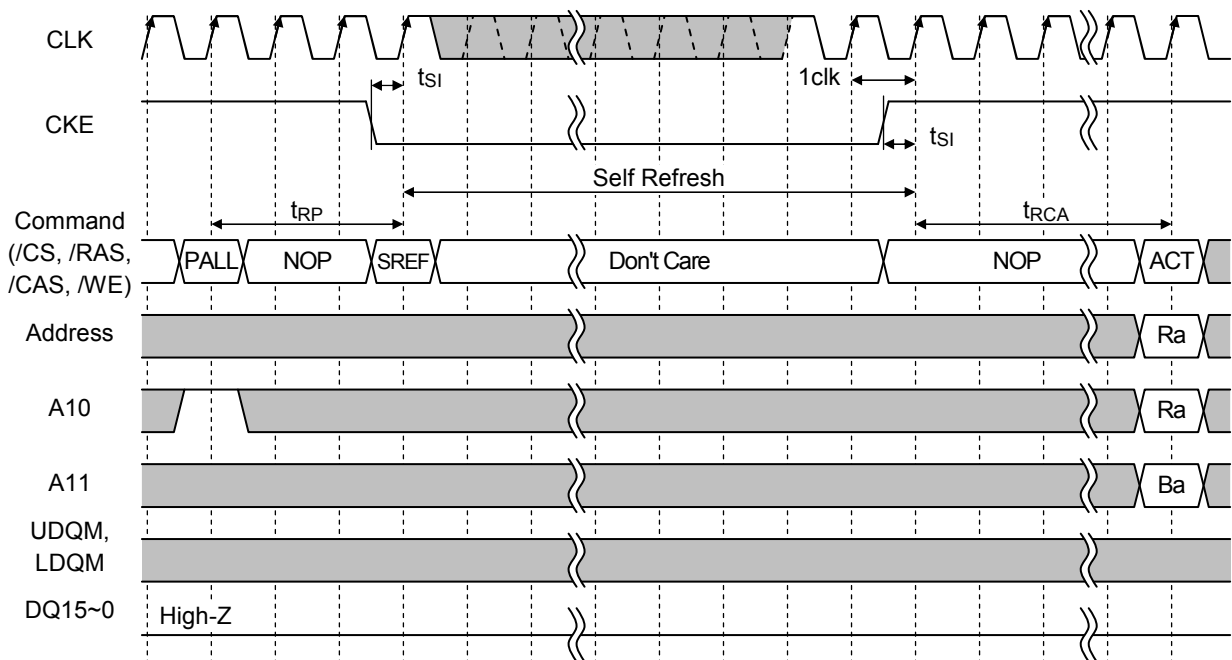
Notes : 1. Cx = Column Address, Bx = Bank Address  
 [█] = NOP command or High or Low level, CKE = High level, [---] = Invalid Data Input

**Auto Refresh Cycle**



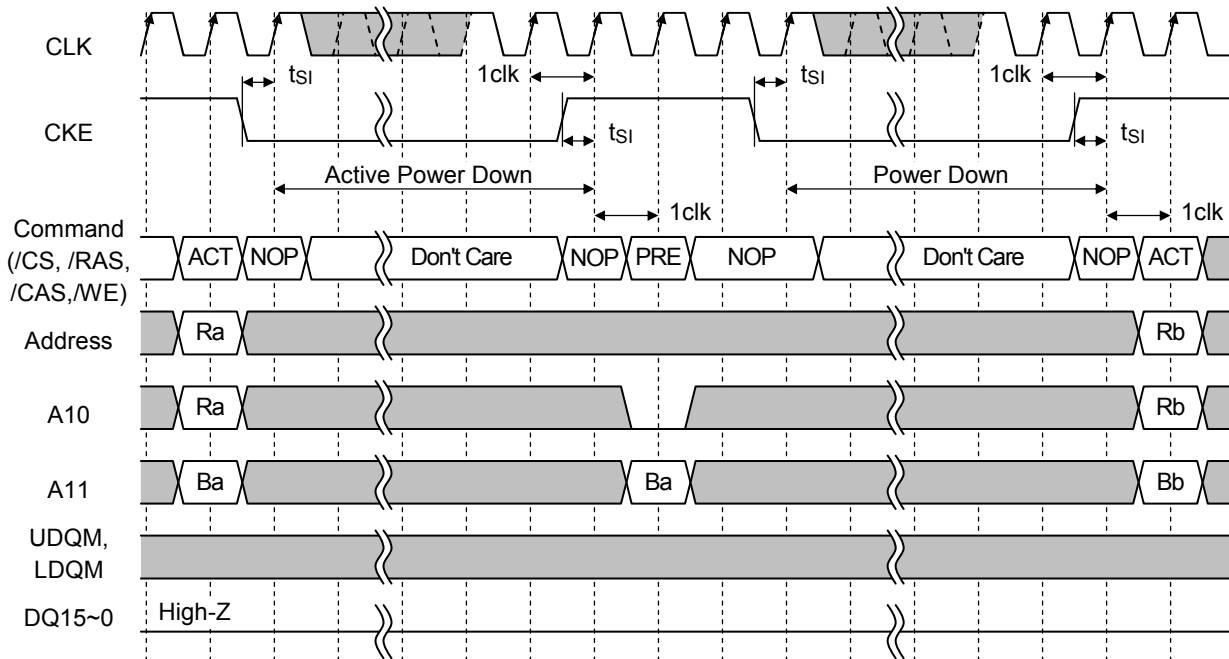
Notes : 1. Rx = Row Address, Bx = Bank Address  
 [Grey Box] = NOP command or High or Low level, CKE = High level, [Dashed Box] = Invalid Data Input

**Self Refresh Cycle**



Notes : 1. Rx = Row Address, Bx = Bank Address  
 [Grey Box] = High or Low level

**Power Down Cycle**



- Notes : 1. Rx = Row Address, Bx = Bank Address  
 [shaded box] = High or Low level

**REVISION HISTORY**

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDD56V16160K-01	Oct. 19, 2010	–	–	First edition



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