

## Dual 25A or Single 50A DC/DC $\mu$ Module Regulator

### FEATURES

- Dual 25A or Single 50A Output
- Input Voltage Range: 4.5V to 15V
- Output Voltage Range: 0.6V to 1.8V
- $\pm 1.5\%$  Maximum Total DC Output Error Over Line, Load and Temperature
- Differential Remote Sense Amplifier
- Current Mode Control/Fast Transient Response
- Adjustable Switching Frequency
- Frequency Synchronization
- Overcurrent Foldback Protection
- Multiphase Parallel Current Sharing with Multiple LTM4650s Up to 300A
- Internal Temperature Monitor
- Pin Compatible with the LTM4620 (Dual 13A, Single 26A) and LTM4630 (Dual 18A, Single 36A)
- Selectable Burst Mode<sup>®</sup> Operation
- Soft-Start/Voltage Tracking
- Output Overvoltage Protection
- 16mm  $\times$  16mm  $\times$  5.01mm BGA Package

### APPLICATIONS

- Processor, ASIC and FPGA Core Power
- Telecom and Networking Equipment
- Storage and ATCA Cards
- Industrial Equipment

### DESCRIPTION

The LTM<sup>®</sup>4650 is a dual 25A or single 50A output switching mode step-down DC/DC  $\mu$ Module<sup>®</sup> (power module) regulator. Included in the package are the switching controllers, power FETs, inductors, and all supporting components. Operating from an input voltage range of 4.5V to 15V, the LTM4650 supports two outputs each with an output voltage range of 0.6V to 1.8V, each set by a single external resistor. Its high efficiency design delivers up to 25A continuous current for each output. Only a few input and output capacitors are needed. The LTM4650 is pin compatible with the LTM4620 (dual 13A, single 26A) and the LTM4630 (dual 18A, single 36A).

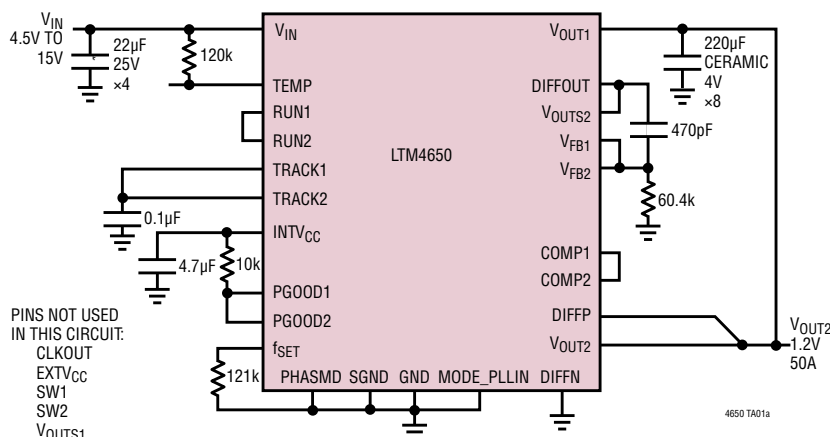
The device supports frequency synchronization, multiphase operation, Burst Mode operation and output voltage tracking for supply rail sequencing and has an onboard temperature diode for device temperature monitoring. High switching frequency and a current mode architecture enable a very fast transient response to line and load changes without sacrificing stability.

Fault protection features include overvoltage and overcurrent protection. The LTM4650 is offered in a 16mm  $\times$  16mm  $\times$  5.01mm BGA package.

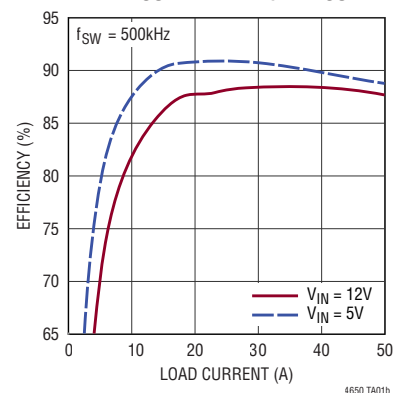
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### TYPICAL APPLICATION

50A, 1.2V Output DC/DC  $\mu$ Module Regulator



1.2V<sub>OUT</sub> Efficiency vs I<sub>OUT</sub>



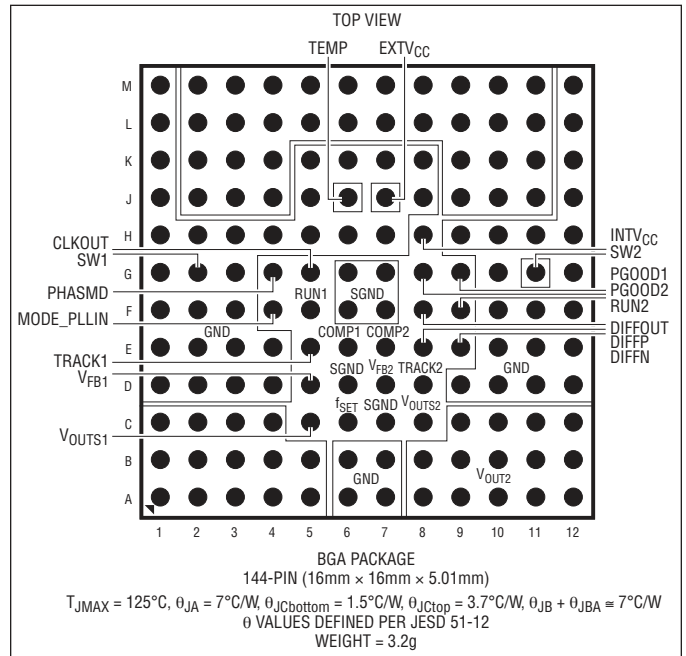
# LTM4650

## ABSOLUTE MAXIMUM RATINGS

(Note 1)

$V_{IN}$ .....	-0.3V to 16V
$V_{SW1}$ , $V_{SW2}$ .....	-1V to 16V
PGOOD1, PGOOD2, RUN1, RUN2, INTV <sub>CC</sub> , EXTV <sub>CC</sub> .....	-0.3V to 6V
MODE_PLLIN, f <sub>SET</sub> , TRACK1, TRACK2, DIFFOUT, PHASMD .....	-0.3V to INTV <sub>CC</sub>
$V_{OUT1}$ , $V_{OUT2}$ , $V_{OUTS1}$ , $V_{OUTS2}$ .....	-0.3V to 6V
DIFFP, DIFFN .....	-0.3V to INTV <sub>CC</sub>
COMP1, COMP2, V <sub>FB1</sub> , V <sub>FB2</sub> (Note 5) .....	-0.3V to 2.7V
INTV <sub>CC</sub> Peak Output Current .....	100mA
Internal Operating Temperature Range (Note 2)	
LTM4650E, LTM4650I .....	-40°C to 125°C
LTM4650MP .....	-55°C to 125°C
Storage Temperature Range .....	
	-55°C to 125°C
Peak Package Body Temperature .....	
	245°C

## PIN CONFIGURATION



## ORDER INFORMATION

PART NUMBER	PAD OR BALL FINISH	PART MARKING*		PACKAGE TYPE	MSL RATING	TEMPERATURE RANGE (NOTE 2)
		DEVICE	FINISH CODE			
LTM4650EY#PBF	SAC305 (RoHS)	LTM4650Y	e1	BGA	3	-40°C to 125°C
LTM4650IY#PBF	SAC305 (RoHS)	LTM4650Y	e1	BGA	3	-40°C to 125°C
LTM4650IY	SnPb (63/37)	LTM4650Y	e0	BGA	3	-40°C to 125°C
LTM4650MPY#PBF	SAC305 (RoHS)	LTM4650Y	e1	BGA	3	-55°C to 125°C
LTM4650MPY	SnPb (63/37)	LTM4650Y	e0	BGA	3	-55°C to 125°C

Contact the factory for parts specified with wider operating temperature ranges. \*Device temperature grade is indicated by a label on the shipping container. Pad or ball finish code is per IPC/JEDEC J-STD-609.

- [Recommended LGA and BGA PCB Assembly and Manufacturing Procedures](#)
- [LGA and BGA Package and Tray Drawings](#)

**ELECTRICAL CHARACTERISTICS** The ● denotes the specifications which apply over the specified internal operating temperature range. Specified as each individual output channel.  $T_A = 25^\circ\text{C}$  (Note 2),  $V_{IN} = 12\text{V}$  and  $V_{RUN1}$ ,  $V_{RUN2}$  at 5V unless otherwise noted. Per the typical application in Figure 22.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	
$V_{IN}$	Input DC Voltage	●	4.5		15	V	
$V_{OUT}$	Output DC Voltage	●	0.6		1.8	V	
$V_{OUT1(DC)}$ , $V_{OUT2(DC)}$	Output Voltage, Total Variation with Line and Load (Note 7)	$C_{IN} = 22\mu\text{F} \times 3$ , $C_{OUT} = 100\mu\text{F} \times 2$ Ceramic, 470 $\mu\text{F}$ POSCAP, $V_{OUT} = 1.2\text{V}$ , $I_{OUT} = 0\text{A}$ to 25A	●	1.182	1.2	1.218	V
<b>Input Specifications</b>							
$V_{RUN1}$ , $V_{RUN2}$	RUN Pin On/Off Threshold	RUN Rising		1.1	1.25	1.40	V
$V_{RUN1HYS}$ , $V_{RUN2HYS}$	RUN Pin On Hysteresis				150		mV
$I_{INRUSH(VIN)}$	Input Inrush Current at Start-Up	$I_{OUT} = 0\text{A}$ , $C_{IN} = 22\mu\text{F} \times 3$ , $C_{SS} = 0.01\mu\text{F}$ , $C_{OUT} = 100\mu\text{F} \times 3$ , $V_{OUT1} = 1.5\text{V}$ , $V_{OUT2} = 1.5\text{V}$			1		A
$I_Q(VIN)$	Input Supply Bias Current	$V_{IN} = 12\text{V}$ , $V_{OUT} = 1.2\text{V}$ , Burst Mode Operation $V_{IN} = 12\text{V}$ , $V_{OUT} = 1.2\text{V}$ , Pulse-Skipping Mode $V_{IN} = 12\text{V}$ , $V_{OUT} = 1.2\text{V}$ , Switching Continuous Shutdown, RUN = 0, $V_{IN} = 12\text{V}$			4.5 25 240 35		mA mA mA $\mu\text{A}$
$I_S(VIN)$	Input Supply Current	$V_{IN} = 4.5\text{V}$ , $V_{OUT} = 1.2\text{V}$ , $I_{OUT} = 25\text{A}$ $V_{IN} = 12\text{V}$ , $V_{OUT} = 1.2\text{V}$ , $I_{OUT} = 25\text{A}$			8.4 3.2		A A
<b>Output Specifications</b>							
$I_{OUT1(DC)}$ , $I_{OUT2(DC)}$	Output Continuous Current Range	$V_{IN} = 12\text{V}$ , $V_{OUT} = 1.2\text{V}$ (Note 6)		0		25	A
$\Delta V_{OUT1(LINE)}/V_{OUT1}$ $\Delta V_{OUT2(LINE)}/V_{OUT2}$	Line Regulation Accuracy	$V_{OUT} = 1.2\text{V}$ , $V_{IN}$ from 4.5V to 15V, $I_{OUT} = 0\text{A}$ for Each Output	●		0.01	0.1	%/V
$\Delta V_{OUT1}/V_{OUT1}$ $\Delta V_{OUT2}/V_{OUT2}$	Load Regulation Accuracy	For Each Output, $V_{OUT} = 1.2\text{V}$ , 0A to 25A, $V_{IN} = 12\text{V}$ (Note 6)	●		0.5	0.75	%
$V_{OUT1(AC)}$ , $V_{OUT2(AC)}$	Output Ripple Voltage	For Each Output, $I_{OUT} = 0\text{A}$ , $C_{OUT} = 100\mu\text{F} \times 3$ Ceramic, 470 $\mu\text{F}$ POSCAP, $V_{IN} = 12\text{V}$ , $V_{OUT} = 1.2\text{V}$ , Frequency = 500kHz			15		mV <sub>p-p</sub>
$f_S$ (Each Channel)	Output Ripple Voltage Frequency	$V_{IN} = 12\text{V}$ , $V_{OUT} = 1.2\text{V}$ , $f_{SET} = 1.25\text{V}$ (Note 4)			500		kHz
$f_{SYNC}$ (Each Channel)	SYNC Capture Range			400		780	kHz
$\Delta V_{OUTSTART}$ (Each Channel)	Turn-On Overshoot	$C_{OUT} = 100\mu\text{F}$ Ceramic, 470 $\mu\text{F}$ POSCAP, $V_{OUT} = 1.2\text{V}$ , $I_{OUT} = 0\text{A}$ , $V_{IN} = 12\text{V}$			10		mV
$t_{START}$ (Each Channel)	Turn-On Time	$C_{OUT} = 100\mu\text{F}$ Ceramic, 470 $\mu\text{F}$ POSCAP, No Load, TRACK/SS with 0.01 $\mu\text{F}$ to GND, $V_{IN} = 12\text{V}$			5		ms
$\Delta V_{OUT(LS)}$ (Each Channel)	Peak Deviation for Dynamic Load	Load: 0% to 50% to 0% of Full Load, $C_{OUT} = 22\mu\text{F} \times 3$ Ceramic, 470 $\mu\text{F}$ POSCAP, $V_{IN} = 12\text{V}$ , $V_{OUT} = 1.5\text{V}$			30		mV
$t_{SETTLE}$ (Each Channel)	Settling Time for Dynamic Load Step	Load: 0% to 50% to 0% of Full Load, $V_{IN} = 12\text{V}$ , $C_{OUT} = 100\mu\text{F}$ , 470 $\mu\text{F}$ POSCAP			20		$\mu\text{s}$
$I_{OUT(PK)}$ (Each Channel)	Output Current Limit	$V_{IN} = 12\text{V}$ , $V_{OUT} = 1.2\text{V}$			35		A

**ELECTRICAL CHARACTERISTICS** The ● denotes the specifications which apply over the specified internal operating temperature range. Specified as each individual output channel.  $T_A = 25^\circ\text{C}$  (Note 2),  $V_{IN} = 12\text{V}$  and  $V_{RUN1}$ ,  $V_{RUN2}$  at 5V unless otherwise noted. Per the typical application in Figure 22.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	
<b>Control Section</b>							
$V_{FB1}$ , $V_{FB2}$	Voltage at $V_{FB}$ Pins	$I_{OUT} = 0\text{A}$ , $V_{OUT} = 1.2\text{V}$	● 0.594	0.600	0.606	V	
$I_{FB}$		(Note 5)		-5	-20	nA	
$V_{OVL}$	Feedback Overvoltage Lockout		● 0.64	0.66	0.68	V	
TRACK1 (I), TRACK2 (I)	Track Pin Soft-Start Pull-Up Current	TRACK1 (I), TRACK2 (I) Start at 0V		1	1.25	1.5	$\mu\text{A}$
UVLO	Undervoltage Lockout (Falling)			3.3		V	
UVLO Hysteresis				0.6		V	
$t_{ON(MIN)}$	Minimum On-Time	(Note 5)		90		ns	
$R_{FBH1}$ , $R_{FBH2}$	Resistor Between $V_{OUTS1}$ , $V_{OUTS2}$ and $V_{FB1}$ , $V_{FB2}$ Pins for Each Output		60.05	60.4	60.75	$\text{k}\Omega$	
$V_{PGOOD1}$ , $V_{PGOOD2}$ Low	PGOOD Voltage Low	$I_{PGOOD} = 2\text{mA}$		0.1	0.3	V	
$I_{PGOOD}$	PGOOD Leakage Current	$V_{PGOOD} = 5\text{V}$			$\pm 5$	$\mu\text{A}$	
$V_{PGOOD}$	PGOOD Trip Level	$V_{FB}$ with Respect to Set Output Voltage: $V_{FB}$ Ramping Negative $V_{FB}$ Ramping Positive		-10 10		% %	
<b>INTV<sub>CC</sub> Linear Regulator</b>							
$V_{INTVCC}$	Internal $V_{CC}$ Voltage	$6\text{V} < V_{IN} < 15\text{V}$	4.8	5	5.2	V	
$V_{INTVCC}$ Load Regulation	INTV <sub>CC</sub> Load Regulation	$I_{CC} = 0\text{mA}$ to 50mA		0.75	2	%	
$V_{EXTVCC}$	EXTV <sub>CC</sub> Switchover Voltage	EXTV <sub>CC</sub> Ramping Positive	4.5	4.7		V	
$V_{EXTVCC(DROP)}$	EXTV <sub>CC</sub> Dropout	$I_{CC} = 20\text{mA}$ , $V_{EXTVCC} = 5\text{V}$		50	100	mV	
$V_{EXTVCC(HYST)}$	EXTV <sub>CC</sub> Hysteresis			220		mV	
<b>Oscillator and Phase-Locked Loop</b>							
Frequency Nominal	Nominal Frequency	$f_{SET} = 1.2\text{V}$	450	500	550	kHz	
Frequency Low	Lowest Frequency	$f_{SET} = 0.93\text{V}$		400		kHz	
Frequency High	Highest Frequency	$f_{SET} > 2.4\text{V}$ , Up to INTV <sub>CC</sub>		780		kHz	
$f_{SET}$	Frequency Set Current		9	10	11	$\mu\text{A}$	
$R_{MODE\_PLLIN}$	MODE_PLLIN Input Resistance			250		$\text{k}\Omega$	
CLKOUT	Phase (Relative to $V_{OUT1}$ )	PHASMD = GND PHASMD = Float PHASMD = INTV <sub>CC</sub>		60 90 120		Deg Deg Deg	
CLK High	Clock High Output Voltage		2			V	
CLK Low	Clock Low Output Voltage				0.2	V	

**ELECTRICAL CHARACTERISTICS** The ● denotes the specifications which apply over the specified internal operating temperature range. Specified as each individual output channel.  $T_A = 25^\circ\text{C}$  (Note 2),  $V_{IN} = 12\text{V}$  and  $V_{RUN1}, V_{RUN2}$  at 5V unless otherwise noted. Per the typical application in Figure 22.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
<b>Differential Amplifier</b>						
$A_V$ Differential Amplifier	Gain			1		V/V
$R_{IN}$	Input Resistance	Measured at DIFFP Input		80		$k\Omega$
$V_{OS}$	Input Offset Voltage	$V_{DIFFP} = V_{DIFFOUT} = 1.5\text{V}$ , $I_{DIFFOUT} = 100\mu\text{A}$			3	mV
PSRR Differential Amplifier	Power Supply Rejection Ratio	$5\text{V} < V_{IN} < 15\text{V}$		90		dB
$I_{CL}$	Maximum Output Current			3		mA
$V_{OUT(MAX)}$	Maximum Output Voltage	$I_{DIFFOUT} = 300\mu\text{A}$	$INTV_{CC} - 1.4$			V
GBW	Gain Bandwidth Product			3		MHz
$V_{TEMP}$	Diode Connected PNP	$I = 100\mu\text{A}$		0.6		V
TC	Temperature Coefficient		●	-2.2		mV/C

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** The LTM4650 is tested under pulsed load conditions such that  $T_J \approx T_A$ . The LTM4650E is guaranteed to meet specifications from  $0^\circ\text{C}$  to  $125^\circ\text{C}$  internal temperature. Specifications over the  $-40^\circ\text{C}$  to  $125^\circ\text{C}$  internal operating temperature range are assured by design, characterization and correlation with statistical process controls. The LTM4650I is guaranteed over the full  $-40^\circ\text{C}$  to  $125^\circ\text{C}$  internal operating temperature range. The LTM4650MP is tested and guaranteed over the  $-55^\circ\text{C}$  to  $125^\circ\text{C}$  internal operating temperature range. Note that the

maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors.

**Note 3:** Two outputs are tested separately and the same testing condition is applied to each output.

**Note 4:** LTM4650 device is designed to operate from 400kHz to 750kHz.

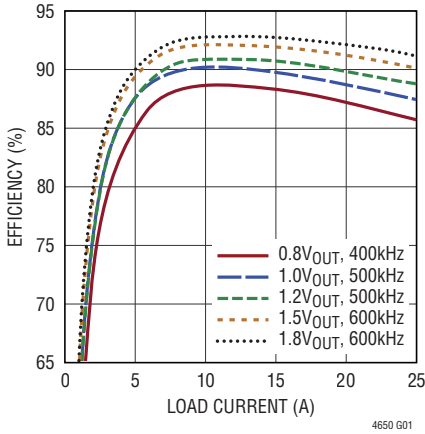
**Note 5:** These parameters are tested at wafer sort.

**Note 6:** See output current derating curves for different  $V_{IN}$ ,  $V_{OUT}$  and  $T_A$ .

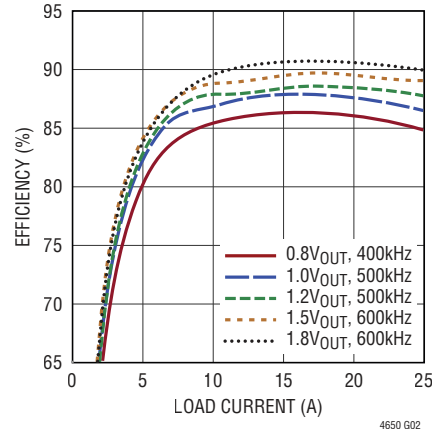
**Note 7:** Total DC output voltage error includes all errors over temperature: line and load regulation as well as the tolerance of the integrated top feedback resistor.

**TYPICAL PERFORMANCE CHARACTERISTICS**

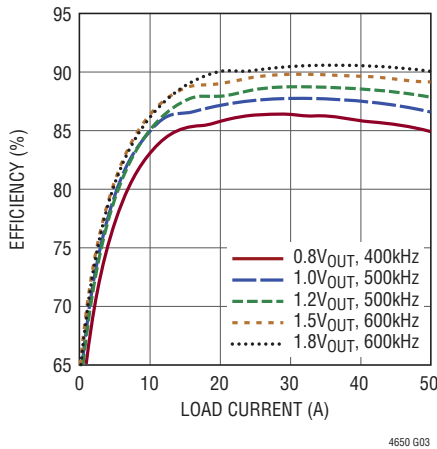
**Efficiency vs Output Current,  
 $V_{IN} = 5V$**



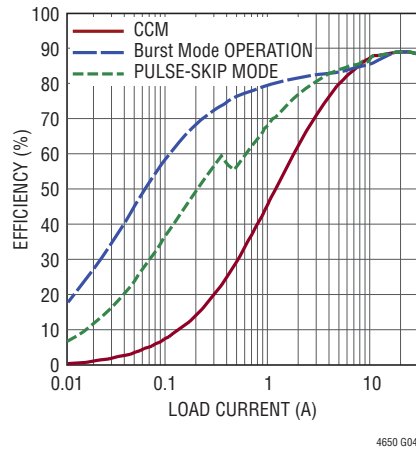
**Efficiency vs Output Current,  
 $V_{IN} = 12V$**



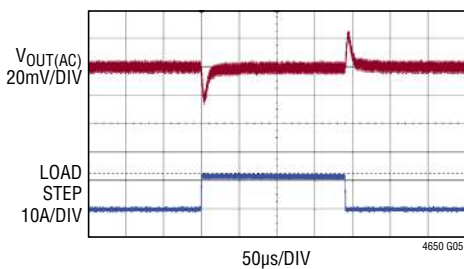
**Dual Phase Single Output Efficiency  
vs Output Current,  $V_{IN} = 12V$ ,  
 $f_s = 500kHz$**



**Burst Mode and Pulse-Skip Mode  
Efficiency  $V_{IN}=12V$ ,  $V_{OUT} = 1.2V$ ,  
 $f_s = 500kHz$**

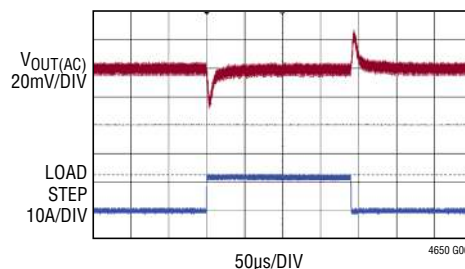


**1V Dual Phase Single Output  
Load Transient Response**



12VIN, 1VOUT, 500kHz, 12.5A LOAD STEP  
10A/µs STEP-UP AND STEP-DOWN  
COUT = 220µF ×8 CERAMIC  
CFF = 470pF

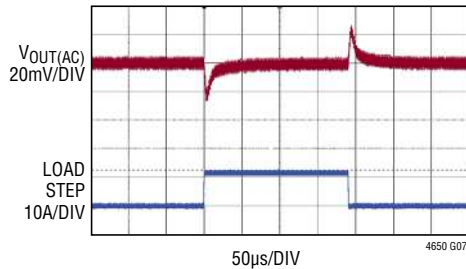
**1.2V Dual Phase Single Output  
Load Transient Response**



12VIN, 1.2VOUT, 500kHz, 12.5A LOAD STEP  
10A/µs STEP-UP AND STEP-DOWN  
COUT = 220µF ×8 CERAMIC  
CFF = 470pF

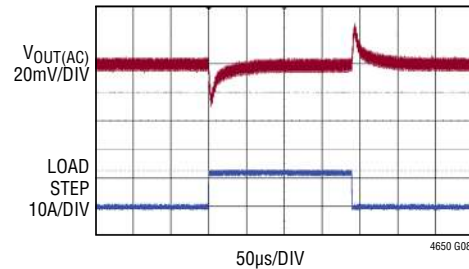
## TYPICAL PERFORMANCE CHARACTERISTICS

### 1.5V Dual Phase Single Output Load Transient Response



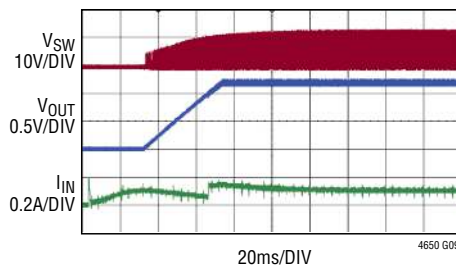
12V<sub>IN</sub>, 1.5V<sub>OUT</sub>, 600kHz, 12.5A LOAD STEP  
10A/µs STEP-UP AND STEP-DOWN  
C<sub>OUT</sub> = 220µF ×8 CERAMIC  
C<sub>FF</sub> = 470pF

### 1.8V Dual Phase Single Output Load Transient Response



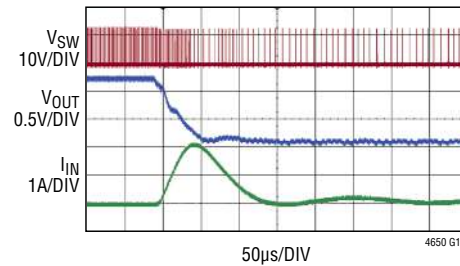
12V<sub>IN</sub>, 1.8V<sub>OUT</sub>, 600kHz, 12.5A LOAD STEP  
10A/µs STEP-UP AND STEP-DOWN  
C<sub>OUT</sub> = 220µF ×8 CERAMIC  
C<sub>FF</sub> = 470pF

### Single Phase Start-Up with No load



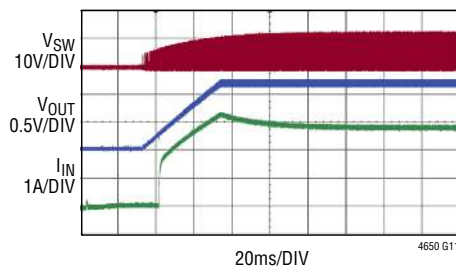
12V<sub>IN</sub>, 1.2V<sub>OUT</sub>, 500kHz  
C<sub>OUT</sub> = 470µF ×1 POSCAP + ×2 100µF CERAMIC  
C<sub>SS</sub> = 0.1µF

### Single Phase Short-Circuit Protection with No load



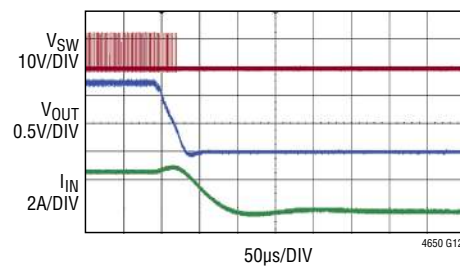
12V<sub>IN</sub>, 1.2V<sub>OUT</sub>, 500kHz  
C<sub>OUT</sub> = 470µF ×1 POSCAP + ×2 100µF CERAMIC  
C<sub>SS</sub> = 0.1µF

### Single Phase Start-Up with 25A



12V<sub>IN</sub>, 1.2V<sub>OUT</sub>, 500kHz  
C<sub>OUT</sub> = 1470µF ×1 POSCAP + ×2 100µF CERAMIC  
C<sub>SS</sub> = 0.1µF

### Single Phase Short-Circuit Protection with 25A



12V<sub>IN</sub>, 1.2V<sub>OUT</sub>, 500kHz  
C<sub>OUT</sub> = 470µF ×1 POSCAP + ×2 100µF CERAMIC



## PIN FUNCTIONS (Recommended to use test points to monitor signal pin connections.)



**PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG  $\mu$ Module PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY.**

**$V_{OUT1}$  (A1-A5, B1-B5, C1-C4):** Power Output Pins. Apply output load between these pins and GND pins. Recommend placing output decoupling capacitance directly between these pins and GND pins. Review Table 4.

**GND (A6-A7, B6-B7, D1-D4, D9-D12, E1-E4, E10-E12, F1-F3, F10-F12, G1, G3, G10, G12, H1-H7, H9-H12, J1, J5, J8, J12, K1, K5-K8, K12, L1, L12, M1, M12):** Power Ground Pins for Both Input and Output Returns.

**$V_{OUT2}$  (A8-A12, B8-B12, C9-C12):** Power Output Pins. Apply output load between these pins and GND pins. Recommend placing output decoupling capacitance directly between these pins and GND pins. Review Table 4.

**$V_{OUTS1}$ ,  $V_{OUTS2}$  (C5, C8):** This pin is connected to the top of the internal top feedback resistor for each output. The pin can be directly connected to its specific output, or connected to DIFFOUT when the remote sense amplifier is used. In paralleling modules, one of the  $V_{OUTS}$  pins is connected to the DIFFOUT pin in remote sensing or directly to  $V_{OUT}$  with no remote sensing. It is very important to connect these pins to either the DIFFOUT or  $V_{OUT}$  since this is the feedback path, and cannot be left open. See the Applications Information section.

**$f_{SET}$  (C6):** Frequency Set Pin. A 10 $\mu$ A current is sourced from this pin. A resistor from this pin to ground sets a voltage that in turn programs the operating frequency. Alternatively, this pin can be driven with a DC voltage that can set the operating frequency. See the Applications Information section.

**SGND (C7, D6, G6-G7, F6-F7):** Signal Ground Pin. Return ground path for all analog and low power circuitry. Tie a single connection to the output capacitor GND in the application. See layout guidelines in Figure 21.

**$V_{FB1}$ ,  $V_{FB2}$  (D5, D7):** The Negative Input of the Error Amplifier for Each Channel. Internally, this pin is connected to  $V_{OUTS1}$  or  $V_{OUTS2}$  with a 60.4k $\Omega$  precision resistor. Different output voltages can be programmed with an additional resistor between  $V_{FB}$  and GND pins. In PolyPhase<sup>®</sup> operation, tying the  $V_{FB}$  pins together allows for parallel operation. See the Applications Information section for details.

**TRACK1, TRACK2 (E5, D8):** Output Voltage Tracking Pin and Soft-Start Inputs. Each channel has a 1.3 $\mu$ A pull-up current source. When one channel is configured to be main of the two channels, then a capacitor from this pin to ground will set a soft-start ramp rate. The remaining channel can be set up as the subordinate, and have the main's output applied through a voltage divider to the subordinate output's track pin. This voltage divider is equal to the subordinate output's feedback divider for coincidental tracking. See the Applications Information section.

**COMP1, COMP2 (E6, E7):** Current control threshold and error amplifier compensation point for each channel. The current comparator threshold increases with this control voltage. Tie the COMP pins together for parallel operation. The device is internal compensated.

**DIFFP (E8):** Positive input of the remote sense amplifier. This pin is connected to the remote sense point of the output voltage. See the Applications Information section.

**DIFFN (E9):** Negative input of the remote sense amplifier. This pin is connected to the remote sense point of the output GND. See the Applications Information section.

**MODE\_PLLIN (F4):** Force Continuous Mode, Burst Mode Operation, or Pulse-Skipping Mode Selection Pin and External Synchronization Input to Phase Detector Pin. Connect this pin to SGND to force both channels into force continuous mode of operation. Connect to INTV<sub>CC</sub>



## PIN FUNCTIONS (Recommended to use test points to monitor signal pin connections.)

to enable pulse-skipping mode of operation. Leaving the pin floating will enable Burst Mode operation. A clock on the pin will force both channels into continuous mode of operation and synchronized to the external clock applied to this pin.

**RUN1, RUN2 (F5, F9):** Run Control Pin. A voltage above 1.25V will turn on each channel in the module. A voltage below 1.25V on the RUN pin will turn off the related channel. Each RUN pin has a 1 $\mu$ A pull-up current, once the RUN pin reaches 1.2V an additional 4.5 $\mu$ A pull-up current is added to this pin.

**DIFFOUT (F8):** Internal Remote Sense Amplifier Output. Connect this pin to  $V_{OUTS1}$  or  $V_{OUTS2}$  depending on which output is using remote sense. In parallel operation connect one of the  $V_{OUTS}$  pin to DIFFOUT for remote sensing.

**SW1, SW2 (G2, G11):** Switching node of each channel that is used for testing purposes. Also an R-C snubber network can be applied to reduce or eliminate switch node ringing, or otherwise leave floating. See the Applications Information section.

**PHASMD (G4):** Connect this pin to SGND,  $INTV_{CC}$ , or floating this pin to select the phase of CLKOUT to 60 degrees, 120 degrees, and 90 degrees respectively.

**CLKOUT (G5):** Clock output with phase control using the PHASMD pin to enable multiphase operation between devices. See the Applications Information section.

**PGOOD1, PGOOD2 (G9, G8):** Output Voltage Power Good Indicator. Open drain logic output that is pulled to ground when the output voltage is not within  $\pm 10\%$  of the regulation point.

**INTV<sub>CC</sub> (H8):** Internal 5V Regulator Output. The control circuits and internal gate drivers are powered from this voltage. Decouple this pin to PGND with a 4.7 $\mu$ F low ESR tantalum or ceramic.  $INTV_{CC}$  is activated when either RUN1 or RUN2 is activated.

**TEMP (J6):** Temperature Monitor. An internal diode connected NPN transistor between this pin and SGND with 10nF filtering capacitor. See the Applications Information section.

**EXTV<sub>CC</sub> (J7):** External power input that is enabled through a switch to  $INTV_{CC}$  whenever  $EXTV_{CC}$  is greater than 4.7V. Do not exceed 6V on this input, and connect this pin to  $V_{IN}$  when operating  $V_{IN}$  on 5V. An efficiency increase will occur that is a function of the  $(V_{IN} - INTV_{CC})$  multiplied by power MOSFET driver current. Typical current requirement is 30mA.  $V_{IN}$  must be applied before  $EXTV_{CC}$ , and  $EXTV_{CC}$  must be removed before  $V_{IN}$ .

**$V_{IN}$  (M2-M11, L2-L11, J2-J4, J9-J11, K2-K4, K9-K11):** Power Input Pins. Apply input voltage between these pins and GND pins. Recommend placing input decoupling capacitance directly between  $V_{IN}$  pins and GND pins.

**Heat Sink (Top Exposed Metal):** The top exposed metal is electrically unconnected.

## SIMPLIFIED BLOCK DIAGRAM

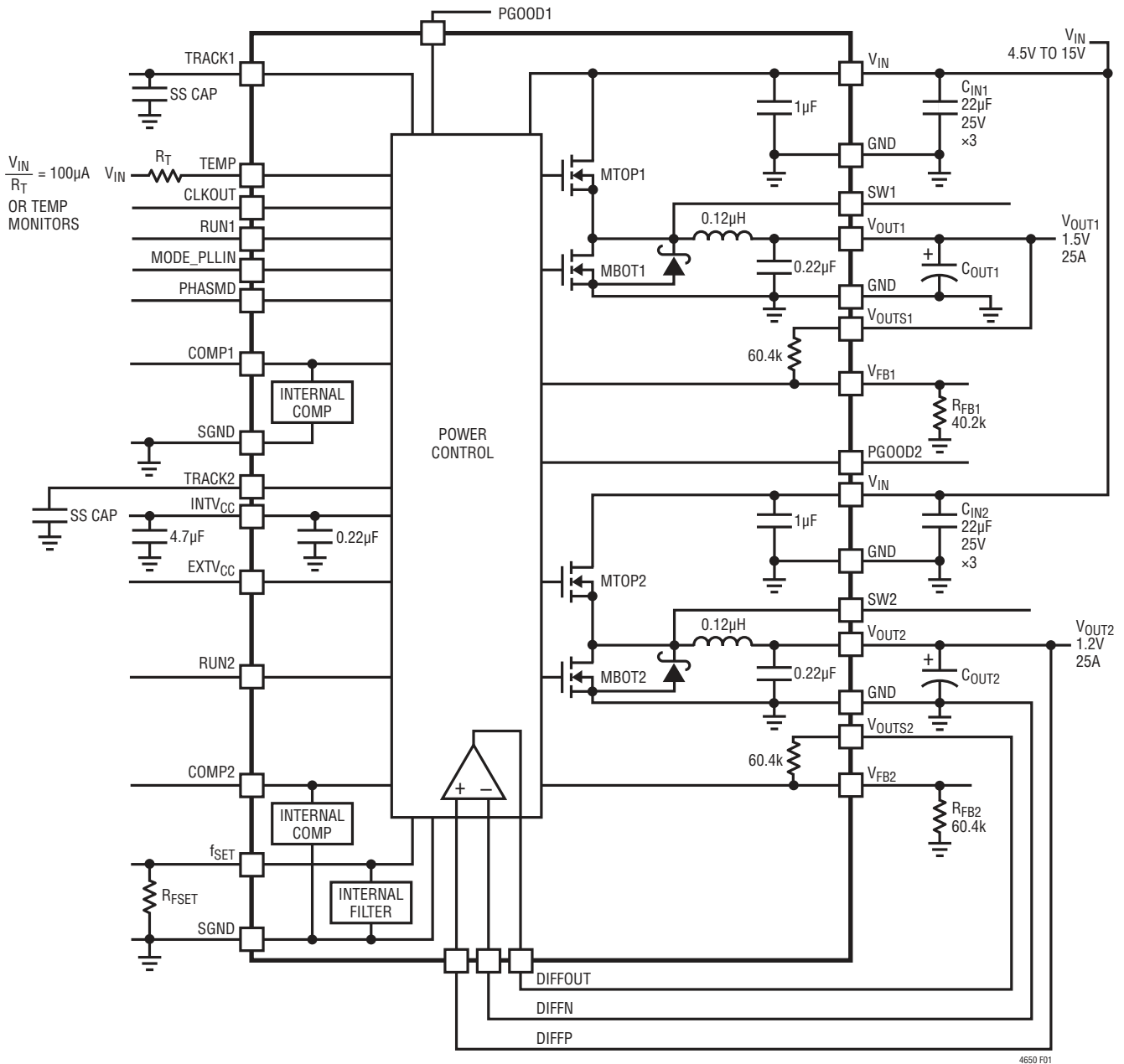


Figure 1. Simplified LTM4650 Block Diagram

## DECOUPLING REQUIREMENTS $T_A = 25^\circ\text{C}$ . Use Figure 1 configuration.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$C_{IN1}, C_{IN2}$	External Input Capacitor Requirement ( $V_{IN1} = 4.5\text{V to }15\text{V}, V_{OUT1} = 1.5\text{V}$ ) ( $V_{IN2} = 4.5\text{V to }15\text{V}, V_{OUT2} = 1.0\text{V}$ )	$I_{OUT1} = 25\text{A}$ $I_{OUT2} = 25\text{A}$	44	66		$\mu\text{F}$
$C_{OUT1}$ $C_{OUT2}$	External Output Capacitor Requirement ( $V_{IN1} = 4.5\text{V to }15\text{V}, V_{OUT1} = 1.5\text{V}$ ) ( $V_{IN2} = 4.5\text{V to }15\text{V}, V_{OUT2} = 1.0\text{V}$ )	$I_{OUT1} = 25\text{A}$ $I_{OUT2} = 25\text{A}$	600	800		$\mu\text{F}$

Rev. D

## OPERATION

### Power Module Description

The LTM4650 is a dual-output standalone nonisolated switching mode DC/DC power supply. It can provide two 25A outputs with few external input and output capacitors and setup components. This module provides precisely regulated output voltages programmable via external resistors from  $0.6V_{DC}$  to  $1.8V_{DC}$  over 4.5V to 15V input voltages. The typical application schematic is shown in Figure 22.

The LTM4650 has dual integrated constant-frequency current mode regulators and built-in power MOSFET devices with fast switching speed. The typical switching frequency is from 400kHz to 600kHz depending on output voltage. For switching-noise sensitive applications, it can be externally synchronized from 400kHz to 780kHz. A resistor can be used to program a free run frequency on the FSET pin. See the Applications Information section.

With current mode control and internal feedback loop compensation, the LTM4650 module has sufficient stability margins and good transient performance with a wide range of output capacitors, even with all ceramic output capacitors.

Current mode control provides cycle-by-cycle fast current limit and foldback current limit in an overcurrent condition. Internal overvoltage and undervoltage comparators pull the open-drain PGOOD outputs low if the output feedback voltage exits a  $\pm 10\%$  window around the regulation point. As the output voltage exceeds 10% above regulation, the bottom MOSFET will turn on to clamp the output voltage. The top MOSFET will be turned off. This overvoltage protect is feedback voltage referred.

Pulling the RUN pins below 1.1V forces the regulators into a shutdown state, by turning off both MOSFETs. The TRACK pins are used for programming the output voltage ramp and voltage tracking during start-up or used for soft-starting the regulator. See the Applications Information section.

The LTM4650 is internally compensated to be stable over all operating conditions. Table 4 provides a guide line for input and output capacitances for several operating conditions. The Analog Devices  $\mu$ Module Power Design Tool will be provided for transient and stability analysis. The  $V_{FB}$  pin is used to program the output voltage with a single external resistor to ground. A differential remote sense amplifier is available for sensing the output voltage accurately on one of the outputs at the load point, or in parallel operation sensing the output voltage at the load point.

Multiphase operation can be easily employed with the MODE\_PLLIN, PHASMD, and CLKOUT pins. Up to 12 phases can be cascaded to run simultaneously with respect to each other by programming the PHASMD pin to different levels. See the Applications Information section.

High efficiency at light loads can be accomplished with selectable Burst Mode operation or pulse-skipping operation using the MODE\_PLLIN pin. These light load features will accommodate battery operation. Efficiency graphs are provided for light load operation in the Typical Performance Characteristics section. See the Applications Information section for details.

A general purpose temperature diode is included inside the module to monitor the temperature of the module. See the Applications Information section for details.

The switch pins are available for functional operation monitoring and a resistor-capacitor snubber circuit can be carefully placed on the switch pin to ground to dampen any high frequency ringing on the transition edges. See the Applications Information section for details.

## APPLICATIONS INFORMATION

The typical LTM4650 application circuit is shown in Figure 22. External component selection is primarily determined by the maximum load current and output voltage. Refer to Table 4 for specific external capacitor requirements for particular applications.

### V<sub>IN</sub> to V<sub>OUT</sub> Step-Down Ratios

There are restrictions in the maximum V<sub>IN</sub> and V<sub>OUT</sub> step-down ratio that can be achieved for a given input voltage. Each output of the LTM4650 is capable of 98% duty cycle, but the V<sub>IN</sub> to V<sub>OUT</sub> minimum dropout is still shown as a function of its load current and will limit output current capability related to high duty cycle on the top side switch. Minimum on-time t<sub>ON(MIN)</sub> is another consideration in operating at a specified duty cycle while operating at a certain frequency due to the fact that t<sub>ON(MIN)</sub> < D/f<sub>SW</sub>, where D is duty cycle and f<sub>SW</sub> is the switching frequency. t<sub>ON(MIN)</sub> is specified in the electrical parameters as 90ns.

### Output Voltage Programming

The PWM controller has an internal 0.6V reference voltage. As shown in the Simplified Block Diagram, a 60.4kΩ internal feedback resistor connects between the V<sub>OUTS1</sub> to V<sub>FB1</sub> and V<sub>OUTS2</sub> to V<sub>FB2</sub>. It is very important that these pins be connected to their respective outputs for proper feedback regulation. Overvoltage can occur if these V<sub>OUTS1</sub> and V<sub>OUTS2</sub> pins are left floating when used as individual regulators, or at least one of them is used in paralleled regulators. The output voltage will default to 0.6V with no feedback resistor on either V<sub>FB1</sub> or V<sub>FB2</sub>. Adding a resistor R<sub>FB</sub> from V<sub>FB</sub> pin to GND programs the output voltage:

$$V_{OUT} = 0.6V \cdot \frac{60.4k + R_{FB}}{R_{FB}}$$

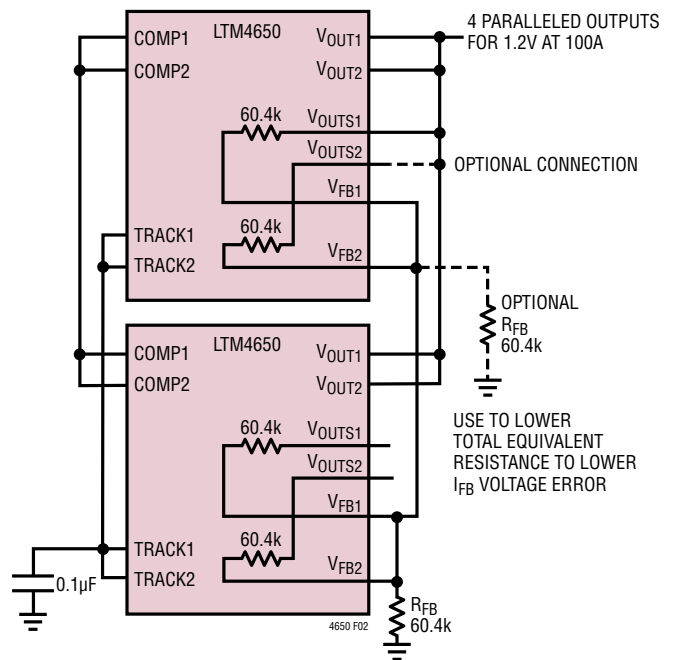
**Table 1. V<sub>FB</sub> Resistor Table vs Various Output Voltages**

V <sub>OUT</sub>	0.6V	0.8V	0.9V	1.0V	1.2V	1.5V	1.8V
R <sub>FB</sub>	Open	182k	121k	90.9k	60.4k	40.2k	30.2k

For parallel operation of multiple channels the same feedback setting resistor can be used for the parallel design. This is done by connecting the V<sub>OUTS1</sub> to the output as shown in Figure 2, thus tying one of the internal 60.4k

resistors to the output. All of the V<sub>FB</sub> pins tie together with one programming resistor as shown in Figure 2.

In parallel operation, the V<sub>FB</sub> pins have an I<sub>FB</sub> current of 20nA maximum each channel. To reduce output voltage error due to this current, an additional V<sub>OUTS</sub> pin can be tied to V<sub>OUT</sub>, and an additional R<sub>FB</sub> resistor can be used to lower the total Thevenin equivalent resistance seen by this current. For example in Figure 2, the total Thevenin equivalent resistance of the V<sub>FB</sub> pin is (60.4k//R<sub>FB</sub>), which is 30.2k where R<sub>FB</sub> is equal to 60.4k for a 1.2V output. Four phases connected in parallel equates to a worse case feedback current of 4 • I<sub>FB</sub> = 80nA maximum. The voltage error is 80nA • 30.2k = 2.4mV. If V<sub>OUTS2</sub> is connected, as shown in Figure 2, to V<sub>OUT</sub>, and another 60.4k resistor is connected from V<sub>FB2</sub> to ground, then the voltage error is reduced to 1.2mV. If the voltage error is acceptable then no additional connections are necessary. The onboard 60.4k resistor is 0.5% accurate and the V<sub>FB</sub> resistor can be chosen by the user to be as accurate as needed. All COMP pins are tied together for current sharing between the phases. The TRACK/SS pins can be tied together and a single soft-start capacitor can be used to soft-start the regulator. The soft-start



**Figure 2. 4-Phase Parallel Configurations**

## APPLICATIONS INFORMATION

equation will need to have the soft-start current parameter increased by the number of paralleled channels. See Output Voltage Tracking section.

### Input Capacitors

The LTM4650 module should be connected to a low AC-impedance DC source. For the regulator input two 22 $\mu$ F input ceramic capacitors are required for each channel for RMS ripple current. A 47 $\mu$ F to 100 $\mu$ F surface mount aluminum electrolytic bulk capacitor can be used for more input bulk capacitance. This bulk input capacitor is only needed if the input source impedance is compromised by long inductive leads, traces or not enough source capacitance. If low impedance power planes are used, then this bulk capacitor is not needed.

For a buck converter, the switching duty cycle can be estimated as:

$$D = \frac{V_{OUT}}{V_{IN}}$$

Without considering the inductor current ripple, for each output, the RMS current of the input capacitor can be estimated as:

$$I_{CIN(RMS)} = \frac{I_{OUT(MAX)}}{\eta\%} \cdot \sqrt{D \cdot (1-D)}$$

In the above equation,  $\eta\%$  is the estimated efficiency of the power module. The bulk capacitor can be a switcher-rated electrolytic aluminum capacitor, Polymer capacitor.

### Output Capacitors

The LTM4650 is designed for low output voltage ripple noise and good transient response. The bulk output capacitors defined as  $C_{OUT}$  are chosen with low enough effective series resistance (ESR) to meet the output voltage ripple and transient requirements.  $C_{OUT}$  can be a low ESR tantalum capacitor, the low ESR polymer capacitor or ceramic capacitor. The typical output capacitance range for each output is from 400 $\mu$ F to 600 $\mu$ F. Additional output filtering may be required by the system designer, if further reduction of output ripples or dynamic transient spikes is required. Table 4 shows a matrix of different output voltages and output capacitors to minimize the

voltage droop and overshoot during a 12.5A (25%) load step transient. The table optimizes total equivalent ESR and total bulk capacitance to optimize the transient performance. Stability criteria are considered in the Table 4 matrix, and the Analog Devices LTpowerCAD Design Tool will be provided for stability analysis. Multiphase operation will reduce effective output ripple as a function of the number of phases. [Application Note 77](#) discusses this noise reduction versus output ripple current cancellation, but the output capacitance should be considered carefully as a function of stability and transient response. The Analog Devices  $\mu$ Module Power Design Tool can calculate the output ripple reduction as the number of implemented phases increases by N times. A small value 10 $\Omega$  to 50 $\Omega$  resistor can be placed in series from  $V_{OUT}$  to the  $V_{OUTS}$  pin to allow for a bode plot analyzer to inject a signal into the control loop and validate the regulator stability. The same resistor could be placed in series from  $V_{OUT}$  to DIFFP and a bode plot analyzer could inject a signal into the control loop and validate the regulator stability.

### Burst Mode Operation

The LTM4650 is capable of Burst Mode operation on each regulator in which the power MOSFETs operate intermittently based on load demand, thus saving quiescent current. For applications where maximizing the efficiency at very light loads is a high priority, Burst Mode operation should be applied. Burst Mode operation is enabled with the MODE\_PLLIN pin floating. During this operation, the peak current of the inductor is set to approximately one third of the maximum peak current value in normal operation even though the voltage at the COMP pin indicates a lower value. The voltage at the COMP pin drops when the inductor's average current is greater than the load requirement. As the COMP voltage drops below 0.5V, the BURST comparator trips, causing the internal sleep line to go high and turn off both power MOSFETs.

In sleep mode, the internal circuitry is partially turned off, reducing the quiescent current to about 450 $\mu$ A for each output. The load current is now being supplied from the output capacitors. When the output voltage drops, causing COMP to rise above 0.5V, the internal sleep line goes low, and the LTM4650 resumes normal operation. The



## APPLICATIONS INFORMATION

next oscillator cycle will turn on the top power MOSFET and the switching cycle repeats. Either regulator can be configured for Burst Mode operation.

### Pulse-Skipping Mode Operation

In applications where low output ripple and high efficiency at intermediate currents are desired, pulse-skipping mode should be used. Pulse-skipping operation allows the LTM4650 to skip cycles at low output loads, thus increasing efficiency by reducing switching loss. Tying the MODE\_PLLIN pin to INTV<sub>CC</sub> enables pulse-skipping operation. At light loads the internal current comparator may remain tripped for several cycles and force the top MOSFET to stay off for several cycles, thus skipping cycles. The inductor current does not reverse in this mode. This mode will maintain higher effective frequencies thus lower output ripple and lower noise than Burst Mode operation. Either regulator can be configured for pulse-skipping mode.

### Forced Continuous Operation

In applications where fixed frequency operation is more critical than low current efficiency, and where the lowest output ripple is desired, forced continuous operation should be used. Forced continuous operation can be enabled by tying the MODE\_PLLIN pin to GND. In this mode, inductor current is allowed to reverse during low output loads, the COMP voltage is in control of the current comparator threshold throughout, and the top MOSFET always turns on with each oscillator pulse. During start-up, forced continuous mode is disabled and inductor current is prevented from reversing until the LTM4650's output voltage is in regulation. Either regulator can be configured for force continuous mode.

### Multiphase Operation

For output loads that demand more than 25A of current, two outputs in LTM4650 or even multiple LTM4650s can be paralleled to run out of phase to provide more output current without increasing input and output voltage ripples. The MODE\_PLLIN pin allows the LTM4650 to synchronize to an external clock (between 400kHz and 780kHz) and the internal phase-locked-loop allows the LTM4650 to lock onto incoming clock phase as well. The CLKOUT signal can be connected to the MODE\_PLLIN pin

of the following stage to line up both the frequency and the phase of the entire system. Tying the PHASMD pin to INTV<sub>CC</sub>, SGND, or (floating) generates a phase difference (between MODE\_PLLIN and CLKOUT) of 120 degrees, 60 degrees, or 90 degrees respectively. A total of 12 phases can be cascaded to run simultaneously with respect to each other by programming the PHASMD pin of each LTM4650 channel to different levels. Figure 3 shows a 2-phase design, 4-phase design and a 6-phase design example for clock phasing with the PHASMD table.

A multiphase power supply significantly reduces the amount of ripple current in both the input and output capacitors. The RMS input ripple current is reduced by, and the effective ripple frequency is multiplied by, the number of phases used (assuming that the input voltage is greater than the number of phases used times the output voltage). The output ripple amplitude is also reduced by the number of phases used when all of the outputs are tied together to achieve a single high output current design.

The LTM4650 device is an inherently current mode controlled device, so parallel modules will have very good current sharing. This will balance the thermals on the design. Figure 26 shows an example of parallel operation and pin connection.

### Input RMS Ripple Current Cancellation

[Application Note 77](#) provides a detailed explanation of multiphase operation. The input RMS ripple current cancellation mathematical derivations are presented, and a graph is displayed representing the RMS ripple current reduction as a function of the number of interleaved phases. Figure 4 shows this graph.

### Frequency Selection and Phase-Lock Loop (MODE\_PLLIN and f<sub>SET</sub> Pins)

The LTM4650 device is operated over a range of frequencies to improve power conversion efficiency. It is recommended to operate the module at 400kHz for output voltage below 1.0V, 500kHz for output voltage between 1.0V to 1.5V and 600kHz for output voltage above 1.5V, for the best efficiency and inductor current ripple.

# APPLICATIONS INFORMATION

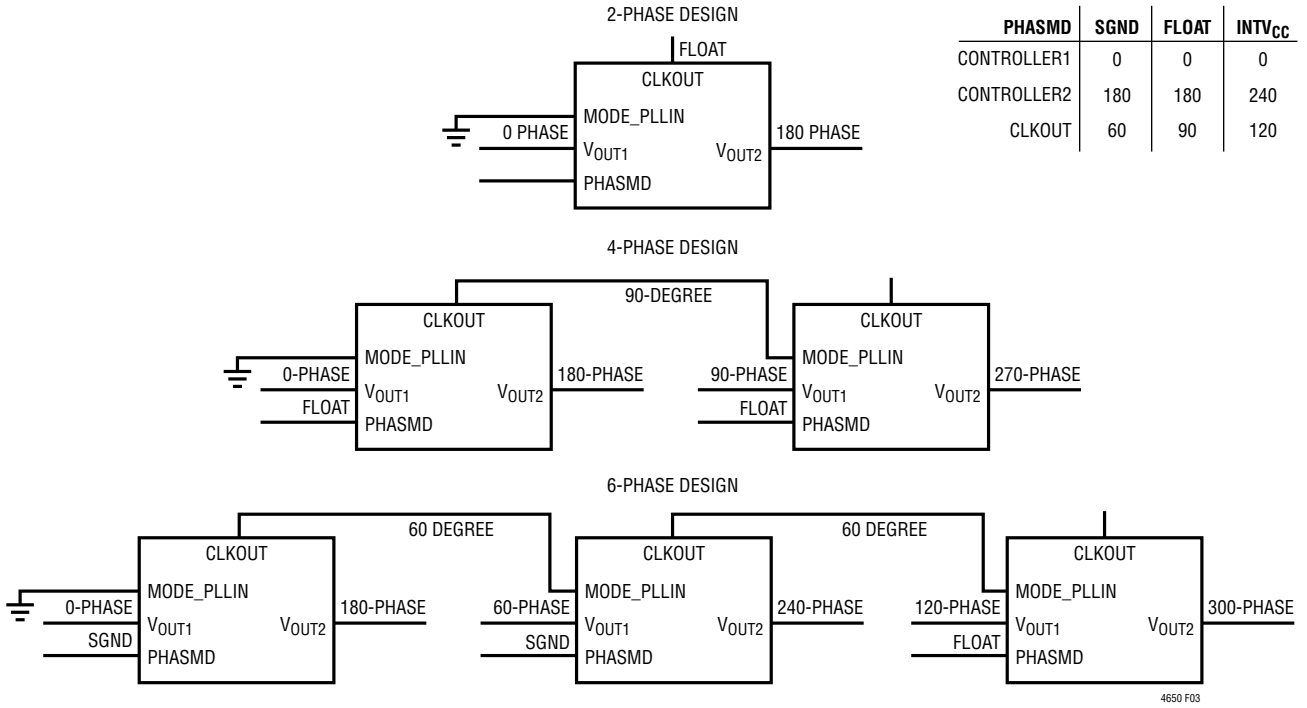


Figure 3. Examples of 2-Phase, 4-Phase, and 6-Phase Operation with PHASMD Table

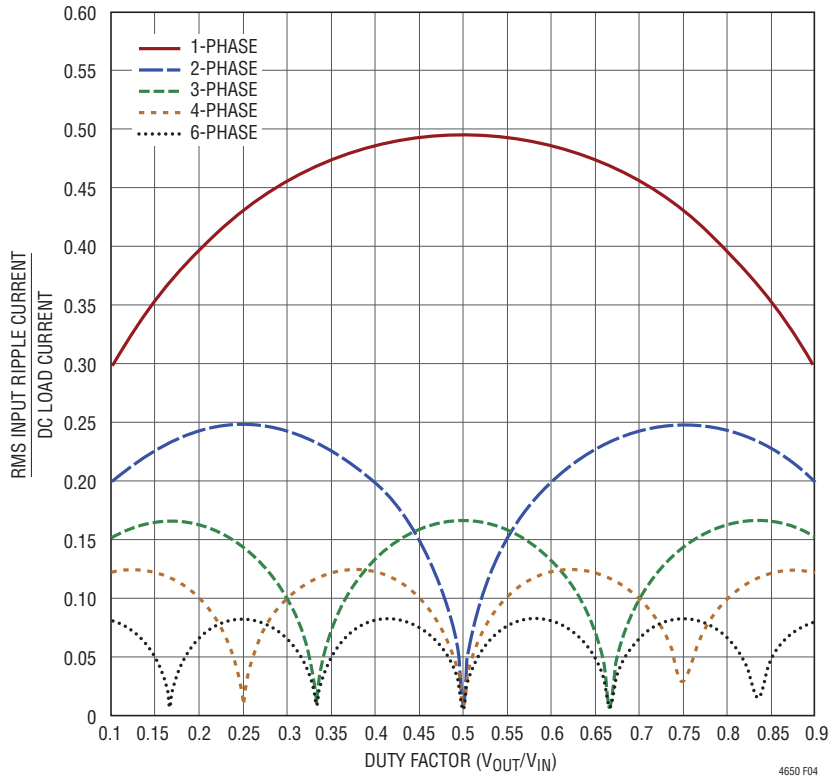


Figure 4. Input RMS Current Ratios to DC Load Current as a Function of Duty Cycle



## APPLICATIONS INFORMATION

The LTM4650 switching frequency can be set with an external resistor from the  $f_{SET}$  pin to SGND. An accurate  $10\mu\text{A}$  current source into the resistor will set a voltage that programs the frequency or a DC voltage can be applied. Figure 5 shows a graph of frequency setting verses programming voltage. An external clock can be applied to the MODE\_PLLIN pin from 0V to INTV<sub>CC</sub> over a frequency range of 400kHz to 780kHz. The clock input high threshold is 1.6V and the clock input low threshold is 1V. The LTM4650 has the PLL loop filter components on board. The frequency setting resistor should always be present to set the initial switching frequency before locking to an external clock. Both regulators will operate in continuous mode while being externally clock.

The output of the PLL phase detector has a pair of complementary current sources that charge and discharge the internal filter network. When the external clock is applied then the  $f_{SET}$  frequency resistor is disconnected with an internal switch, and the current sources control the frequency adjustment to lock to the incoming external clock. When no external clock is applied, then the internal switch is on, thus connecting the external  $f_{SET}$  frequency set resistor for free run operation.

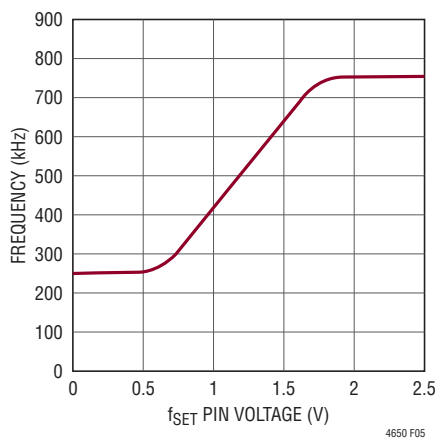


Figure 5. Operating Frequency vs  $f_{SET}$  Pin Voltage

### Minimum On-Time

Minimum on-time  $t_{ON}$  is the smallest time duration that the LTM4650 is capable of turning on the top MOSFET on either channel. It is determined by internal timing delays, and the gate charge required turning on the top MOSFET.

Low duty cycle applications may approach this minimum on-time limit and care should be taken to ensure that:

$$\frac{V_{OUT}}{V_{IN} \cdot \text{FREQ}} > t_{ON(MIN)}$$

If the duty cycle falls below what can be accommodated by the minimum on-time, the controller will begin to skip cycles. The output voltage will continue to be regulated, but the output ripple and current will increase. The on-time can be increased by lowering the switching frequency. A good rule of thumb is to keep on-time longer than 110ns.

### Output Voltage Tracking

Output voltage tracking can be programmed externally using the TRACK pins. The output can be tracked up and down with another regulator. The main regulator's output is divided down with an external resistor divider that is the same as the subordinate regulator's feedback divider to implement coincident tracking. The LTM4650 uses an accurate 60.4k resistor internally for the top feedback resistor for each channel. Figure 6 shows an example of coincident tracking. Equations:

$$\text{SUBORDINATE} = \left(1 + \frac{60.4k}{R_{TA}}\right) \cdot V_{TRACK}$$

$V_{TRACK}$  is the track ramp applied to the subordinate's track pin.  $V_{TRACK}$  has a control range of 0V to 0.6V, or the internal reference voltage. When the main's output is divided down with the same resistor values used to set the subordinate's output, then the subordinate will coincident track with the main until it reaches its final value. The main will continue to its final value from the subordinate's regulation point. Voltage tracking is disabled when  $V_{TRACK}$  is more than 0.6V.  $R_{TA}$  in Figure 6 will be equal to the  $R_{FB}$  for coincident tracking. Figure 7 shows the coincident tracking waveforms.

The TRACK pin of the main can be controlled by a capacitor placed on the main regulator TRACK pin to ground. A  $1.3\mu\text{A}$  current source will charge the TRACK pin up to the reference voltage and then proceed up to INTV<sub>CC</sub>. After the 0.6V ramp, the TRACK pin will no longer be in control, and the internal voltage reference will control output regulation from the feedback divider. Foldback current

## APPLICATIONS INFORMATION

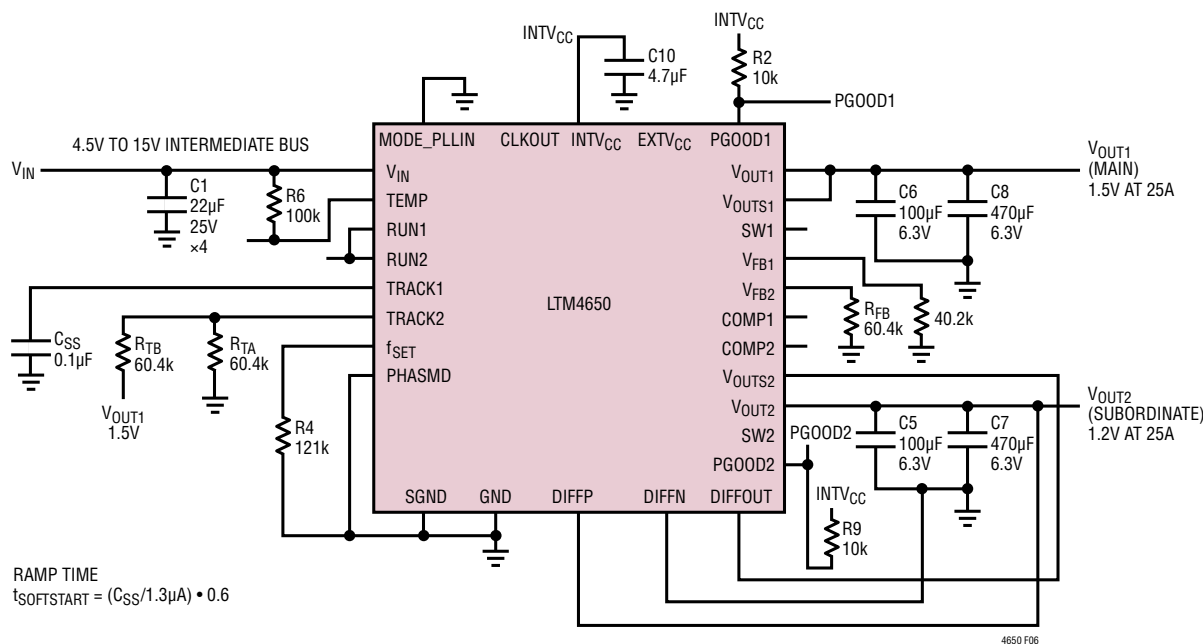


Figure 6. Example of Output Tracking Application Circuit

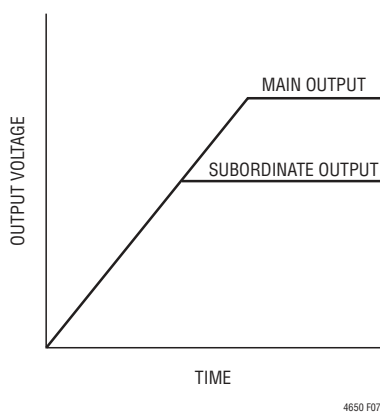


Figure 7. Output Coincident Tracking Waveform

limit is disabled during this sequence of turn-on during tracking or soft-starting. The TRACK pins are pulled low when the RUN pin is below 1.2V. The total soft-start time can be calculated as:

$$t_{\text{SOFT-START}} = \left( \frac{C_{\text{SS}}}{1.3\mu\text{A}} \right) \cdot 0.6$$

Regardless of the mode selected by the MODE\_PLLIN pin, the regulator channels will always start in pulse-skipping

mode up to TRACK = 0.5V. Between TRACK = 0.5V and 0.54V, it will operate in forced continuous mode and revert to the selected mode once TRACK > 0.54V. In order to track with another channel once in steady state operation, the LTM4650 is forced into continuous mode operation as soon as  $V_{\text{FB}}$  is below 0.54V regardless of the setting on the MODE\_PLLIN pin.

Ratiometric tracking can be achieved by a few simple calculations and the slew rate value applied to the main's TRACK pin. As mentioned above, the TRACK pin has a control range from 0 to 0.6V. The main's TRACK pin slew rate is directly equal to the main's output slew rate in Volts/Time. The equation:

$$\frac{\text{MR}}{\text{SR}} \cdot 60.4\text{k} = R_{\text{TB}}$$

where MR is the main's output slew rate and SR is the subordinate's output slew rate in Volts/Time. When coincident tracking is desired, then MR and SR are equal, thus  $R_{\text{TB}}$  is equal to the 60.4k.  $R_{\text{TA}}$  is derived from equation:

$$R_{\text{TA}} = \frac{0.6\text{V}}{\frac{V_{\text{FB}}}{60.4\text{k}} + \frac{V_{\text{FB}}}{R_{\text{FB}}} - \frac{V_{\text{TRACK}}}{R_{\text{TB}}}}$$

## APPLICATIONS INFORMATION

where  $V_{FB}$  is the feedback voltage reference of the regulator, and  $V_{TRACK}$  is 0.6V. Since  $R_{TB}$  is equal to the 60.4k top feedback resistor of the subordinate regulator in equal slew rate or coincident tracking, then  $R_{TA}$  is equal to  $R_{FB}$  with  $V_{FB} = V_{TRACK}$ . Therefore  $R_{TB} = 60.4k$ , and  $R_{TA} = 60.4k$  in Figure 6.

In ratiometric tracking, a different slew rate maybe desired for the subordinate regulator.  $R_{TB}$  can be solved for when SR is slower than MR. Make sure that the subordinate supply slew rate is chosen to be fast enough so that the subordinate output voltage will reach its final value before the main output.

For example,  $MR = 1.5V/1ms$ , and  $SR = 1.2V/1ms$ . Then  $R_{TB} = 76.8k$ . Solve for  $R_{TA}$  to equal to 49.9k.

Each of the TRACK pins will have the 1.3 $\mu$ A current source on when a resistive divider is used to implement tracking on that specific channel. This will impose an offset on the TRACK pin input. Smaller value resistors with the same ratios as the resistor values calculated from the above equation can be used. For example, where the 60.4k is used then a 6.04k can be used to reduce the TRACK pin offset to a negligible value.

### Power Good

The PGOOD pins are open drain pins that can be used to monitor valid output voltage regulation. This pin monitors a 10% window around the regulation point. A resistor can be pulled up to a particular supply voltage no greater than 6V maximum for monitoring.

### Stability Compensation

The module has already been internally compensated for all output voltages. Table 4 is provided for most application requirements. The Analog Devices  $\mu$ Module Power Design Tool will be provided for other control loop optimization.

### Run Enable

The RUN pins have an enable threshold of 1.4V maximum, typically 1.25V with 150mV of hysteresis. They control the turn on each of the channels and  $INTV_{CC}$ . These pins can be

pulled up to  $V_{IN}$  for 5V operation, or a 5V Zener diode can be placed on the pins and a 10k to 100k resistor can be placed up to higher than 5V input for enabling the channels. The RUN pins can also be used for output voltage sequencing. In parallel operation the RUN pins can be tied together and controlled from a single control. See the Typical Application circuits in Figure 22.

### $INTV_{CC}$ and $EXTV_{CC}$

The LTM4650 module has an internal 5V low dropout regulator that is derived from the input voltage. This regulator is used to power the control circuitry and the power MOSFET drivers. This regulator can source up to 70mA, and typically uses ~30mA for powering the device at the maximum frequency. This internal 5V supply is enabled by either RUN1 or RUN2.

$EXTV_{CC}$  allows an external 5V supply to power the LTM4650 and reduce power dissipation from the internal low dropout 5V regulator. The power loss savings can be calculated by:

$$(V_{IN} - 5V) \cdot 30mA = P_{LOSS}$$

$EXTV_{CC}$  has a threshold of 4.7V for activation, and a maximum rating of 6V. When using a 5V input, connect this 5V input to  $EXTV_{CC}$  also to maintain a 5V gate drive level.  $EXTV_{CC}$  must sequence on after  $V_{IN}$ , and  $EXTV_{CC}$  must sequence off before  $V_{IN}$ .

### Differential Remote Sense Amplifier

An accurate differential remote sense amplifier is provided to sense low output voltages accurately at the remote load points. This is especially true for high current loads. The amplifier can be used on one of the two channels, or on a single parallel output. It is very important that the DIFFP and DIFFN are connected properly at the output, and DIFFOUT is connected to either  $V_{OUTS1}$  or  $V_{OUTS2}$ . In parallel operation, the DIFFP and DIFFN are connected properly at the output, and DIFFOUT is connected to one of the  $V_{OUTS}$  pins. Review the parallel schematics in Figure 23 and review Figure 2.

## APPLICATIONS INFORMATION

### SW Pins

The SW pins are generally for testing purposes by monitoring these pins. These pins can also be used to dampen out switch node ringing caused by LC parasitic in the switched current paths. Usually a series R-C combination is used called a snubber circuit. The resistor will dampen the resonance and the capacitor is chosen to only affect the high frequency ringing across the resistor. If the stray inductance or capacitance can be measured or approximated then a somewhat analytical technique can be used to select the snubber values. The inductance is usually easier to predict. It combines the power path board inductance in combination with the MOSFET interconnect bond wire inductance.

First the SW pin can be monitored with a wide bandwidth scope with a high frequency scope probe. The ring frequency can be measured for its value. The impedance Z can be calculated:

$$ZL = 2\pi fL,$$

where f is the resonant frequency of the ring, and L is the total parasitic inductance in the switch path. If a resistor is selected that is equal to Z, then the ringing should be dampened. The snubber capacitor value is chosen so that its impedance is equal to the resistor at the ring frequency. Calculated by:  $ZC = 1/(2\pi fC)$ . These values are a good place to start with. Modification to these components should be made to attenuate the ringing with the least amount of power loss.

### Temperature Monitoring

Measuring the absolute temperature of a diode is possible due to the relationship between current, voltage and temperature described by the classic diode equation:

$$I_D = I_S \cdot e^{\left(\frac{V_D}{\eta \cdot V_T}\right)}$$

or

$$V_D = \eta \cdot V_T \cdot \ln \frac{I_D}{I_S}$$

where  $I_D$  is the diode current,  $V_D$  is the diode voltage,  $\eta$  is the ideality factor (typically close to 1.0) and  $I_S$  (saturation current) is a process dependent parameter.  $V_T$  can be broken out to:

$$V_T = \frac{k \cdot T}{q}$$

where T is the diode junction temperature in Kelvin, q is the electron charge and k is Boltzmann's constant.  $V_T$  is approximately 26mV at room temperature (298K) and scales linearly with Kelvin temperature. It is this linear temperature relationship that makes diodes suitable temperature sensors. The  $I_S$  term in the previous equation is the extrapolated current through a diode junction when the diode has zero volts across the terminals. The  $I_S$  term varies from process to process, varies with temperature, and by definition must always be less than  $I_D$ . Combining all of the constants into one term:

$$K_D = \frac{\eta \cdot k}{q}$$

where  $K_D = 8.62 \cdot 10^{-5}$ , and knowing  $\ln(I_D/I_S)$  is always positive because  $I_D$  is always greater than  $I_S$ , leaves us with the equation that:

$$V_D = T(\text{KELVIN}) \cdot K_D \cdot \ln \frac{I_D}{I_S}$$

where  $V_D$  appears to increase with temperature. It is common knowledge that a silicon diode biased with a current source has an approximate  $-2\text{mV}/^\circ\text{C}$  temperature relationship (Figure 8), which is at odds with the equation. In fact, the  $I_S$  term increases with temperature, reducing the  $\ln(I_D/I_S)$  absolute value yielding an approximate  $-2\text{mV}/^\circ\text{C}$  composite diode voltage slope.

To obtain a linear voltage proportional to temperature we cancel the  $I_S$  variable in the natural logarithm term to remove the  $I_S$  dependency from the equation 1. This is accomplished by measuring the diode voltage at two currents  $I_1$ , and  $I_2$ , where  $I_1 = 10 \cdot I_2$  and subtracting we get:

$$\Delta V_D = T(\text{KELVIN}) \cdot K_D \cdot \ln \frac{I_1}{I_S} - T(\text{KELVIN}) \cdot K_D \cdot \ln \frac{I_2}{I_S}$$

## APPLICATIONS INFORMATION

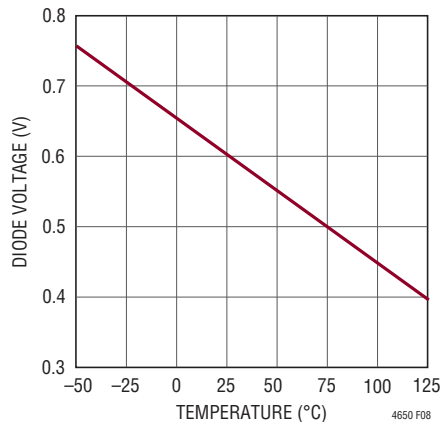


Figure 8. Diode Voltage  $V_D$  vs Temperature  $T(^{\circ}\text{C})$

Combining like terms, then simplifying the natural log terms yields:

$$\Delta V_D = T(\text{KELVIN}) \cdot K_D \cdot \ln(10)$$

and redefining constant

$$K'_D = K_D \cdot \ln(10) = \frac{198\mu\text{V}}{\text{K}}$$

yields

$$\Delta V_D = K'_D \cdot T(\text{KELVIN})$$

Solving for temperature:

$$T(\text{KELVIN}) = \frac{\Delta V_D}{K'_D} \quad (-\text{CELSIUS}) = T(\text{KELVIN}) - 273.15$$

where

$$300^{\circ}\text{K} = 27^{\circ}\text{C}$$

means that if we take the difference in voltage across the diode measured at two currents with a ratio of 10, the resulting voltage is  $198\mu\text{V}$  per Kelvin of the junction with a zero intercept at 0 Kelvin.

The diode connected PNP transistor at the TEMP pin can be used to monitor the internal temperature of the LTM4650. See Figure 23 for an example.

### Thermal Considerations and Output Current Derating

The thermal resistances reported in the Pin Configuration section of the data sheet are consistent with those parameters defined by JESD51-9 and are intended for use with finite element analysis (FEA) software modeling tools that leverage the outcome of thermal modeling, simulation, and correlation to hardware evaluation performed on a  $\mu\text{Module}$  package mounted to a hardware test board—also defined by JESD51-9 (“Test Boards for Area Array Surface Mount Package Thermal Measurements”). The motivation for providing these thermal coefficients is found in JESD 51-12 (“Guidelines for Reporting and Using Electronic Package Thermal Information”).

Many designers may opt to use laboratory equipment and a test vehicle such as the demo board to anticipate the  $\mu\text{Module}$  regulator’s thermal performance in their application at various electrical and environmental operating conditions to compliment any FEA activities. Without FEA software, the thermal resistances reported in the Pin Configuration section are in-and-of themselves not relevant to providing guidance of thermal performance; instead, the derating curves provided in the data sheet can be used in a manner that yields insight and guidance pertaining to one’s application-usage, and can be adapted to correlate thermal performance to one’s own application.

The Pin Configuration section typically gives four thermal coefficients explicitly defined in JESD 51-12; these coefficients are quoted or paraphrased below:

1.  $\theta_{JA}$ , the thermal resistance from junction to ambient, is the natural convection junction-to-ambient air thermal resistance measured in a one cubic foot sealed enclosure. This environment is sometimes referred to as “still air” although natural convection causes the air to move. This value is determined with the part mounted to a JESD 51-9 defined test board, which does not reflect an actual application or viable operating condition.
2.  $\theta_{JCbott}$ , the thermal resistance from junction to the bottom of the product case, is the junction-to-board thermal resistance with all of the component power dissipation flowing through the bottom of the package. In the typical  $\mu\text{Module}$ , the bulk of the heat flows out the bottom of the package, but there is always heat



## APPLICATIONS INFORMATION

flow out into the ambient environment. As a result, this thermal resistance value may be useful for comparing packages but the test conditions don't generally match the user's application.

3.  $\theta_{JC\text{TOP}}$ , the thermal resistance from junction to top of the product case, is determined with nearly all of the component power dissipation flowing through the top of the package. As the electrical connections of the typical  $\mu\text{Module}$  are on the bottom of the package, it is rare for an application to operate such that most of the heat flows from the junction to the top of the part. As in the case of  $\theta_{JC\text{BOTTOM}}$ , this value may be useful for comparing packages but the test conditions don't generally match the user's application.
4.  $\theta_{JB}$ , the thermal resistance from junction to the printed circuit board, is the junction-to-board thermal resistance where almost all of the heat flows through the bottom of the  $\mu\text{Module}$  and into the board, and is really the sum of the  $\theta_{JC\text{bottom}}$  and the thermal resistance of the bottom of the part through the solder joints and through a portion of the board. The board temperature is measured a specified distance from the package, using a two sided, two layer board. This board is described in JESD 51-9.

A graphical representation of the aforementioned thermal resistances is given in Figure 9; blue resistances are contained within the  $\mu\text{Module}$  regulator, whereas green resistances are external to the  $\mu\text{Module}$ .

As a practical matter, it should be clear to the reader that no individual or sub-group of the four thermal resistance parameters defined by JESD 51-12 or provided in the Pin Configuration section replicates or conveys normal operating conditions of a  $\mu\text{Module}$ . For example, in normal board-mounted applications, never does 100% of the device's total power loss (heat) thermally conduct exclusively through the top or exclusively through bottom of the  $\mu\text{Module}$ —as the standard defines for  $\theta_{JC\text{top}}$  and  $\theta_{JC\text{bottom}}$ , respectively. In practice, power loss is thermally dissipated in both directions away from the package—granted, in the absence of a heat sink and airflow, a majority of the heat flow is into the board.

Within a SIP (system-in-package) module, be aware there are multiple power devices and components dissipating power, with a consequence that the thermal resistances relative to different junctions of components or die are not exactly linear with respect to total package power loss. To reconcile this complication without sacrificing modeling simplicity—but also, not ignoring practical realities—an approach has been taken using FEA software modeling along with laboratory testing in a controlled-environment chamber to reasonably define and correlate the thermal resistance values supplied in this data sheet: (1) Initially, FEA software is used to accurately build the mechanical geometry of the  $\mu\text{Module}$  and the specified PCB with all of the correct material coefficients along with accurate power loss source definitions; (2) this model simulates a software-defined JEDEC environment consistent with JESD51-9 to predict power loss heat flow and

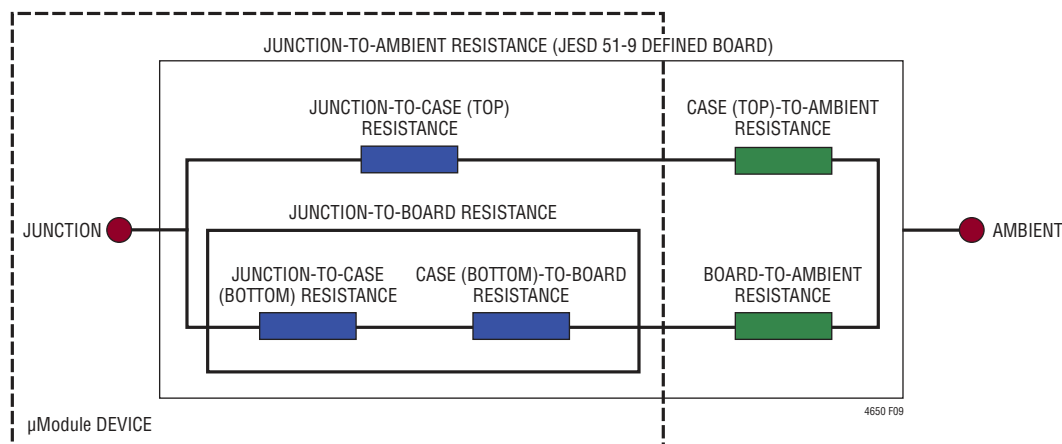


Figure 9. Graphical Representation of JESD51-12 Thermal Coefficients

## APPLICATIONS INFORMATION

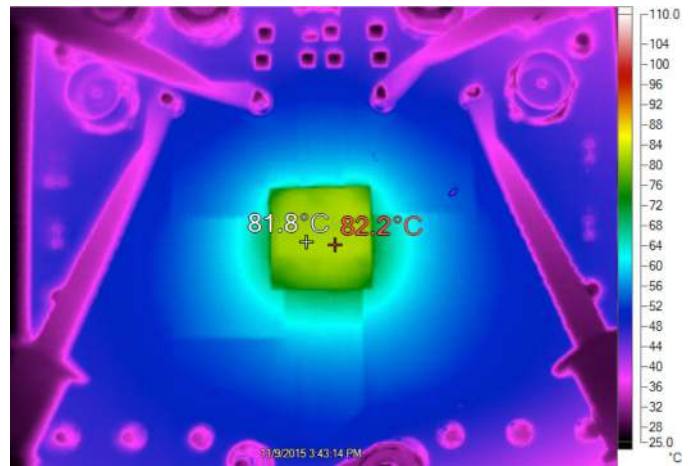
temperature readings at different interfaces that enable the calculation of the JEDEC-defined thermal resistance values; (3) the model and FEA software is used to evaluate the  $\mu$ Module with heat sink and airflow; (4) having solved for and analyzed these thermal resistance values and simulated various operating conditions in the software model, a thorough laboratory evaluation replicates the simulated conditions with thermocouples within a controlled-environment chamber while operating the device at the same power loss as that which was simulated. An outcome of this process and due-diligence yields a set of derating curves provided in other sections of this data sheet. After these laboratory test have been performed and correlated to the  $\mu$ Module model, then the  $\theta_{JB}$  and  $\theta_{BA}$  are summed together to correlate quite well with the  $\mu$ Module model with no airflow or heat sinking in a properly define chamber. This  $\theta_{JB} + \theta_{BA}$  value is shown in the Pin Configuration section and should accurately equal the  $\theta_{JA}$  value because approximately 100% of power loss flows from the junction through the board into ambient with no airflow or top mounted heat sink. Each system has its own thermal characteristics, therefore thermal analysis must be performed by the user in a particular system.

The LTM4650 module has been designed to effectively remove heat from both the top and bottom of the package. The bottom substrate material has very low thermal resistance to the printed circuit board. An external heat sink can be applied to the top of the device for excellent heat sinking with airflow.

Figure 10 shows a temperature plot of the LTM4650 with 12V input, 1.0V output at 50A without heat sink and a no airflow condition.

### Safety Considerations

The LTM4650 modules do not provide isolation from  $V_{IN}$  to  $V_{OUT}$ . There is no internal fuse. If required, a slow blow fuse with a rating twice the maximum input current needs to be provided to protect each unit from catastrophic failure. The device does support over current protection. A temperature diode is provided for monitoring internal temperature, and can be used to detect the need for thermal shutdown that can be done by controlling the RUN pin.



**Figure 10. Thermal Image 12V to 1V, 50A with No Airflow and No Heat Sink (Based on 4-Layer 101mm × 114mm PCB Board Containing 2oz Copper on the Top, Bottom and All Internal Layers)**

### Power Derating

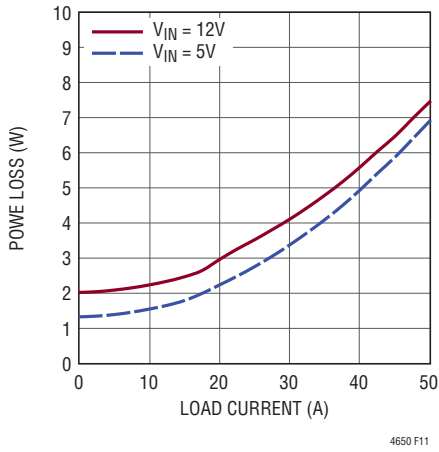
The 0.9V and 1.5V power loss curves in Figure 11 and Figure 12 can be used in coordination with the load current derating curves in Figure 13 to Figure 20 for calculating an approximate  $\theta_{JA}$  thermal resistance for the LTM4650 with various heat sinking and airflow conditions. The power loss curves are taken at room temperature, and are increased with a 1.2 multiplicative factor at 120°C.

The derating curves are plotted with CH1 and CH2 in parallel single output operation starting at 50A of load with low ambient temperature. The output voltages are 0.9V and 1.5V. These are chosen to include the lower and higher output voltage ranges for correlating the thermal resistance. Thermal models are derived from several temperature measurements in a controlled temperature chamber along with thermal modeling analysis.

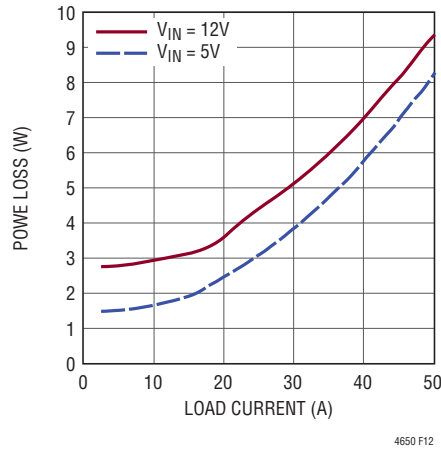
The junction temperatures are monitored while ambient temperature is increased with and without airflow. The power loss increase with ambient temperature change is factored into the derating curves. The junctions are maintained at ~120°C maximum while lowering output current or power while increasing ambient temperature. The decreased output current will decrease the internal module loss as ambient temperature is increased.



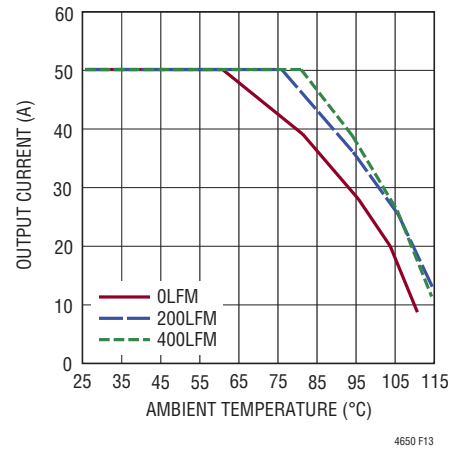
# APPLICATIONS INFORMATION



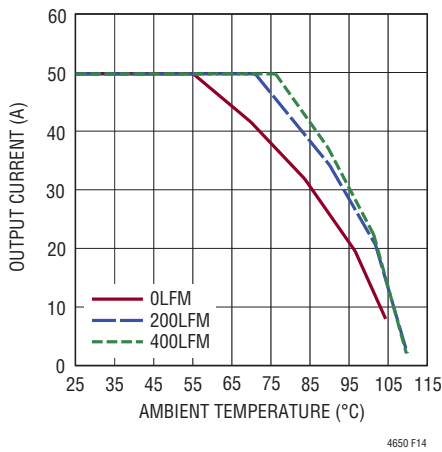
**Figure 11. 0.9V Output Power Loss Curve**



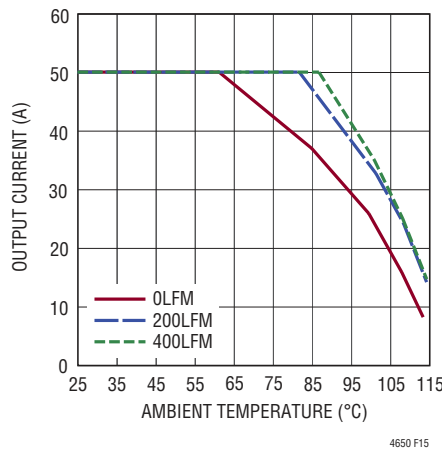
**Figure 12. 1.5V Output Power Loss Curve**



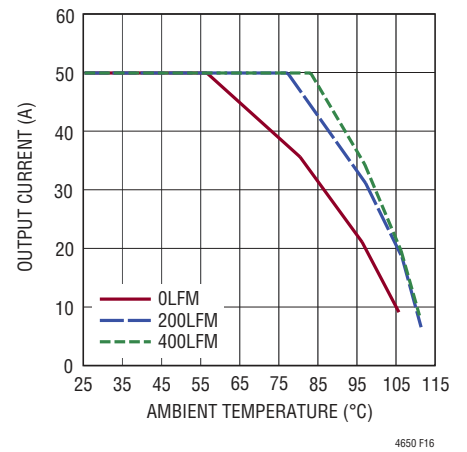
**Figure 13. 5V to 0.9V Derating Curve, No Heat Sink**



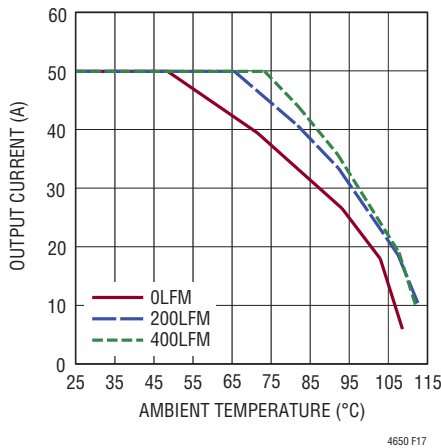
**Figure 14. 12V to 0.9V Derating Curve, No Heat Sink**



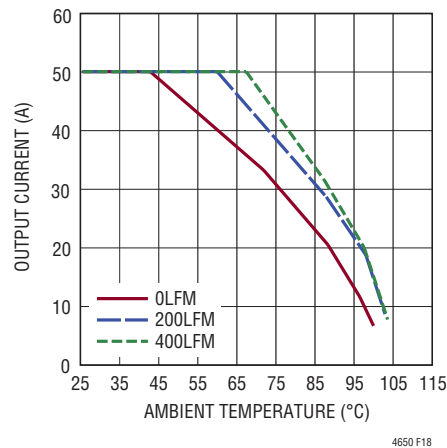
**Figure 15. 5V to 0.9V Derating Curve, BGA Heat Sink**



**Figure 16. 12V to 0.9V Derating Curve, BGA Heat Sink**

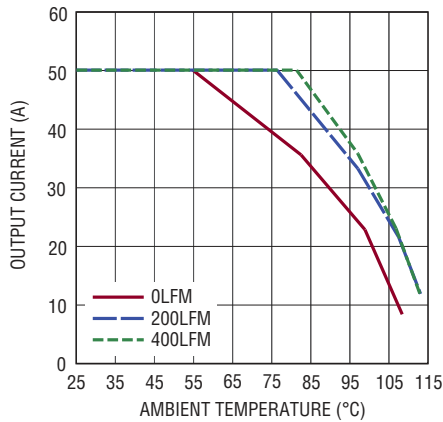


**Figure 17. 5V to 1.5V Derating Curve, No Heat Sink**

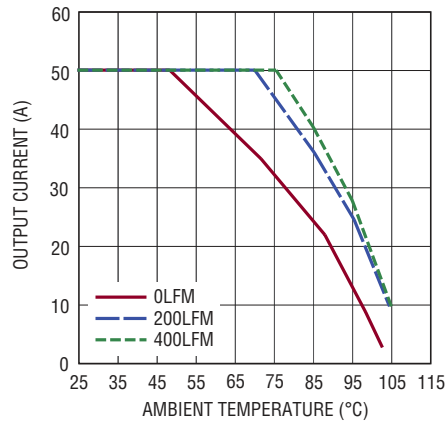


**Figure 18. 12V to 1.5V Derating Curve, No Heat Sink**

## APPLICATIONS INFORMATION



**Figure 19. 5V to 1.5V Derating Curve, BGA Heat Sink**



**Figure 20. 12V to 1.5V Derating Curve, BGA Heat Sink**

The monitored junction temperature of 120°C minus the ambient operating temperature specifies how much module temperature rise can be allowed. As an example in Figure 14, the load current is derated to ~35A at ~90°C with 200LFM air but not heat sink and the power loss for the 12V to 0.9V at 35A output is a ~5.6W loss. The 5.6W loss is calculated with the ~4.7W room temperature loss from the 12V to 0.9V power loss curve at 35A, and the 1.20 multiplying factor at 120°C junction temperature. If the 90°C ambient temperature is subtracted from the 120°C junction temperature, then the difference of 30°C divided 5.5W equals a 5.4°C/W  $\theta_{JA}$  thermal resistance. Table 2 specifies a 5.5°C/W value which is pretty close. Table 2 and

Table 3 provide equivalent thermal resistances for 0.9V and 1.5V outputs with and without airflow and heat sinking.

The derived thermal resistances in Table 2 and Table 3 for the various conditions can be multiplied by the calculated power loss as a function of ambient temperature to derive temperature rise above ambient, thus maximum junction temperature. Room temperature power loss can be derived from the efficiency curves and adjusted with the above ambient temperature multiplicative factors. The printed circuit board is a 1.6mm thick 4-layer board with 2oz copper on each layer. The PCB dimensions are 101mm × 114mm. The BGA heat sinks are listed in Table 3.

**Table 2. 0.9V Output**

DERATING CURVE	V <sub>IN</sub> (V)	POWER LOSS CURVE	AIRFLOW (LFM)	HEAT SINK	$\theta_{JA}$ (°C/W)
Figure 13, Figure 14	5, 12	Figure 11	0	None	7.5
Figure 13, Figure 14	5, 12	Figure 11	200	None	5.5
Figure 13, Figure 14	5, 12	Figure 11	400	None	5
Figure 15, Figure 16	5, 12	Figure 11	0	BGA Heat Sink	7
Figure 15, Figure 16	5, 12	Figure 11	200	BGA Heat Sink	4.5
Figure 15, Figure 16	5, 12	Figure 11	400	BGA Heat Sink	4

## APPLICATIONS INFORMATION

**Table 3. 1.5V Output**

DERATING CURVE	V <sub>IN</sub> (V)	POWER LOSS CURVE	AIRFLOW (LFM)	HEAT SINK	θ <sub>JA</sub> (°C/W)
Figure 17, Figure 18	5, 12	Figure 12	0	None	7.5
Figure 17, Figure 18	5, 12	Figure 12	200	None	5.5
Figure 17, Figure 18	5, 12	Figure 12	400	None	5
Figure 18, Figure 19	5, 12	Figure 12	0	BGA Heat Sink	7
Figure 18, Figure 19	5, 12	Figure 12	200	BGA Heat Sink	4.5
Figure 18, Figure 19	5, 12	Figure 12	400	BGA Heat Sink	4

**HEAT SINK MANUFACTURER**
**PART NUMBER**
**WEBSITE**

Wakefield	LTN20069-T5	wakefield-vette.com
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**Table 4. Two-Phase Single Output (see Figure 24)**

	C <sub>IN</sub> (CERAMIC)			C <sub>OUT</sub> (CERAMIC)		
	VENDOR	PART NUMBER	VALUE	VENDOR	PART NUMBER	VALUE
BULK	Sun Electronics	25CE150AX	150μF, 25V	Panasonic	ETPF470M5H	470μF, 2.5V, 5mΩ
CERAMIC	Murata	GRM21BR61E106KA73L	10μF, 25V, 0805, X5R	Murata	GRM32ER60J227M	220μF, 4V, 1206, X5R
	Taiyo Yuden	TMK212BBJ106KG-T	10μF, 25V, 0805, X5R	Taiyo Yuden	AMK325ABJ227MM-T	220μF, 4V, 1210, X5R
	Murata	GRM31CR61E226KE15L	22μF, 25V, 1206, X5R			
	Taiyo Yuden	TMK316BBJ226ML-T	22μF, 25V, 1206, X5R			

**25% Load Step (0A to 12.5A), Ceramic Output Cap Only Solutions**

V <sub>IN</sub> (V)	V <sub>OUT</sub> (V)	C <sub>IN</sub> * BULK (μF)	C <sub>IN</sub> CERAMIC (μF)	C <sub>OUT</sub> BULK (μF)	C <sub>OUT</sub> CERAMIC (μF)	FEED-FORWARD CAPACITOR C <sub>FF</sub> (pF)	PK-PK DEVIATION V <sub>PK-PK</sub> (mV)	SETTLING TIME t <sub>SETTLE</sub> (μs)	LOAD STEP (A)	LOAD STEP SLEW RATE (A/μs)	R <sub>FB</sub> (kΩ)	FREQ (kHz)
12	1.0	150	22 × 2	None	220 × 8	470	47	30	12.5	10	90.9	500
12	1.2	150	22 × 2	None	220 × 8	470	49	30	12.5	10	60.4	500
12	1.5	150	22 × 2	None	220 × 8	470	50	30	12.5	10	40.2	600
12	1.8	150	22 × 2	None	220 × 8	470	53	30	12.5	10	30.2	600

**25% Load Step (0A to 12.5A), Bulk plus Ceramic Output Cap Solutions**

12	1.0	150	22 × 2	470 × 2	220 × 3	None	58	20	12.5	10	90.9	500
12	1.2	150	22 × 2	470 × 2	220 × 3	None	58	20	12.5	10	60.4	500
12	1.5	150	22 × 2	470 × 2	220 × 3	None	61	30	12.5	10	40.2	600
12	1.8	150	22 × 2	470 × 2	220 × 3	None	64	50	12.5	10A	30.2	600

## APPLICATIONS INFORMATION

### Layout Checklist/Example

The high integration of LTM4650 makes the PCB board layout very simple and easy. However, to optimize its electrical and thermal performance, some layout considerations are still necessary.

- Use large PCB copper areas for high current paths, including  $V_{IN}$ , GND,  $V_{OUT1}$  and  $V_{OUT2}$ . It helps to minimize the PCB conduction loss and thermal stress.
- Place high frequency ceramic input and output capacitors next to the  $V_{IN}$ , PGND and  $V_{OUT}$  pins to minimize high frequency noise.
- Place a dedicated power ground layer underneath the unit.
- To minimize the via conduction loss and reduce module thermal stress, use multiple vias for interconnection between top layer and other power layers.
- Do not put via directly on the pad, unless they are capped or plated over.
- Use a separated SGND ground copper area for components connected to signal pins. Connect the SGND to GND underneath the unit.
- For parallel modules, tie the  $V_{OUT}$ ,  $V_{FB}$ , and COMP pins together. Use an internal layer to closely connect these pins together. The TRACK pin can be tied a common capacitor for regulator soft-start.
- Bring out test points on the signal pins for monitoring.

Figure 21 gives a good example of the recommended layout. LGA and BGA PCB layouts are identical with the exception of circle pads for BGA (see Package Description).

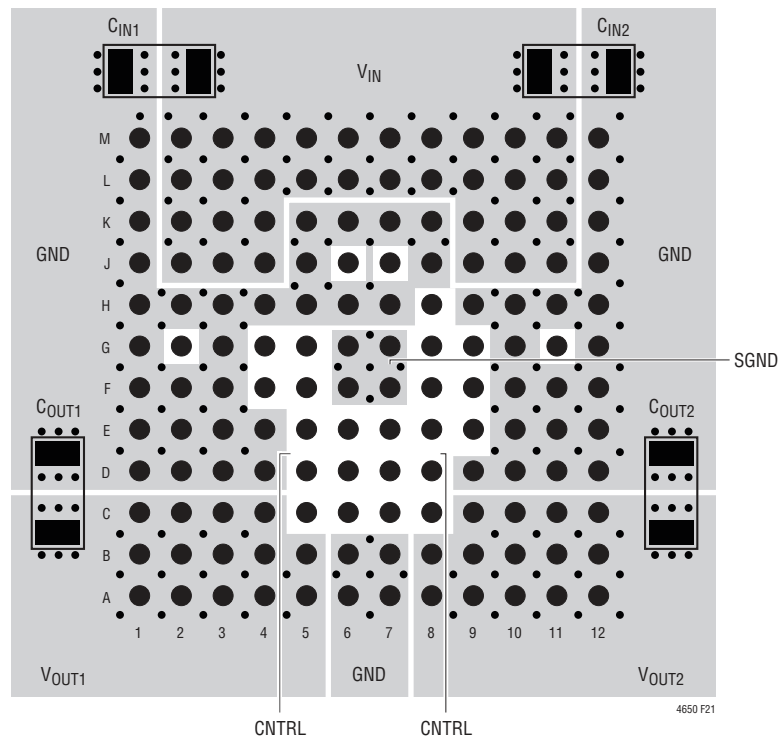
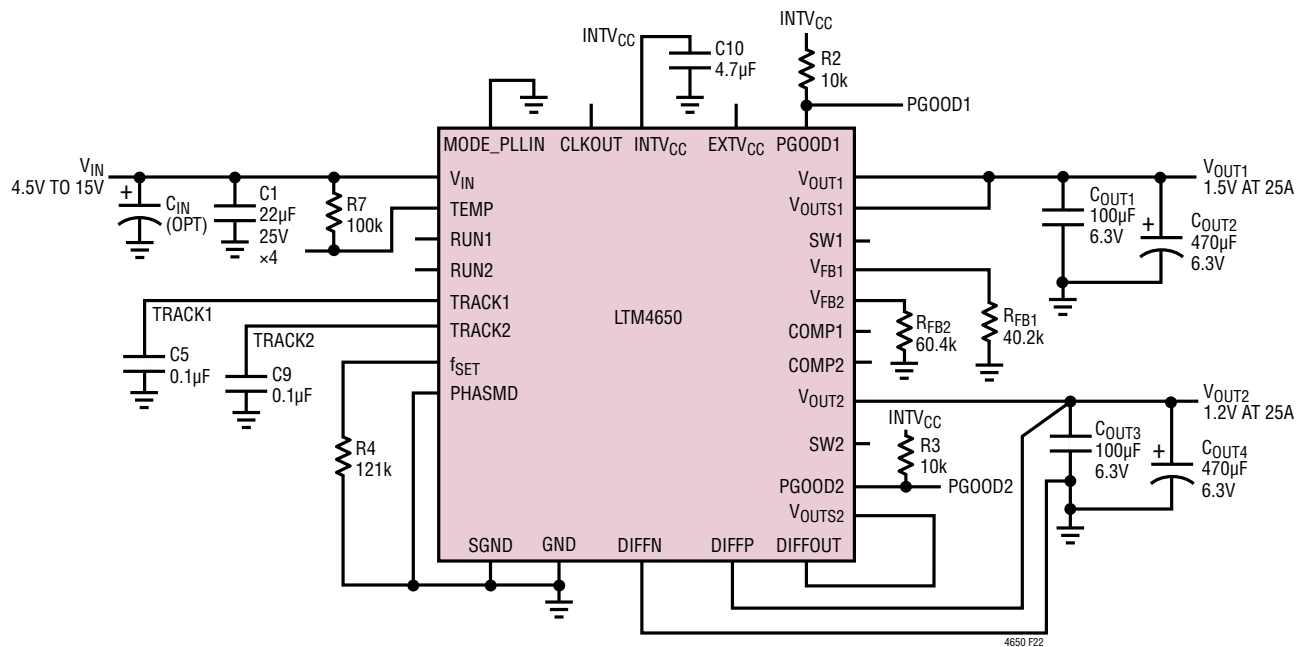


Figure 21. Recommended PCB Layout

## TYPICAL APPLICATION

Figure 22. Typical  $4.5V_{IN}$  to  $15V_{IN}$ , 1.5V and 1.2V at 25A Outputs

## TYPICAL APPLICATIONS

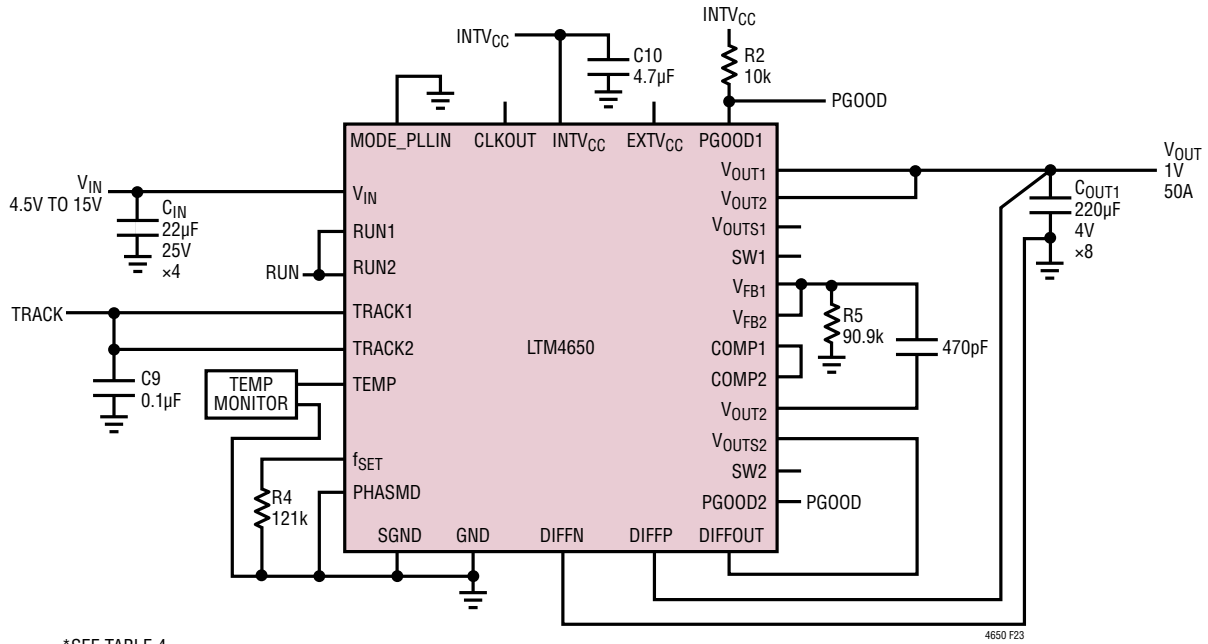


Figure 23. LTM4650 2-Phase, 1V at 50A Design

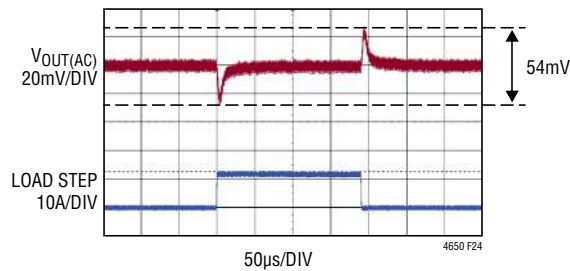


Figure 24. 25%, 12.5A Load Step Transient Waveform Of Figure 23 Circuit

TYPICAL APPLICATION

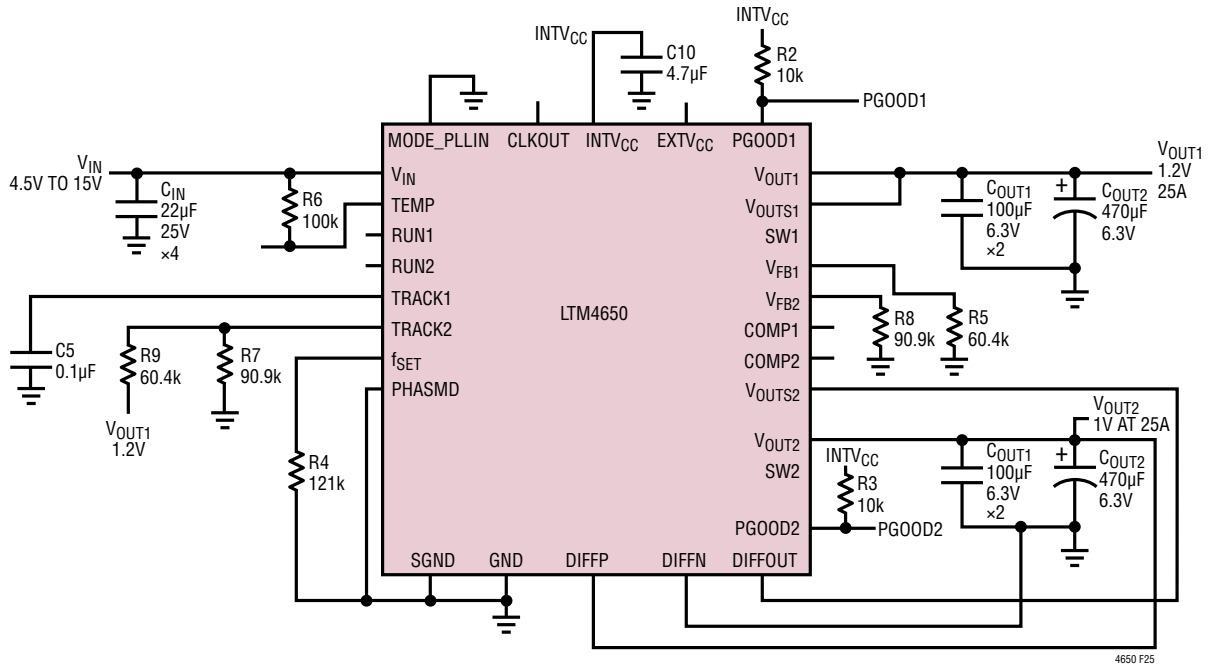


Figure 25. LTM4650 1.2V and 1V Output Tracking



## TYPICAL APPLICATION

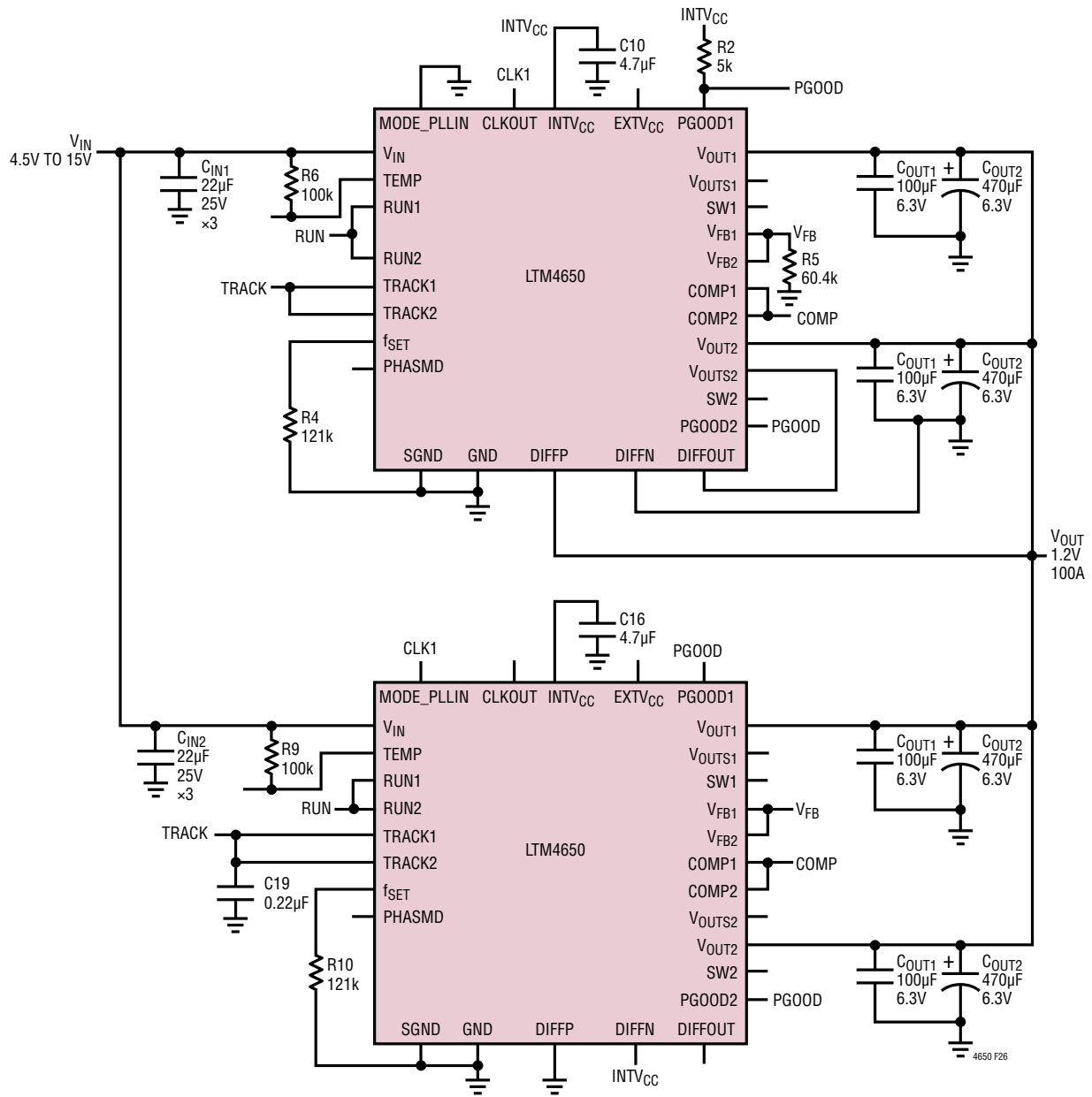


Figure 26. LTM4650 4-Phase, 1.2V at 100A

## PACKAGE DESCRIPTION

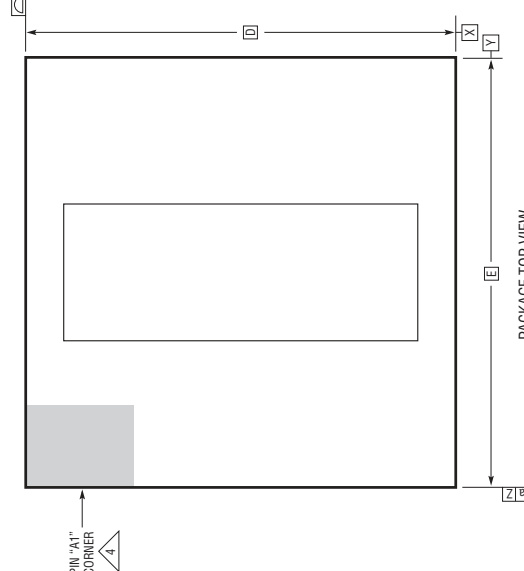
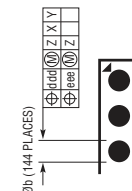
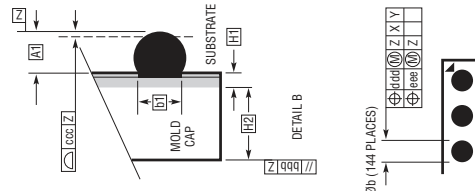
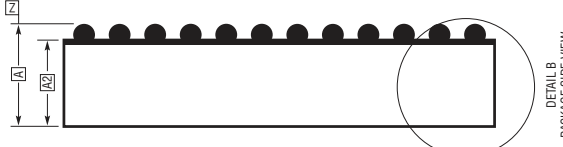
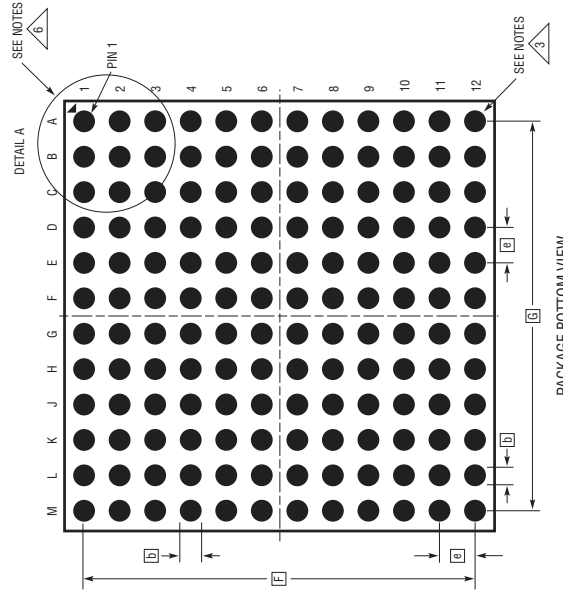
Table 5. LTM4650 Component BGA Pinout

PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION
A1	V <sub>OUT1</sub>	B1	V <sub>OUT1</sub>	C1	V <sub>OUT1</sub>	D1	GND	E1	GND	F1	GND
A2	V <sub>OUT1</sub>	B2	V <sub>OUT1</sub>	C2	V <sub>OUT1</sub>	D2	GND	E2	GND	F2	GND
A3	V <sub>OUT1</sub>	B3	V <sub>OUT1</sub>	C3	V <sub>OUT1</sub>	D3	GND	E3	GND	F3	GND
A4	V <sub>OUT1</sub>	B4	V <sub>OUT1</sub>	C4	V <sub>OUT1</sub>	D4	GND	E4	GND	F4	MODE_PLLIN
A5	V <sub>OUT1</sub>	B5	V <sub>OUT1</sub>	C5	V <sub>OUT1</sub>	D5	V <sub>FB1</sub>	E5	TRACK1	F5	RUN1
A6	GND	B6	GND	C6	f <sub>SET</sub>	D6	SGND	E6	COMP1	F6	SGND
A7	GND	B7	GND	C7	SGND	D7	V <sub>FB2</sub>	E7	COMP2	F7	SGND
A8	V <sub>OUT2</sub>	B8	V <sub>OUT2</sub>	C8	V <sub>OUT2</sub>	D8	TRACK2	E8	DIFFP	F8	DIFFOUT
A9	V <sub>OUT2</sub>	B9	V <sub>OUT2</sub>	C9	V <sub>OUT2</sub>	D9	GND	E9	DIFFN	F9	RUN2
A10	V <sub>OUT2</sub>	B10	V <sub>OUT2</sub>	C10	V <sub>OUT2</sub>	D10	GND	E10	GND	F10	GND
A11	V <sub>OUT2</sub>	B11	V <sub>OUT2</sub>	C11	V <sub>OUT2</sub>	D11	GND	E11	GND	F11	GND
A12	V <sub>OUT2</sub>	B12	V <sub>OUT2</sub>	C12	V <sub>OUT2</sub>	D12	GND	E12	GND	F12	GND

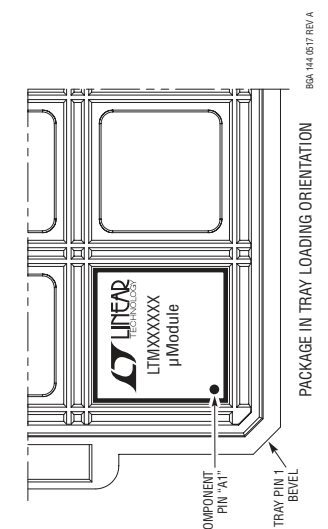
PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION
G1	GND	H1	GND	J1	GND	K1	GND	L1	GND	M1	GND
G2	SW1	H2	GND	J2	V <sub>IN</sub>	K2	V <sub>IN</sub>	L2	V <sub>IN</sub>	M2	V <sub>IN</sub>
G3	GND	H3	GND	J3	V <sub>IN</sub>	K3	V <sub>IN</sub>	L3	V <sub>IN</sub>	M3	V <sub>IN</sub>
G4	PHASMD	H4	GND	J4	V <sub>IN</sub>	K4	V <sub>IN</sub>	L4	V <sub>IN</sub>	M4	V <sub>IN</sub>
G5	CLKOUT	H5	GND	J5	GND	K5	GND	L5	V <sub>IN</sub>	M5	V <sub>IN</sub>
G6	SGND	H6	GND	J6	TEMP	K6	GND	L6	V <sub>IN</sub>	M6	V <sub>IN</sub>
G7	SGND	H7	GND	J7	EXTV <sub>CC</sub>	K7	GND	L7	V <sub>IN</sub>	M7	V <sub>IN</sub>
G8	PGOOD2	H8	INTV <sub>CC</sub>	J8	GND	K8	GND	L8	V <sub>IN</sub>	M8	V <sub>IN</sub>
G9	PGOOD1	H9	GND	J9	V <sub>IN</sub>	K9	V <sub>IN</sub>	L9	V <sub>IN</sub>	M9	V <sub>IN</sub>
G10	GND	H10	GND	J10	V <sub>IN</sub>	K10	V <sub>IN</sub>	L10	V <sub>IN</sub>	M10	V <sub>IN</sub>
G11	SW2	H11	GND	J11	V <sub>IN</sub>	K11	V <sub>IN</sub>	L11	V <sub>IN</sub>	M11	V <sub>IN</sub>
G12	GND	H12	GND	J12	GND	K12	GND	L12	GND	M12	GND

# PACKAGE DESCRIPTION

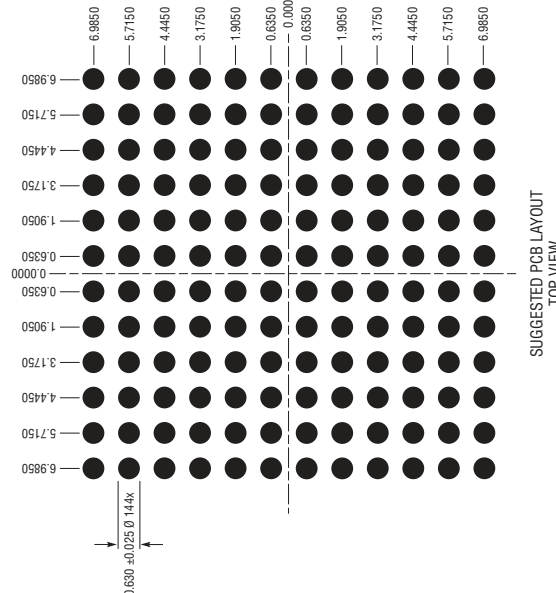
**BGA Package**  
**144-Lead (16mm × 16mm × 5.01mm)**  
 (Reference LTC DWG # 05-08-1523 Rev A)



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
  2. ALL DIMENSIONS ARE IN MILLIMETERS
  3. BALL DESIGNATION PER JEDEC MS-028 AND JEP95
  4. DETAILS OF PIN #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE PIN #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE
  5. PRIMARY DATUM - Z - IS SEATING PLANE
  6. PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG  $\mu$ Module PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY



SYMBOL	DIMENSIONS		NOTES
	MIN	MAX	
A	4.81	5.21	BALL HT
A1	0.50	0.70	BALL HT
A2	4.31	4.51	
b	0.60	0.90	BALL DIMENSION
b1	0.60	0.66	PAD DIMENSION
D	16.00		
E	16.00		
e	1.27		
F	13.97		
G	13.97		
H1	0.36	0.46	SUBSTRATE THK
H2	3.95	4.05	MOLD CAP HT
aaa		0.15	
bbb		0.10	
ccc		0.20	
ddd		0.30	
eee		0.15	
			TOTAL NUMBER OF BALLS: 144

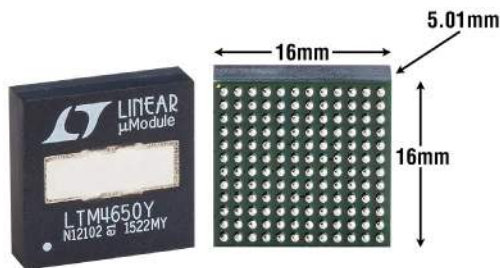


## REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	05/16	Updated package drawing.	32
B	12/16	Changed $V_{OUT}$ specs and condition from $V_{OUT} = 1.5V$ to 1.2V. Added Note 7.	3 3, 5
C	08/18	Added MP-Grade.	2, 5
D	11/22	Changed master to main and slave to subordinate and fixed major formatting issues. Swapped G10 and G11 titles. Changed pin ID to PHASMD. Added ink marking statement to package photos.	All 7 10, 31 34

# LTM4650

## PACKAGE PHOTOS Part marking is either ink mark or laser mark



## DESIGN RESOURCES

SUBJECT	DESCRIPTION
<a href="#">μModule Design and Manufacturing Resources</a>	<p>Design:</p> <ul style="list-style-type: none"> <li>• Selector Guides</li> <li>• Demo Boards and Gerber Files</li> <li>• Free Simulation Tools</li> </ul> <p>Manufacturing:</p> <ul style="list-style-type: none"> <li>• Quick Start Guide</li> <li>• PCB Design, Assembly and Manufacturing Guidelines</li> <li>• Package and Board Level Reliability</li> </ul>
<a href="#">μModule Regulator Products Search</a>	<ol style="list-style-type: none"> <li>1. Sort table of products by parameters and download the result as a spread sheet.</li> <li>2. Search using the Quick Power Search parametric table.</li> </ol>
<a href="#">Digital Power System Management</a>	<p>Analog Devices' family of digital power supply management ICs are highly integrated solutions that offer essential functions, including power supply monitoring, supervision, margining and sequencing, and feature EEPROM for storing user configurations and fault logging.</p>

## RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
<a href="#">LTM4630</a>	Lower Current than LTM4650, Dual 18A or Single 36A	Pin Compatible with LTM4650; $4.5V \leq V_{IN} \leq 15V$ , $0.6V \leq V_{OUT} \leq 1.8V$ , 15mm × 15mm × 4.41mm LGA and 15mm × 15mm × 5.01mm BGA Packages
<a href="#">LTM4630A</a>	Lower Current and Higher $V_{OUT}$ than LTM4650, Up to 5.3V <sub>OUT</sub> , Dual 18A or Single 26A	Pin Compatible with LTM4650; $4.5V \leq V_{IN} \leq 15V$ , $0.6V \leq V_{OUT} \leq 5.3V$ , 15mm × 15mm × 4.41mm LGA Package
<a href="#">LTM4630-1</a>	Lower Current than LTM4650 with External Compensation and ±0.8% (LTM4630-1A) or ±1.5% (LTM4630-1B) $V_{OUT}$ Accuracy	Pin Compatible with LTM4650; $4.5V \leq V_{IN} \leq 15V$ , $0.6V \leq V_{OUT} \leq 1.8V$ , 15mm × 15mm × 5.01mm BGA Package
<a href="#">LTM4620</a>	Lower Current than LTM4650, Dual 13A or Single 26A	Pin Compatible with LTM4650; $4.5V \leq V_{IN} \leq 16V$ , $0.6V \leq V_{OUT} \leq 5.3V$ , 15mm 15mm × 4.41mm LGA and 15mm × 15mm × 5.01mm BGA Packages
<a href="#">LTM4620A</a>	Lower Current and Higher $V_{OUT}$ than LTM4650, Up to 5.3V <sub>OUT</sub> , Dual 13A or Single 26A.	Pin Compatible with LTM4650; $4.5V \leq V_{IN} \leq 16V$ , $0.6V \leq V_{OUT} \leq 5.3V$ , 15mm 15mm × 4.41mm LGA and 15mm × 15mm × 5.01mm BGA Packages
<a href="#">LTM4628</a>	Lower Current, Higher $V_{IN}$ and $V_{OUT}$ than LTM4650, Dual 8A or Single 16A	Pin Compatible with LTM4650; $4.5V \leq V_{IN} \leq 26.5V$ , $0.6V \leq V_{OUT} \leq 5.5V$ , 15mm 15mm × 4.32mm LGA and 15mm × 15mm × 4.92mm BGA Packages
<a href="#">LTM4677</a>	Dual 18A or Single 36A with PSM	$4.5V \leq V_{IN} \leq 16V$ , $0.5V \leq V_{OUT} \leq 1.8V$ . 16mm × 16mm × 5.01mm BGA Package
<a href="#">LTM4644</a>	Quad 4A	$4V \leq V_{IN} \leq 14V$ , $0.6V \leq V_{OUT} \leq 5.5V$ . 9mm × 15mm × 5.01mm BGA Package
<a href="#">LTM4639</a>	Lower $V_{IN}$ (2.375V ≤ $V_{IN}$ ≤ 7V), 20A	$0.6V \leq V_{OUT} \leq 5.5V$ . 15mm × 15mm × 4.92mm BGA Package

Rev. D