

# THC63LVD1027

Dual Link LVDS Repeater

#### General Description

The THC63LVD1027 LVDS(Low Voltage Differential Signaling) repeater is designed to support pixel data transmission between Host and Flat Panel Display up to WUXGA resolution.

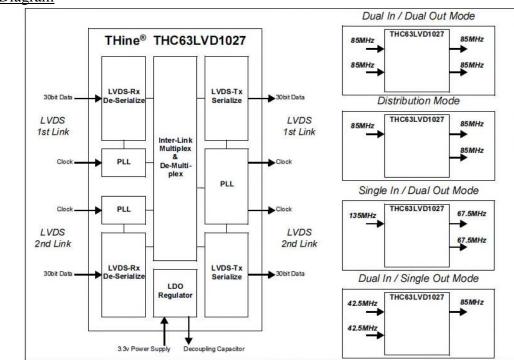
THC63LVD1027 receives the dual link LVDS data streams and transmits the LVDS data through various line rate conversion modes, Dual Link Input / Dual Link Output, Single Link Input / Dual Link Output, and Dual Link Input / Single Link Output.

#### **Features**

- 30bits/pixel dual link LVDS Receiver
- 30bits/pixel dual Link LVDS Transmitter
- Operating Temperature Range : -40°C~85°C
- Wide LVDS input skew margin: ± 480ps at 75MHz
- Accurate LVDS output timing: ± 250ps at 75MHz
- Reduced swing LVDS output mode supported to suppress the system EMI

• Various line rate conversion modes supported Dual link input / Dual link output [clkout=1x clkin] Single link input / Dual link output [clkout=1/2x clkin] Dual link input / Single link output [clkout=2x clkin]

- Distribution (signal duplication) mode supported
- Power down mode supported
- 3.3V single voltage power supply
- No external components required for PLLs
- 64pin TSSOP with Exposed PAD (0.5mm lead pitch)





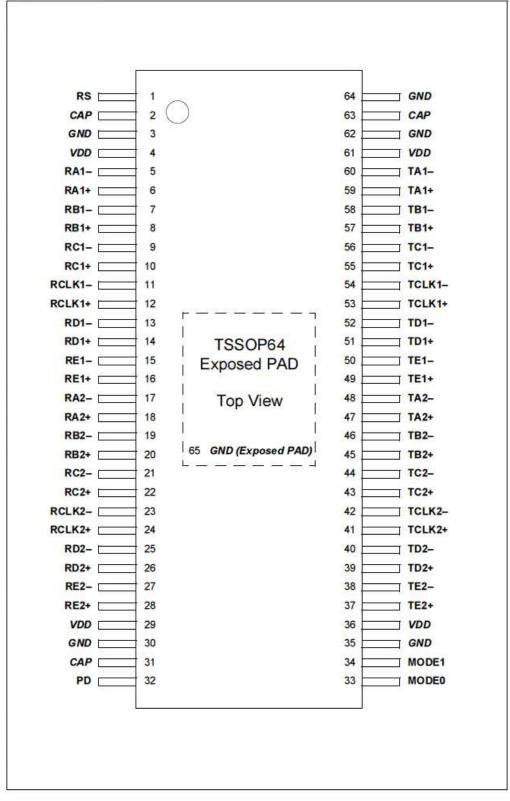
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# Block Diagram



#### Pin Diagram







### Pin Description

### Table 1. Pin Description

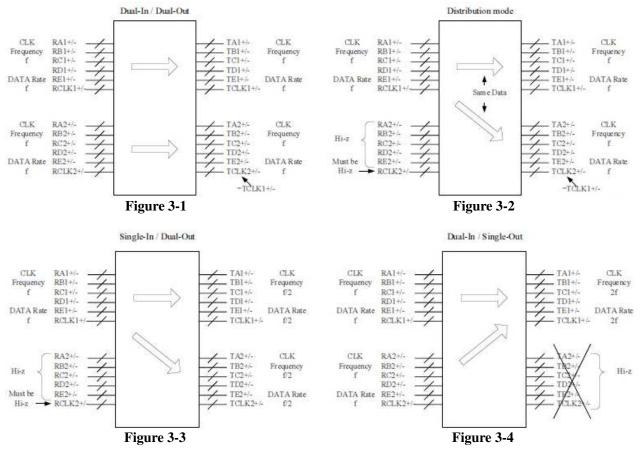
Pin Name	Direction	Туре		•	Description	0 <b>n</b>			
RA1+/-			LVDS data in	LVDS data input for channel A of 1st Link					
RB1+/-			LVDS data in						
RC1+/-									
RD1+/-			LVDS data input for channel C of 1st Link LVDS data input for channel D of 1st Link						
RE1+/-			LVDS data in						
RCLK1+/-				-					
RA2+/-	<b>.</b> .		LVDS clock input for 1st Link LVDS data input for channel A of 2nd Link						
RB2+/-	Input		LVDS data in						
				-					
RC2+/-			LVDS data in	-					
RD2+/-			LVDS data in						
RE2+/-			LVDS data in						
RCLK2+/-			LVDS clock i	input fo	or 2nd Link				
		LVDS	(See "Mode select			de,RCLK2+/- must be Hi-Z.			
TA1+/-			LVDS data or						
TB1+/-			LVDS data of						
TC1+/-			LVDS data of						
TD1+/-			LVDS data of						
TE1+/-									
TCLK1+/-				LVDS data output for channel E of 1st Link LVDS clock output for 1st Link					
	Output								
TA2+/-	-					A of 2nd Link			
TB2+/-						B of 2nd Link			
TC2+/-						C of 2nd Link			
TD2+/-						D of 2nd Link			
TE2+/-						E of 2nd Link			
TCLK2+/-			LVDS clock o		for 2nd Lin	ık			
PD			Power Down						
			H: Normal operat L: Power down st		VDS output sig	male turn to Hi Z			
RS			LVDS output						
<b>N</b> O			H: Normal swing		iever sereet				
			L: Reduced swin						
MODE1	Input	LV-TTL	Mode selection						
MODE0	mpar	2,112		IODE0	RCLK2+/-	Description			
			L L	L L	Clkin Hi-Z	Dual-in/Dual-out mode Distribution mode			
			H	L	Hi-Z Hi-Z	Single-in/Dual-out mode			
			L	H	Clkin	Dual-in/Single-out mode			
			Н	Н	-	Reserved			
			In Distribution and	d Single-i	n/Dual-out mod	de, RCLK2+/- must be Hi-Z.			
VDD	]		3.3V power st	upply	pins				
GND	Power	-	Ground pins	(Expos	sed PAD is	also Ground)			
САР			Decoupling ca						
						decoupling capacitors(Ccap).			
			Recommended Ccap is 0.1µF.						



### Mode Setting

Table 2. Mode Setting								
Input/Output	RCLK2+/-	MODE1	MODE0					
		(Input mode)	(Output mode)					
		H: Single	H: Single					
		L: Dual	L: Dual					
Dual-In/Dual-Out	CLK in	L	L					
(Fig.3-1,14-1)								
Distribution	Hi-Z	L	L					
(Fig.3-2,14-2)								
Single-In/Dual-Out	Hi-Z	Н	L					
(Fig.3-3,14-3)								
Dual-In/Single-Out	CLK in	L	Н					
(Fig.3-4,14-4)								
Reserved	-	Н	Н					

### Signal Flow for Each Setting





#### Output Control / Fail Safe

THC63LVD1027 has a function to control output depending on LVDS input condition.

PD	RCLK1+/-	RCLK2+/-	Output
L	*	*	All Hi-Z
Н	Hi-Z	*	All Hi-Z
Н	CLK in	CLK in	Refer to p.4 Mode Setting #
Н	CLK in	Hi-Z	Refer to p.4 Mode Setting #

#### **Table 3. Output Control**

\*: Don't care

#: If a particular input data pair is Hi-Z, the corresponding output data become L according to LVDS DC spec.

For fail-safe purpose, all LVDS input pins are connected to VDD via resistance for detecting Hi-Z state.

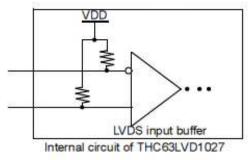


Figure 4. Fail Safe Circuit



### Absolute Maximum Ratings

Table 4.	Absolute	Maximum	Rating
I able h	insolute	1710/MIIIGIII	INCOMPANY

Parameter	Min	Max	Unit
Power Supply Voltage	-0.3	+4.0	V
LVCMOS Input Voltage	-0.3	V <sub>DD</sub> +0.3	V
LVDS Input Voltage	-0.3	V <sub>DD</sub> +0.3	V
Junction Temperature	-	125	°C
Storage Temperature	-55	125	°C
Reflow Peak Temperature / Time	-	260 / 10sec	°C
Maximum Power Dissipation @+25°C	-	2.5	W

### **Operating Conditions**

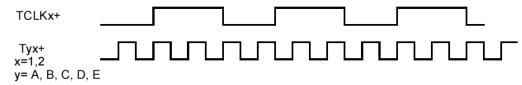
#### **Table 5. Operating Condition**

Symbol	Paramete	Min	Тур	Max	Unit	
Та	Operating Ambient 7	Cemperature	-40	25	+85	°C
V <sub>DD</sub>	Power Supply Voltag	ge	3.0	3.3	3.6	V
	Dual-In/Dual-Out	Input	20	-	85	MHz
	Duai-III/Duai-Out	Output	20	-	85	MILL
	Distribution	Input	20	-	85	MHz
F <sub>clk</sub>	Distribution	Output	20	-	85	WITTZ
I' clk	Single-In/Dual-Out	Input	40	-	135	MHz
	Single-III/Dual-Out	Output	20	-	67.5	WITTZ
	Dual In/Single Out	Input	20	-	42.5	MHz
	Dual-In/Single-Out Output		40	-	85	IVITIZ

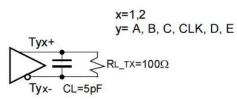


### Power Consumption

		Tab	le 6. Power Cons	sumption				
Symbol	Parameter		Conditions		Min	Тур.	Max	Unit
			CLKIN=40MHz		-	-	265	
		Dual-In/Dual-Out	CLKIN=65MHz		-	-	305	
		Duai-III/Duai-Out	CLKIN=75MHz		-	-	325	mA
			CLKIN=85MHz		-	-	340	
			CLKIN=40MHz		-	-	215	
		Distribution	CLKIN=65MHz		-	-	235	
		Distribution	CLKIN=75MHz	$R_{L_Tx}=100\Omega$	-	-	245	mA
	Operating Current		CLKIN=85MHz		-	-	260	
т	(Worst Case Pattern)		CLKIN=40MHz	CL=5pF	-	-	175	
ICCW			CLKIN=65MHz	RS=VDD Fig 6.	-	-	190	mA
	Fig 5.		CLKIN=75MHz		-	-	200	
		Single-In/Dual-Out	CLKIN=85MHz		-	-	210	
			CLKIN=112MHz		-	-	230	
			CLKIN=135MHz		-	-	250	
			CLKIN=20MHz		-	-	215	
		Dual In/Single Out	CLKIN=32.5MHz		-	-	235	mA
		Dual-In/Single-Out	CLKIN=37.5MHz		-	-	245	
			CLKIN=42.5MHz		-	-	260	
I <sub>CCS</sub>	Power Down Current	-	-	-	-	-	8	mA







LVDS Output Load

Figure 6. LVDS Output Load



### **Electrical Characteristics**

# **DC Specifications**

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
VCAP	Capacitor pin appearance voltage	C <sub>CAP</sub> =0.1µF	-	1.8	-	V
VIL	LV-TTL Input Low Voltage	-	GND	-	0.8	V
VIH	LV-TTL Input High Voltage	-	2.0	-	VDD	V
I <sub>IN_TTL</sub>	LV-TTL Input Leakage Current	-	-4	-	+4	μΑ

# Table 7. DC Specifications

### LVDS Receiver DC Specifications

#### Table 8. LVDS Receiver DC Specifications

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V <sub>IN_RX</sub>	LVDS-Rx Input Voltage Range	-	0.3	-	2.1	
VIC_RX	LVDS-Rx Common Voltage	-	0.6	1.2	1.8	V
V <sub>TH_RX</sub>	LVDS-Rx Differential High Threshold		-	-	+100	
V <sub>TL_RX</sub>	LVDS-Rx Differential Low Threshold	$V_{IC_{RX}} = 1.2V$	-100	-	-	mV
Vid_rx	LVDS-Rx Differential Input Voltage	-	100	-	600	
		PD=VDD	-0.3	-	+0.3	mA
I <sub>IN_RX</sub>	LVDS-Rx Input Leakage Current	PD=GND Vin=GND or VDD	-10	-	+10	μΑ

### LVDS Transmitter DC Specifications

### Table 9. LVDS Transmitter DC Specifications

Symbol	Parameter	Conditions		Min	Тур	Max	Unit				
V <sub>OC_TX</sub>	LVDS-Tx Common Voltage		-	1.125	1.25	1.375	V				
ΔVoc_tx	Change in VOC between complementary output states	D	D	D	D		-	-	-	35	mV
	LVDS-Tx Differential	$R_{L_TX} =$	Normal Swing	250	350	450	mV				
Vod_tx	Output Threshold	100Ω	Reduced Swing	100	200	300	тv				
$\Delta V_{OD_TX}$	Change in VOD between complementary output states		-	-	-	35	mV				
Ios_tx	LVDS-Tx Output Short Current	V <sub>DD</sub> =3.3V	Vout=GND	-24	-	-	mA				
I <sub>OZ_TX</sub>	LVDS-Tx Output Tri-state Current	PD=GND	Vout=GND to VDD	-10	-	+10	μΑ				



### **AC Specifications**

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
t <sub>LT</sub>	Phase Lock Loop Set Time (Fig 7.)	-	-	-	-	10	ms
		Dual-In/Dual-Out	CLKIN=75MHz	9t <sub>RCP</sub> +3	9t <sub>RCP</sub> +5	$9t_{RCP}$ +7	
	Data Latency (Fig 8.)	Distribution	CLKIN=75MHz	9t <sub>RCP</sub> +3	9t <sub>RCP</sub> +5	9t <sub>RCP</sub> +7	
tdl		Single-In/Dual-Out	CLKIN=75MHz	(11+2/7)t <sub>RCP</sub> +3	(11+2/7)t <sub>RCP</sub> +5	(11+2/7)t <sub>RCP</sub> +7	ns
		Dual-In/Single-Out	CLKIN=37.5MHz	(8+5/14)t <sub>RCP</sub> +3	(8+5/14)t <sub>RCP</sub> +5	(8+5/14)t <sub>RCP</sub> +7	
<b>t</b> deh	DE Input High Time (Fig 9.)		-	2t <sub>RCP</sub>	-	-	
t <sub>DEL</sub>	DE Input Low Time (Fig 9.)	Single-In/Dual-Out	-	2trcp	-	-	ns
tdeint	DE Input Period (Fig 9.)		-	4t <sub>RCP</sub>	Must be 2n t <sub>RCP</sub> (n=integer)	-	

#### Table 10. AC Specifications

# AC Timing Diagrams

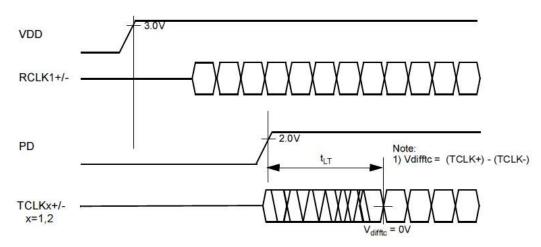


Figure 7.	Phase	Lock	Loop	Set	Time
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### AC Timing Diagrams (Continued)

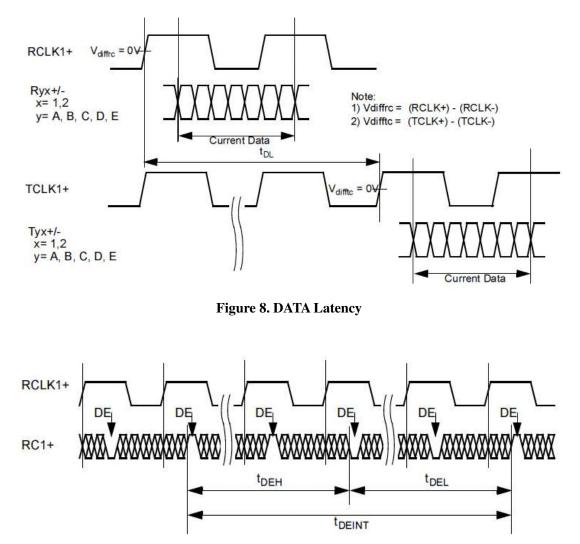


Figure 9. Single Link Input / Dual Link Output Mode RC1(DE) Input Timing



# LVDS Receiver AC Specifications

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
t <sub>RCP</sub>	LVDS Clock Period	-	7.4	-	50	
trch	LVDS Clock High Duration	-	2/7t <sub>RCP</sub>	4/7t <sub>RCP</sub>	5/7t <sub>RCP</sub>	ns
t <sub>RCL</sub>	LVDS Clock Low Duration	-	2/7t <sub>RCP</sub>	3/7t <sub>RCP</sub>	5/7t <sub>RCP</sub>	
		CLKIN=75MHz <sup>(1)</sup>	480	-	-	
trsup	LVDS Data Input Setup Margin	CLKIN=112MHz <sup>(1)</sup>	250	-	-	ps
		CLKIN=135MHz <sup>(1)</sup>	220	-	-	
		CLKIN=75MHz <sup>(1)</sup>	480	-	-	
trhld	LVDS Data Input Hold Margin	CLKIN=112MHz <sup>(1)</sup>	250	-	-	ps
		CLKIN=135MHz <sup>(1)</sup>	220	-	-	
t <sub>RIP6</sub>	LVDS Data Input Position 6	-	2/7trcp-trhld	2/7t <sub>RCP</sub>	2/7trcp+trsup	
t <sub>RIP5</sub>	LVDS Data Input Position 5	-	3/7t <sub>RCP</sub> -t <sub>RHLD</sub>	3/7t <sub>RCP</sub>	3/7trcp+trsup	
t <sub>RIP4</sub>	LVDS Data Input Position 4	-	4/7t <sub>RCP</sub> -t <sub>RHLD</sub>	4/7t <sub>RCP</sub>	4/7t <sub>RCP</sub> +t <sub>RSUP</sub>	
t <sub>RIP3</sub>	LVDS Data Input Position 3	-	5/7t <sub>RCP</sub> -t <sub>RHLD</sub>	5/7t <sub>RCP</sub>	5/7trcp+trsup	ps
t <sub>RIP2</sub>	LVDS Data Input Position 2	-	6/7trcp-trhld	6/7t <sub>RCP</sub>	6/7trcp+trsup	
t <sub>RIP1</sub>	LVDS Data Input Position 1	-	7/7t <sub>RCP</sub> -t <sub>RHLD</sub>	7/7t <sub>RCP</sub>	7/7trcp+trsup	
t <sub>RIP0</sub>	LVDS Data Input Position 0	-	8/7t <sub>RCP</sub> -t <sub>RHLD</sub>	8/7t <sub>RCP</sub>	8/7t <sub>RCP</sub> +t <sub>RSUP</sub>	
t <sub>CK12</sub>	Skew Time Between RCLK1 and RCLK2	-	-0.3 t <sub>RCP</sub>	-	+0.3 trcp	ps

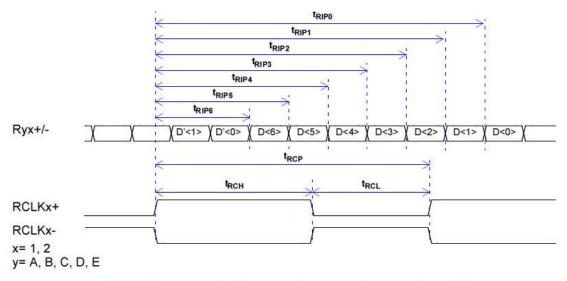
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### Table 11. LVDS Receiver AC Specifications

(1) V<sub>IC\_RX</sub>=1.2V, t<sub>RCH</sub>=4/7 t<sub>RCP</sub>



### LVDS Receiver Input Timing



Ry1+/- skew margin is the one between RCLK1+/- and Ry1+/-. Ry2+/- skew margin is the one between RCLK2+/- and Ry2+/-.

Figure 10. LVDS Receiver Timing

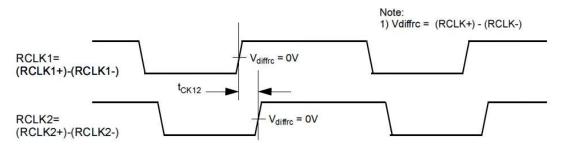


Figure 11. Skew time between RCLK1 and RCLK2



# LVDS Transmitter AC Specifications

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
t <sub>TCP</sub>	LVDS Clock Period	-	11.76	-	50	
t <sub>TCH</sub>	LVDS Clock High Duration	-	-	4/7t <sub>TCP</sub>	-	ns
t <sub>TCL</sub>	LVDS Clock Low Duration	-	-	3/7t <sub>TCP</sub>	-	
ttsup	LVDS Data Output Setup	CLKOUT=75MHz	-	-	250	ps
t <sub>THLD</sub>	LVDS Data Output Hold	CLKOUT=75MHz	-	-	250	ps
t <sub>TOP6</sub>	LVDS Data Output Position 6	-	2/7ttcp-tthld	2/7t <sub>TCP</sub>	2/7ttcp+ttsup	
t <sub>TOP5</sub>	LVDS Data Output Position 5	-	3/7t <sub>TCP</sub> -t <sub>THLD</sub>	3/7t <sub>TCP</sub>	3/7t <sub>TCP</sub> +t <sub>TSUP</sub>	
ttop4	LVDS Data Output Position 4	-	4/7t <sub>TCP</sub> -t <sub>THLD</sub>	4/7t <sub>TCP</sub>	4/7ttcp+ttsup	
<b>t</b> торз	LVDS Data Output Position 3	-	5/7t <sub>TCP</sub> -t <sub>THLD</sub>	5/7t <sub>TCP</sub>	5/7t <sub>TCP</sub> +t <sub>TSUP</sub>	ps
t <sub>TOP2</sub>	LVDS Data Output Position 2	-	6/7t <sub>TCP</sub> -t <sub>THLD</sub>	6/7t <sub>TCP</sub>	6/7t <sub>TCP</sub> +t <sub>TSUP</sub>	
t <sub>TOP1</sub>	LVDS Data Output Position 1	-	7/7t <sub>TCP</sub> -t <sub>THLD</sub>	7/7t <sub>TCP</sub>	7/7t <sub>TCP</sub> +t <sub>TSUP</sub>	
t <sub>top0</sub>	LVDS Data Output Position 0	-	8/7t <sub>TCP</sub> -t <sub>THLD</sub>	8/7t <sub>TCP</sub>	8/7ttcp+ttsup	
t <sub>LVT</sub>	LVDS Transition Time (Fig 13.)	Fig.6	-	0.6	1.5	ns

### Table 12. LVDS Transmitter AC Specifications



### LVDS Transmitter Output Diagram

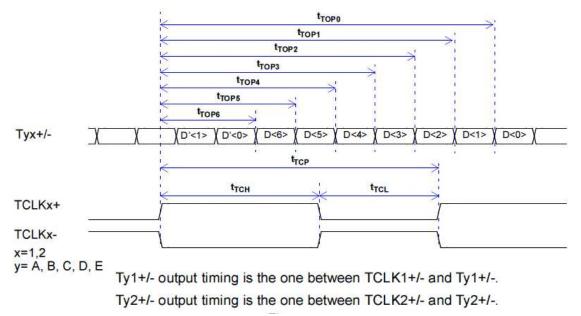


Figure 12. LVDS Transmitter Timing

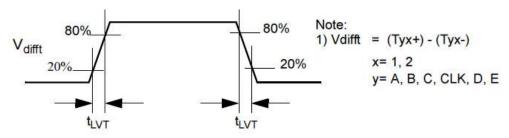


Figure 13. LVDS Transition Timing



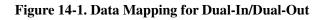
# LVDS Data Mapping

# Dual-In / Dual-Out

# LVDS-Rx Input Mapping

RCLK1+									1				/	
RA1+/-	G1 [4]	R1 [9]	R1 [8]	R1 [7]	R1 [6]	R1 [5]	R1 [4]	G3 [4]	R3 [9]	R3 [8]	R3 [7]	R3 [6]	R3 [5]	R3 [4]
RB1+/-	B1 [5]	B1 [4]	G1 [9]	G1 [8]	G1 [7]	G1 [6]	G1 [5]	B3 [5]	(B3 [4]	G3 [9]	G3 [8]	G3 [7]	G3 [6]	G3 [5]
RC1+/-	DE	VSYNC	HSYNC	B1 [9]	B1 [8]	B1 [7]	B1 [6]	DE	VSYNC	HSYNC	B3 [9]	B3 [8]	B3 [7]	B3 [6]
RD1+/-	data11	B1 [3]	B1 [2]	G1 [3]	G1 [2]	R1 [3]	R1 [2]	data11	B3 [3]	B3 [2]	G3 [3]	G3 [2]	R3 [3]	R3 [2]
RE1+/-	data12	B1 [1]	B1 [0]	G1 [1]	G1 [0]	R1 [1]	R1 [0]	data 12	B3 [1]	B3 [0]	G3 [1]	G3 [0]	R3 [1]	R3 [0]
RCLK2+						[								
RA2+/-	G2 [4]	R2 [9]	R2 [8]	R2 [7]	R2 [6]	R2 [5]	R2 [4]	G4 [4]	R4 [9]	R4 [8]	R4 [7]	R4 [6]	R4 [5]	R4 [4]
RB2+/-	B2 [5]	B2 [4]	G2 [9]	G2 [8]	G2 [7]	G2 [6]	R2 [5]	B4 [5]	B4 [4]	G4 [9]	G4 [8]	G4 [7]	G4 [6]	G4 [5]
RC2+/-	DE	VSYNC	HSYNC	B2 [9]	B2 [8]	B2 [7]	B2 [6]	DE	VSYNC	HSYNC	B4 [9]	B4 [8]	B4 [7]	B4 [6]
RD2+/-	data21	B2 [3]	B2 [2]	G2 [3]	G2 [2]	R2 [3]	R2 [2]	data21	B4 [3]	B4 [2]	G4 [3]	G4 [2]	R4 [3]	R4 [2]
ND2	A A			S. 124	_		R2 [0]	data22	B4 [1]	B4 [0]	G4 [1]	G4 [0]	R4 [1]	R4 [0]
RE2+/		<sup>в2</sup> [1] Марр	B2 [0]	G2 [1]	G2 [0]	R2 [1]	K2 [0]	()				04 [0]	V ise [1]	Vierfol
RE2+/			/	G2 [1]	G2 [0]	R2 [1]	K2 [0]	()				04 [0]	V IN LI	Vierfol
RE2+/	Dutput I	Марр	oing										[	n
RE2+/	Dutput I		/	(G2 [1])	G2 [0]	(R2 [1])		G3 [4]		R3 [8]	R3 [7]		(R3 [5]	X R3 [4]
RE2+/	Output   ( G1 [4] (	Марр	oing				R1 [4]						[	n
RE2+/	Dutput I (G1 [4]) (B1 [5])	Mapp R1 [9] B1 [4]	Coing R1 [8] G1 [9]	(R1[7])	R1 [6]	(R1 [5])	R1 [4]	G3 [4]	(R3 [9])	R3 [8]	R3 [7]	R3 [6]	(R3 [5]	(R3 [4]
RE2+/-	Output           (G1 [4])           (B1 [5])           (DE)	Mapp R1 [9] B1 [4]	Coing R1 [8] G1 [9]	(R1 [7]) (G1 [8])	R1 [6] G1 [7]	(R1 [5])	R1 [4] G1 [5]	G3 [4] B3 [5]	(R3 [9]) (B3 [4])	R3 [8] G3 [9]	R3 [7] G3 [8]	(R3 [6] (G3 [7]	( R3 [5] ( G3 [6]	X R3 [4] X G3 [5]
RE2+/- VDS-Tx ( TCLK1+ TA1+/- TB1+/- TC1+/-	Output           (G1 [4])           (B1 [5])           (DE)	Mapp R1 [9]) B1 [4]) VSYNC) B1 [3])	Cing R1 [8] G1 [9] HSYNC	(R1 [7]) (G1 [8]) (B1 [9])	R1 [6] G1 [7] B1 [8]	(R1 [5]) (G1 [6]) (B1 [7]) (R1 [3])	R1 [4] G1 [5] B1 [6] R1 [2]	(G3 [4]) (B3 [5]) (DE)	(R3 [9]) (B3 [4]) (VSYNC) (B3 [3])	R3 [8] G3 [9] HSYNC	R3 [7] G3 [8] B3 [9]	(R3 [6] (G3 [7] (B3 [8] (G3 [2]	(R3 [5] (G3 [6] (B3 [7] (R3 [3]	(R3 [4] G3 [5] (B3 [6]
RE2+/	Output           ) G1 [4] (           ) B1 [5] (           ) DE (           (data11) (	Mapp R1 [9]) B1 [4]) VSYNC) B1 [3])	R1 [8] G1 [9] HSYNC B1 [2]	(R1 [7]) (G1 [8]) (B1 [9]) (G1 [3])	R1 [6] G1 [7] B1 [8] G1 [2]	(R1 [5]) (G1 [6]) (B1 [7]) (R1 [3])	R1 [4] G1 [5] B1 [6] R1 [2]	(G3 [4]) (B3 [5]) (DE) (data 11)	(R3 [9]) (B3 [4]) (VSYNC) (B3 [3])	R3 [8] G3 [9] HSYNC B3 [2]	R3 [7] G3 [8] B3 [9] G3 [3]	(R3 [6] (G3 [7] (B3 [8] (G3 [2]	(R3 [5] (G3 [6] (B3 [7] (R3 [3]	X R3 [4] X G3 [5] X B3 [6] X R3 [2]
RE2+/	Output           ) G1 [4] (           ) B1 [5] (           ) DE (           (data11) (	Mapp R1 [9]) B1 [4]) VSYNC) B1 [3]) B1 [1])	R1 [8] G1 [9] HSYNC B1 [2]	(R1 [7]) (G1 [0]) (B1 [9]) (G1 [3]) (G1 [1])	R1 [6] G1 [7] B1 [8] G1 [2]	(R1 [5]) (G1 [6]) (B1 [7]) (R1 [3]) (R1 [1])	R1 [4] G1 [5] B1 [6] R1 [2]	(G3 [4]) (B3 [5]) (DE) (data 11)	(R3 [9]) (B3 [4]) (VSYNC) (B3 [3]) (B3 [1])	R3 [8] G3 [9] HSYNC B3 [2]	R3 [7] G3 [8] B3 [9] G3 [3]	(R3 [6] (G3 [7] (B3 [8] (G3 [2] (G3 [0])	(R3 [5] (G3 [6] (B3 [7] (R3 [3]	X R3 [4] X G3 [5] X B3 [6] X R3 [2]
RE2+/-	Output         (G1 [4])         (B1 [5])         (DE)         (data11)         (data12)         (G2 [4])	Mapp R1 [9]) B1 [4]) VSYNC) B1 [3]) B1 [1])	Ding R1 [8] G1 [9] HSYNC B1 [2] B1 [0]	(R1 [7]) (G1 [0]) (B1 [9]) (G1 [3]) (G1 [1])	R1 [6] G1 [7] B1 [8] G1 [2] G1 [0]	(R1 [5]) (G1 [6]) (B1 [7]) (R1 [3]) (R1 [1])	R1 [4] G1 [5] B1 [6] R1 [2] R1 [0] R2 [4]	(G3 [4]) (B3 [5]) (DE) (data 11) (data 12)	(R3 [9]) (B3 [4]) (VSYNC) (B3 [3]) (B3 [1])	R3 [8] G 3 [9] HSYNC B3 [2] B3 [0]	R3 [7] G3 [8] B3 [9] G3 [3] G3 [1]	R3 [6] G3 [7] B3 [8] G3 [2] G3 [0] R4 [6]	(R3 [5] (G3 [6] (B3 [7] (R3 [3] (R3 [1] (R4 [5]	X R3 [4] X G3 [5] X B3 [6] X R3 [2] X R3 [0]
RE2+/	Output         ) G1 [4] (         ) B1 [5] (         ) DE (1)         ) data11 (         ) data12 (         ) G2 [4] (         ) B2 [5] (	Mapp R1 [9] B1 [4] VSYNC B1 [3] B1 [1] R2 [9] B2 [4]	Ding R1 [8] G1 [9] HSYNC B1 [2] B1 [0] R2 [8]	(R1 [7]) (G1 [0]) (B1 [9]) (G1 [3]) (G1 [1]) (R2 [7])	R1 [6] G1 [7] B1 [8] G1 [2] G1 [0] R2 [6]	(R1 [5]) (G1 [6]) (B1 [7]) (R1 [3]) (R1 [1]) (R2 [5])	R1 [4] G1 [5] B1 [6] R1 [2] R1 [0] R2 [4]	G3 [4] B3 [5] DE data 11 data 12 G4 [4]	(R3 [9]) (B3 [4]) (VSYNC) (B3 [3]) (B3 [1]) (R4 [9]) (B4 [4])	R3 [8] G 3 [9] HSYNC B3 [2] B3 [0] R4 [8]	R3 [7] G3 [8] B3 [9] G3 [3] G3 [1] R4 [7]	(R3 [6]) (G3 [7]) (B3 [8]) (G3 [2]) (G3 [0]) (R4 [6]) (G4 [7])	(R3 [5] (G3 [6] (B3 [7] (R3 [3] (R3 [1] (R4 [5]	X R3 [4] X G3 [5] X B3 [6] X R3 [2] X R3 [0]
RE2+/	Output         ) G1 [4] (         ) G1 [4] (         ) B1 [5] (         ) DE (         ) data11 (         ) data12 (         ) G2 [4] (         ) B2 [5] (         ) DE (	Mapp R1 [9] B1 [4] VSYNC B1 [3] B1 [1] R2 [9] B2 [4]	Ding R1 [8] G1 [9] HSYNC B1 [2] B1 [0] R2 [0] G2 [9]	(R1 [7]) (G1 [8]) (B1 [9]) (G1 [3]) (G1 [1]) (G1 [1]) (R2 [7]) (G2 [8])	R1 [6] G1 [7] B1 [8] G1 [2] G1 [0] R2 [6] G2 [7]	(R1 [5]) (G1 [5]) (B1 [7]) (R1 [3]) (R1 [1]) (R2 [5]) (G2 [5])	R1 [4] G1 [5] B1 [6] R1 [2] R1 [0] R2 [4] G2 [5]	G3 [4] B3 [5] DE (data 11) (data 12) G4 [4] B4 [5]	(R3 [9]) (B3 [4]) (VSYNC) (B3 [3]) (B3 [1]) (R4 [9]) (B4 [4])	R3 [8]         G3 [9]         HSYNC         B3 [2]         B3 [0]         R4 [8]         G4 [9]	R3 [7] G3 [8] B3 [9] G3 [3] G3 [1] R4 [7] G4 [8]	(R3 [6] (G3 [7] (B3 [8] (G3 [2] (G3 [0] (R4 [6] (G4 [7]	(R3 [5] (G3 [6] (B3 [7] (R3 [3] (R3 [1] (R4 [5] (G4 [6]	X R3 [4] X G3 [5] X B3 [6] X R3 [2] X R3 [0] X R4 [4] X G4 [5]
RE2+/- VDS-Tx ( TCLK1+ TA1+/- TB1+/- TC1+/- TD1+/-	Output         ) G1 [4] (         ) G1 [4] (         ) B1 [5] (         ) DE (         ) data11 (         ) data12 (         ) G2 [4] (         ) B2 [5] (         ) DE (	Mapp R1 [9]) B1 [4]) VSYNC) B1 [3]) B1 [1]) B2 [9]) B2 [4]) VSYNC) B2 [3])	R1 [8]           G1 [9]           HSYNC           B1 [2]           B1 [0]           R2 [8]           G2 [9]           HSYNC	(R1 [7]) (G1 [8]) (B1 [9]) (G1 [3]) (G1 [1]) (G1 [1]) (R2 [7]) (G2 [8]) (B2 [9])	R1 [6] G1 [7] B1 [8] G1 [2] G1 [0] R2 [6] G2 [7] B2 [8]	(R1 [5]) (G1 [6]) (B1 [7]) (R1 [3]) (R1 [1]) (R2 [5]) (G2 [6]) (B2 [7]) (R2 [3])	R1 [4] G1 [5] B1 [6] R1 [2] R1 [0] R2 [4] G2 [5] B2 [6] R2 [2]	(G3 [4]) (B3 [5]) (DE) (data 11) (data 12) (G4 [4]) (B4 [5]) (DE)	(R3 [9]) (B3 [4]) (VSYNC) (B3 [3]) (B3 [1]) (B3 [1]) (R4 [9]) (B4 [4]) (VSYNC) (B4 [3])	R3 [8]         G3 [9]         HSYNC         B3 [2]         B3 [0]         R4 [8]         G4 [9]	R3 [7] G3 [8] B3 [9] G3 [3] G3 [1] R4 [7] G4 [8] B4 [9]	(R3 [6]) (G3 [7]) (B3 [8]) (G3 [2]) (G3 [0]) (R4 [6]) (G4 [7]) (B4 [8]) (G4 [2])	(R3 [5] (G3 [6] (B3 [7] (R3 [3] (R3 [1] (R4 [5] (G4 [6] (B4 [7]	X R3 [4] X G3 [5] X B3 [6] X R3 [2] X R3 [0] X R4 [4] X G4 [5] X B4 [6]

Data bits "data11, data12, data21, data22" are available for additional data transmission.





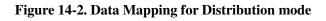
### **Distribution Mode**

In Distribution mode, RCLK2+/- must be Hi-Z.

### LVDS-Rx Input Mapping

CLK1+							
A1+/-	↓ G1 [4] ↓ R1 [9] ↓ R1 [8] ↓ R1 [7] ↓ R1 [6] ↓ R1 [5] ↓ R1 [4] ↓ G2 [4] ↓ R2 [9] ↓ R2 [8] ↓ R2 [7] ↓ R2 [6] ↓ R2 [5] ↓ R2						
B1+/- =							
C1+/-	$\int \text{DE} \left( \text{VSYNC} \left( \text{HSYNC} \right) \text{B1} [9] \right) \text{B1} [8] \left( \text{B1} [7] \right) \text{B1} [6] \left( \text{DE} \left( \text{VSYNC} \right) \text{HSYNC} \right) \text{B2} [9] \left( \text{B2} [8] \right) \text{B2} [7] \left( \text{B2} [7] \right) \text{B2} [7] \right) \text{B2} [7]$						
D1+/-	$\int data11 \int B1 [3] \int B1 [2] \int G1 [3] \int G1 [2] \int R1 [3] \int R1 [3] \int R1 [2] \int data11 \int B2 [3] \int B2 [2] \int G2 [3] \int G2 [2] \int R2 [3] \int$						
E1+/-	$ \left( \frac{data12}{B1} \left[ 1 \right] \times B1 \left[ 0 \right] \times G1 \left[ 1 \right] \times G1 \left[ 0 \right] \times R1 \left[ 1 \right] \times R1 \left[ 0 \right] \times data12 \times B2 \left[ 1 \right] \times B2 \left[ 0 \right] \times G2 \left[ 1 \right] \times G2 \left[ 0 \right] \times R2 \left[ 1 \right] \times R2 \left[$						
CLK2+	Hi-Z						
A2+/-	no care						
8 <b>B2+</b> /-	no care						
C2+/-	no care						
2D2+/-	no care						
2E2+/-	Output Mapping						
	Output Mapping						
	Output Mapping (G1 [4] ( R1 [9] ( R1 [8] ( R1 [7] ( R1 [6] ( R1 [5] ( R1 [4] ( G2 [4] ( R2 [9] ( R2 [8] ( R2 [7] ( R2 [6] ( R2 [5] (R2 [5] (R2 [5] (R2 [5] (R2 [5) (R2 [5) (R2 [5) (R2						
= DS-Tx ( clk1+ = A1+/- = B1+/- =	Output Mapping (G1 (4) (R1 (9) (R1 (8) (R1 (7) (R1 (6) (R1 (5) (R1 (4) (G2 (4) (R2 (9) (R2 (8) (R2 (7) (R2 (6) (R2 (5) (R2 (12 (12 (12 (12 (12 (12 (12 (12 (12 (1						
	Output Mapping         (G1 [4] (R1 [9] (R1 [8] (R1 [7] (R1 [6] (R1 [5] (R1 [4] (G2 [4] (R2 [9] (R2 [8] (R2 [7] (R2 [6] (R2 [5] (R2 [5						
	Output Mapping         (G1 [4] \ R1 [9] \ R1 [8] \ R1 [7] \ R1 [6] \ R1 [5] \ R1 [4] \ G2 [4] \ R2 [9] \ R2 [8] \ R2 [7] \ R2 [6] \ R2 [5] \ R2 [6] \ G2 [7] \ G2 [7] \ G2 [6] \ G2 [7] \ G2 [7] \ G2 [6] \ G2 [7] \ G2						
	Output Mapping         (G1 [4] (R1 [9] (R1 [8] (R1 [7] (R1 [6] (R1 [5] (R1 [4] (G2 [4] (R2 [9] (R2 [8] (R2 [7] (R2 [6] (R2 [5] (R2 [5						
	Output Mapping         (G1 [4] \ R1 [9] \ R1 [8] \ R1 [7] \ R1 [6] \ R1 [5] \ R1 [4] \ G2 [4] \ R2 [9] \ R2 [8] \ R2 [7] \ R2 [6] \ R2 [5] \ R2 [6] \ G2 [7] \ G2 [7] \ G2 [6] \ G2 [7] \ G2 [7] \ G2 [6] \ G2 [7] \ G2						
	Output Mapping         (G1 [4] \ R1 [9] \ R1 [8] \ R1 [7] \ R1 [6] \ R1 [5] \ R1 [4] \ G2 [4] \ R2 [9] \ R2 [8] \ R2 [7] \ R2 [6] \ R2 [5] \ R2 [6] \ G2 [7] \ G2 [7] \ G2 [6] \ G2 [7] \ G2 [7] \ G2 [6] \ G2 [7] \ G2						
	Output Mapping         (G1 [4] (R1 [9] (R1 [8] (R1 [7] (R1 [6] (R1 [5] (R1 [4] (G2 [4] (R2 [9] (R2 [8] (R2 [7] (R2 [6] (R2 [5] (G2 [7] (G2 [6] (G2 [7] (G2 [7						
	Output Mapping         G1 [4] (R1 [9] (R1 [8] (R1 [7]) (R1 [6] (R1 [5] (R1 [4] G2 [4] (R2 [9] (R2 [8] (R2 [7] (R2 [6] (R2 [5] (R2 [5)						
	Output Mapping         G1 [4] (R1 [9] (R1 [8] (R1 [7] (R1 [6] (R1 [5] (R1 [4] G2 [4] (R2 [9] (R2 [8] (R2 [7] (R2 [6] (R2 [5] (R2 [3] (R2 [7] (G2 [6] (G2 [3] (G2 (G1 [2] (R1 [3] (R1 [2] (data11) B2 [3] (B2 [2] (G2 [3] (G2 [2] (R2 [3] (R2 [3] (G2 [3] (G2 [2] (R2 [3] (R2 [3] (R1 [3] (R1 [2] (data11) B2 [3] (B2 [2] (G2 [3] (G2 [2] (R2 [3] (R2 [3] (G1 [2] (R1 [3] (R1 [3] (R1 [2] (data11) B2 [3] (B2 [2] (G2 [3] (G2 [2] (R2 [3]						







#### Single-In / Dual-Out

In Single-in / Dual-out mode, RCLK2+/- must be Hi-Z.



RCLK1+	1						1
		<u> </u>					/
RA1+/-	G1 [4] R1 [9]	R1 [8] R1 [7]	R1 [6] R1 [5]	R1 [4] G2 [4]	R2 [9] R2 [8]	R2 [7] R2 [6]	R2 [5] R2 [4
RB1+/-	B1 [5] B1 [4]	G1 [9] G1 [8]	G1 [7] G1 [6]	G1 [5] B2 [5]	B2 [4] G2 [9]	G2 [8] G2 [7]	G2 [6] G2 [5
RC1+/-	DE	HSYNC B1 [9]	B1 [8] B1 [7]	B1 [6] DE	VSYNCHSYNC	B2 [9] B2 [8]	B2 [7] 82 [6
RD1+/-	data11 B1 [3]	B1 [2] G1 [3]	G1 [2] R1 [3]	R1 [2] data11	B2 [3] B2 [2]	G2 [3] G2 [2]	R2 [3] R2 [2
RE1+/-	(data12) B1 [1]	B1 [0] G1 [1]	G1 [0] R1 [1]	R1 [0] data12	B2 [1] B2 [0]	G2 [1] G2 [0]	R2 [1] R2 [0
RCLK2+				Hi-Z			
RA2+/-				no care			
RB2+/-				no care			
RC2+/-				no care			
RD2+/-				no care			
RE2+/-	utput Map	ping		no care			
UDS-Tx O			V R1 [8]	 	R1 [6]	R1 [5]	R1 [4]
	G1 [4]	R1 [9]	R1 [8]	R1 [7]	R1 [6]	R1 [5]	R1 [4]
			R1 [8]	 	R1 [6] G1 [7] B1 [8]	R1 [5] G1 [6] B1 [7]	R1 [4] G1 [5] B1 [6]
UDS-Tx O TCLK1+	G1 [4]	R1 [9] B1 [4]	G1 [9]	R1 [7]	G1 [7]	G1 [6]	G1 [5]
VDS-Tx O TCLK1+ — TA1+/- — TB1+/- — TC1+/- —	G1 [4] B1 [5]	R1 [9] B1 [4] VSYNC		(R1 [7] (G1 [8] (B1 [9]	G1 [7]	G1 [6] B1 [7]	G1 [5]
VDS-Tx O TCLK1+ — TA1+/- — TB1+/- — TC1+/- — TD1+/- —	G1 [4] B1 [5] DE data11	R1 [9] B1 [4] VSYNC B1 [3]	G1 [9] HSYNC B1 [2]	(R1 [7]) (G1 [8] (B1 [9]) (G1 [3]	G1 [7] B1 [8] G1 [2]	G1 [6] B1 [7] R1 [3]	G1 [5] B1 [6] R1 [2]
VDS-Tx O TCLK1+ — TA1+/- — TB1+/- — TC1+/- — TD1+/- — TE1+/- —	G1 [4] B1 [5] DE data11	R1 [9] B1 [4] VSYNC B1 [3]	G1 [9] HSYNC B1 [2]	(R1 [7]) (G1 [8] (B1 [9]) (G1 [3]	G1 [7] B1 [8] G1 [2]	G1 [6] B1 [7] R1 [3]	G1 [5] B1 [6] R1 [2]
VDS-Tx O TCLK1+ TA1+/- TB1+/- TC1+/- TC1+/- TC1+/- TE1+/- TCLK2+ TA2+/- TA2+/-	G1 [4]       B1 [5]       DE       data11       data12	R1 [9] B1 [4] VSYNC B1 [3] B1 [1]	G1 [9] HSYNC B1 [2] B1 [0]	R1 [7] G1 [8] B1 [9] G1 [3] G1 [1]	G1 [7] B1 [8] G1 [2] G1 [0]	G1 [6] B1 [7] R1 [3] R1 [1]	G1 [5] B1 [6] R1 [2] R1 [0]
/DS-Tx O rCLK1+	G1 [4] B1 [5] DE data11 data12	R1 [9] B1 [4] VSYNC B1 [3] B1 [1] R2 [9]	G1 [9] HSYNC B1 [2] B1 [0] R2 [8]	R1 [7] G1 [8] B1 [9] G1 [3] G1 [1] R2 [7]	G1 [7] B1 [8] G1 [2] G1 [0] R2 [6]	G1 [6] B1 [7] R1 [3] R1 [1] R2 [5]	G1 [5] B1 [6] R1 [2] R1 [0] R2 [4]
VDS-Tx O TCLK1+ — TA1+/- — TB1+/- — TC1+/- — TD1+/- — TE1+/- — TCLK2+ —	G1 [4] B1 [5] DE data11 data12 G2 [4] B2 [5]	R1 [9] B1 [4] VSYNC B1 [3] B1 [1] R2 [9] B2 [4]	G1 [9] HSYNC B1 [2] B1 [0] R2 [8] G2 [9]	R1 [7] G1 [8] B1 [9] G1 [3] G1 [1] R2 [7] G2 [8]	G1 [7] B1 [8] G1 [2] G1 [0] R2 [6] G2 [7]	G1 [6] B1 [7] R1 [3] R1 [1] R2 [5] G2 [6]	G1 [5] B1 [6] R1 [2] R1 [0] R2 [4] G2 [5]

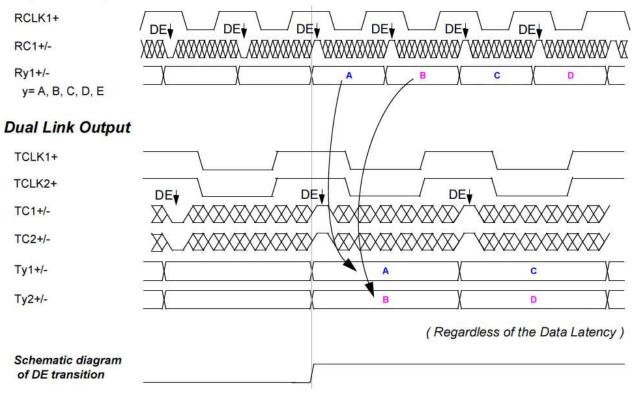
(Regardless of the Data Latency)

Data bits "data11, data12" are available for additional data transmission.

Figure 14-3(a). Data Mapping for Single-In/Dual-Out



### Single Link Input



Single-in / Dual-out mode uses DE signal L-to-H-edge to start distribution of input data.

Figure 14-3(b). Data Mapping for Single-In/Dual-Out



Dual-In / Single-Out
LVDS-Rx Input Mapping

RCLK1+					1		
RA1+/-	G1 [4]	R1 [9]	R1 [8]	R1 [7]	R1 [6]	R1 [5]	R1 [4]
RB1+/-	B1 [5]	B1 [4]	G1 [9]	G1 [8]	G1 [7]	G1 [6]	G1 [5]
RC1+/-	DE	VSYNC	HSYNC	B1 [9]	B1 [8]	B1 [7]	B1 [6]
RD1+/-	data11	B1 [3]	B1 [2]	G1 [3]	G1 [2]	R1 [3]	R1 [2]
RE1+/-	data12	B1 [1]	B1 [0]	G1 [1]	G1 [0]	R1 [1]	R1 [0]
RCLK2+						[	
RA2+/-	G2 [4]	R2 [9]	R2 [8]	R2 [7]	R2 [6]	R2 [5]	R2[4]
RB2+/-	B2 [5]	B2 [4]	G2 [9]	G2 [8]	G2 [7]	G2 [6]	G2 [5]
RC2+/-	DE	VSYNC	HSYNC	B2 [9]	B2 [8]	B2 [7]	B2 [6]
RD2+/-	data21	B2 [3]	B2 [2]	G2 [3]	G2 [2]	R2 [3]	R2 [2]
RE2+/-	data22	B2[1]	B2 [0]	G2 [1]	G2 [0]	R2 [1]	R2 [0]
	Output Mapp		·,				Γ
CLK1+		oing					[
CLK1+	Output Mapp (G1 [4] (R1 [9])		(R1 [6] (R1 [5])	R1 [4] G2 [4]	(R2[9]) R2[8])	R2 [7] X R2 [6]	(R2 [5] (R2 [4]
TCLK1+		oing	(R1 [6] (R1 [5]) (G1 [7] (G1 [6])	R1 [4] (G2 [4]) G1 [5] B2 [5]	(R2[9])(R2[8]) (B2[4])(G2[9])	R2 [7] X R2 [6] G2 [8] G2 [7]	(R2 [5] (R2 [4] (G2 [6] (G2 [5]
/DS-Tx ( rclK1+	X G1 [4] X R1 [9] X B1 [5] X B1 [4]	Ding					
TCLK1+	X G1 [4] X R1 [9] X B1 [5] X B1 [4]	Ding (R1 [8] ( R1 [7]) (G1 [9] ( G1 [8])	(G1 [7] (G1 [6]) (B1 [8] (B1 [7])	G1 [5] B2 [5] B1 [6] DE	B2 [4] (G2 [9]	G2 [8] \ G2 [7]	(G2 [6] (G2 [5]
rCLK1+ rA1+/- rB1+/- rC1+/- rD1+/-	(G1 [4]) (R1 [9]) (B1 [5] (B1 [4]) (DE (VSYNC)	Ding (R1 [8] (R1 [7]) (G1 [9] (G1 [8]) (HSYNC (B1 [9])	(G1 [7] (G1 [6]) (B1 [8] (B1 [7])	G1 [5] B2 [5] B1 [6] DE	(B2 [4] (G2 [9]) (VSYNC (HSYNC (B2 [3] (B2 [2])	G2 [8] X G2 [7] B2 [9] X B2 [8]	(G2 [6] (G2 [5] (B2 [7] B2 [6]
rCLK1+	<pre>(G1 [4] (R1 [9]) (B1 [5] (B1 [4]) (DE (VSYNC) (data11)(B1 [3])</pre>	Ding (R1 [8] (R1 [7]) (G1 [9] (G1 [8]) (HSYNC (B1 [9]) (B1 [2] (G1 [3])	(G1 [7] (G1 [6]) (B1 [8] (B1 [7]) (G1 [2] (R1 [3])	G1 [5] / B2 [5] B1 [6] / DE R1 [2] / data21	(B2 [4] (G2 [9]) (VSYNC (HSYNC (B2 [3] (B2 [2])	G2 [8] (G2 [7] B2 [9] (B2 [8] G2 [3] (G2 [2]	(G2 [6]) (G2 [5] (B2 [7]) (B2 [6] (R2 [3]) (R2 [2]
rCLK1+	<pre>(G1 [4] (R1 [9]) (B1 [5] (B1 [4]) (DE (VSYNC) (data11)(B1 [3])</pre>	Ding (R1 [8] (R1 [7]) (G1 [9] (G1 [8]) (HSYNC (B1 [9]) (B1 [2] (G1 [3])	(G1 [7] (G1 [6]) (B1 [8] (B1 [7]) (G1 [2] (R1 [3])	G1 [5] B2 [5] B1 [6] DE R1 [2] data21 R1 [0] data22	(B2 [4] (G2 [9]) (VSYNC (HSYNC (B2 [3] (B2 [2])	G2 [8] (G2 [7] B2 [9] (B2 [8] G2 [3] (G2 [2]	(G2 [6]) G2 [5] (B2 [7]) B2 [6] (R2 [3]) R2 [2]
rCLK1+	<pre>(G1 [4] (R1 [9]) (B1 [5] (B1 [4]) (DE (VSYNC) (data11)(B1 [3])</pre>	Ding (R1 [8] (R1 [7]) (G1 [9] (G1 [8]) (HSYNC (B1 [9]) (B1 [2] (G1 [3])	(G1 [7] (G1 [6]) (B1 [8] (B1 [7]) (G1 [2] (R1 [3])	G1 [5] B2 [5] B1 [6] DE R1 [2] data21 R1 [0] data22 Hi-Z	(B2 [4] (G2 [9]) (VSYNC (HSYNC (B2 [3] (B2 [2])	G2 [8] (G2 [7] B2 [9] (B2 [8] G2 [3] (G2 [2]	(G2 [6]) (G2 [5] (B2 [7]) (B2 [6] (R2 [3]) (R2 [2]
rCLK1+	<pre>(G1 [4] (R1 [9]) (B1 [5] (B1 [4]) (DE (VSYNC) (data11)(B1 [3])</pre>	Ding (R1 [8] (R1 [7]) (G1 [9] (G1 [8]) (HSYNC (B1 [9]) (B1 [2] (G1 [3])	(G1 [7] (G1 [6]) (B1 [8] (B1 [7]) (G1 [2] (R1 [3])	G1 [5] B2 [5] B1 [6] DE R1 [2] data21 R1 [0] data22 Hi-Z Hi-Z	(B2 [4] (G2 [9]) (VSYNC (HSYNC (B2 [3] (B2 [2])	G2 [8] (G2 [7] B2 [9] (B2 [8] G2 [3] (G2 [2]	(G2 [6]) G2 [5] (B2 [7]) B2 [6] (R2 [3]) R2 [2]
rCLK1+ rA1+/- rB1+/- rC1+/-	<pre>(G1 [4] (R1 [9]) (B1 [5] (B1 [4]) (DE (VSYNC) (data11)(B1 [3])</pre>	Ding (R1 [8] (R1 [7]) (G1 [9] (G1 [8]) (HSYNC (B1 [9]) (B1 [2] (G1 [3])	(G1 [7] (G1 [6]) (B1 [8] (B1 [7]) (G1 [2] (R1 [3])	G1 [5] B2 [5] B1 [6] DE R1 [2] data21 R1 [0] data22 Hi-Z Hi-Z Hi-Z	(B2 [4] (G2 [9]) (VSYNC (HSYNC (B2 [3] (B2 [2])	G2 [8] (G2 [7] B2 [9] (B2 [8] G2 [3] (G2 [2]	(G2 [6]) (G2 [5] (B2 [7]) (B2 [6] (R2 [3]) (R2 [2]

(Regardless of the Data Latency)

Data bits "data11, data12, data21, data22" are available for additional data transmission.

Figure 14-4. Data Mapping for Dual-In/Single-Out



#### <u>Notes</u>

#### 1) LVDS input pin connection

When LVDS line is not derived from the previous device, the line is pulled up to 3.3V internally in THC63LVD1027. This can cause violation of absolute maximum ratings to the previous LVDS Tx device whose operating condition is lower voltage power supply than 3.3V. This phenomenon may happen at power on phase of the whole system including THC63LVD1027. One solution for this problem is PD=L control during no LVDS input period because pull-up resistors are cut off at power down state.

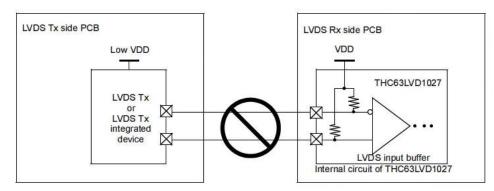


Figure 15. LVDS input pin connection

#### 2) Power On Sequence

Don't input RCLK1+/- and RCLK2+/- before THC63LVD1027 is on in order to keep absolute maximum ratings.



#### 3) Cable Connection and Disconnection

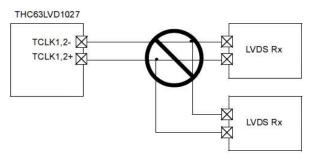
Don't connect and disconnect the LVDS cable, when the power is supplied to the system.

#### 4) GND Connection

Connect the each GND of the PCB which Transmitter, Receiver and THC63LVD1027 on it. It is better for EMI reduction to place GND cable as close to LVDS cable as possible.

#### 5) Multi Drop Connection

Multi drop connection is not recommended.



#### Figure 16.Multi Drop Connection

#### 6) Asynchronous use

Asynchronous use such as following systems are not recommended. Page.11 tCK12 spec should be kept.

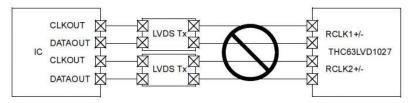


Figure 17-1. Asynchronous Use1

Asynchronous use such as following systems are not recommended.

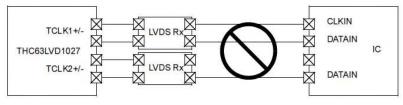


Figure 17-2. Asynchronous Use2

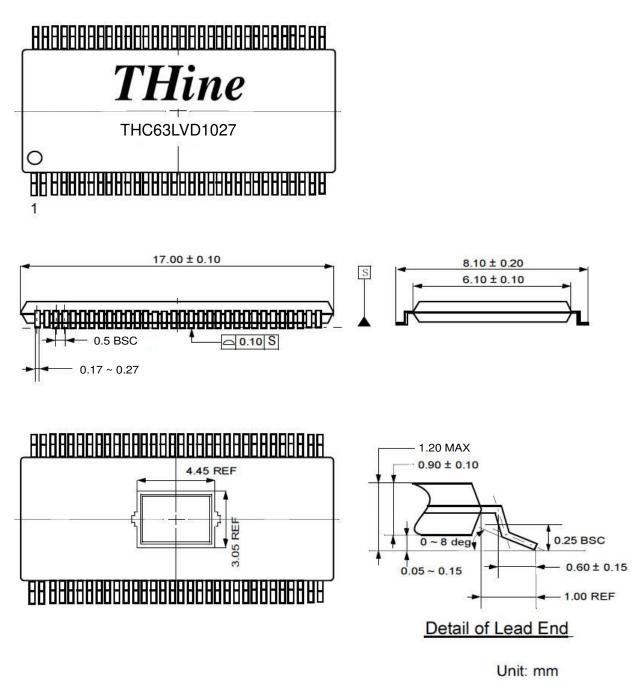
#### 7) De-coupling capacitor

THC63LVD1027 requires appropriate de-coupling capacitor placement on VDD. Especially, VDD pin 36 and pin 61 requires 0.1uF and 4.7nF capacitor parallel placement close to IC pins.

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### Package



Exposed PAD is GND and must be soldered to PCB.

Figure 18. Package Diagram



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- 10. The product or peripheral parts may be damaged by a surge in voltage over the absolute maximum ratings or malfunction, if pins of the product are shorted by such as foreign substance. The damages may cause a smoking and ignition. Therefore, you are encouraged to implement safety measures by adding protection devices, such as fuses.

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