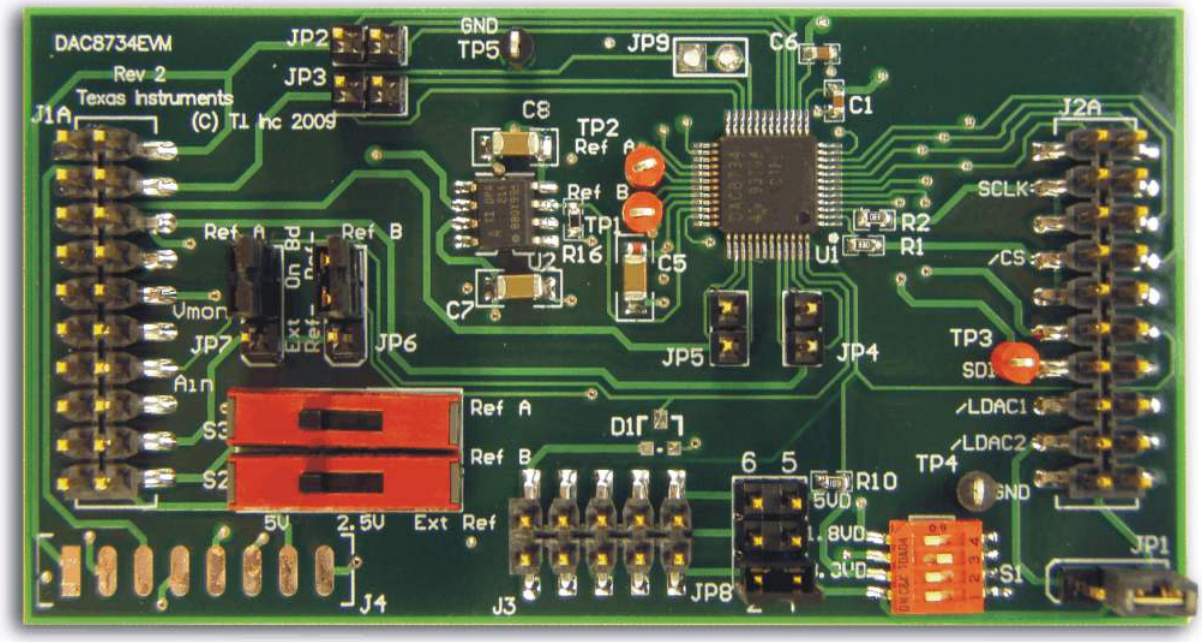
DAC8734EVM



DAC8734EVM

This user's guide describes the characteristics, operation, and use of the DAC8734EVM. The evaluation module (EVM) is an evaluation board that allows for quick and easy evaluation of the DAC8734. The DAC8734 is a quad, high-accuracy, 16-bit R-2-R digital-to-analog converter (DAC). The device features low-power operation, good linearity, and the ability to use different reference voltages for the output channels. This EVM allows evaluation of all aspects of the DAC8734. Complete circuit descriptions, schematic diagrams, and bill of material are included in this document.

The following related documents are available through the Texas Instruments web site at http://www.ti.com.

EVM-Compatible Device Data Sheets

Device	Literature Number
DAC8734	SBAS465
REF5025	SBOS410
REF5050	SBOS410
OPA211	SBOS377
TL750L08	SLVS017

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1 EVM Overview

1.1 Features

DAC8734EVM:

- Contains all support circuitry needed for the DAC8734
- Voltage reference options: Either 5V or 2.5V onboard, or external
- Jumpers on output pins for gain adjustment
- Compatible with the TI Modular EVM System

This manual covers the operation of the DAC8734EVM. Throughout this document, the abbreviation *EVM* and the term *evaluation module* are synonymous with the DAC8734EVM.

1.2 Introduction

The DAC8734 uses a high speed SPI interface (up to 50MHz) to communicate with a DSP or a microprocessor using a compatible serial interface. The DAC features four individual outputs whose gain is controlled by the addition of a feedback resistor. An additional V_{MON} pin can relay any of the four output channels from the DAC or the signal from the A_{IN} pin.

The DAC8734EVM is designed to be run in either bipolar (default mode) or unipolar modes of operation. This flexible design allows for a wide range of supply voltages. The operating mode can be controlled using an onboard switch or digitally, through the digital header.

The DAC8734EVM is an evaluation module built to the TI Modular EVM System specification. It can be connected to any modular EVM system interface card. The EVM ships in the TQFP-48 DAC8734 pin package option.

Note that the DAC8734EVM has no microprocessor and cannot run software. To connect it to a computer, some type of interface is required.

2 Analog Interface

For maximum flexibility, the DAC8734EVM can interface to multiple analog sources. Samtec part numbers SSW-110-22-F-D-VS-K and TSM-110-01-T-DV-P provide a 10-pin, dual-row, header at J1. This header provides access to the analog input and output pins of the DAC. Consult Samtec at http://www.samtec.com or call 1-800-SAMTEC-9 for a variety of mating connector options.

Table 1 summarizes the pinouts for analog interface J1.

Table 1. J1: Analog Interface Pinout

Pin Number	Signal	Description
J1.1	SGND-0	Signal GND DAC output 0
J1.2	V_{OUT}-0	Analog output 0
J1.3	SGND-1	Signal GND DAC output 1
J1.4	V_{OUT}-1	Analog output 1
J1.5	SGND-2	Signal GND DAC output 2
J1.6	V_{OUT}-2	Analog output 2
J1.7	SGND-3	Signal GND DAC output 3
J1.8	V_{OUT}-3	Analog output 3
J1.9-13 (odd)	AGND	Analog ground connections
J1.10	V_{MON_BUF}	Monitor output after buffer
J1.14	A_{IN}	Auxiliary analog input
J1.15	Unused	—
J1.17-19 (odd)	AGND	Analog ground connections
J1.18	RefGND	Reference ground pins on the DAC8734 (see below)
J1.20	EXTREF+	External reference source input (+ side of reference input)
J1.12	Unused	—
J1.16	Unused	—

The analog interface is populated on the top of the evaluation model. This configuration makes it possible to stack multiple EVMs to run them in daisy-chain mode. J4 can be installed with a 90-degree connector to allow access to the analog outputs if multiple EVMs are stacked. The J1B connector can be installed if the part is used as a standalone board.

The DAC8734 can be configured with an output gain of 2 or 4. By default, the analog outputs of the DAC8734EVM are configured with a gain of 4. If a gain of 2 is desired, the proper jumper must be installed (JP2-JP5, depending on the output channel), and the command register must be set accordingly.

The SGND pins of the DAC8734 are connected to the ground of the evaluation board.

The Auxiliary Analog Input pin can be further protected from over-voltage and over-driving conditions. A Schottky diode (D1) can be installed to protect the DAC8734 from an input over-voltage condition. An op amp buffer is placed on the V_{MON} output to limit the current that passes through the pin.

The DAC8734EVM has an external reference voltage option. If an external reference voltage is used, switches S2 and S3 must be properly configured. Use the EXTREF+ (J1.20) to apply an external reference voltage.

The DAC8734 is designed to have the REFGND-A and REFGND-B pins within 0.3V of the AGND. Therefore, we recommend not using the RefGND pin when connecting an external reference. Connect the ground source of the reference voltage to the ground of the board (J1.19). See the *Reference Voltage* section for more information.

3 Digital Interface

The DAC8734EVM is a serial input data converter. The evaluation module is designed for interfacing to multiple control platforms.

3.1 Serial Data Interface

Samtec part numbers SSW-110-22-F-D-VS-K and TSM-110-01-T-DV-P provide a 10-pin, dual-row, header/socket combination at J2. This header/socket provides access to the digital control and serial data pins from both J2A (top side) and J2B (bottom side) of the connector. Consult Samtec at http://www.samtec.com or call 1-800-SAMTEC-9 for a variety of mating connector options.

Table 2 describes the serial interface pins.

Table 2. J2: Serial Interface Pins(1)

Pin No.	Signal Name	I/O Type	Pullup	Function
J2.1	Unused	—	—	
J2.2	GPIO-0	In/Out	High	GPIO-0
J2.3 J2.5	SCLK	In	None	DAC8734 SPI clock; pins are shorted together
J2.4	DGND	In/Out	None	Digital ground
J2.6	GPIO-1	In/Out	High	GPIO-1
J2.7 J2.9	$\overline{CS}$	In	None	SPI bus chip select; pins are shorted together
J2.8	Uni/Bip A	In	High	Output mode select of Group A
J2.10	DGND	In/Out	None	Digital ground
J2.11	SDO/SDI	In/Out	None	DAC8734 SPI data in/out
J2.12	Uni/Bip B	In	High	Output mode select of Group B
J2.13	Unused	—	—	
J2.14	RST	In	High	Input register reset
J2.15	$\overline{LDAC}$	In	High	GPIO signal to control LDAC for DAC output latch update
J2.16	Unused	—	—	
J2.17	$\overline{LDAC}$	In	High	Alternate GPIO signal to control LDAC for DAC output latch update
J2.18	DGND	In/Out	None	Digital ground
J2.19	Unused	—	—	
J2.20	Unused	—	—	

(1) Group A contains V_{OUT}-0 and V_{OUT}-1. Group B contains V_{OUT}-2 and V_{OUT}-3.

The SCLK signal and the $\overline{CS}$ signal can each be controlled by two different pins on J2. Pins J2.3 and J2.5 have been shorted together, as well as pins J2.7 and J2.9.

Pins J2.8, J2.12, J2.14, J2.15, and J2.17 have weak pull-up/pulldown resistors. These resistors provide default settings for many of the control pins. J2.3, J2.5, J2.7, J2.9, J2.11 correspond directly to DAC8734 pins. See the DAC8734 product data sheet for complete details on these pins.

Control signals to and from the DAC8734 can be accessed through the digital interface, or switches and jumpers found directly on the EVM. The /LDAC, Uni/Bip A, Uni/Bip B, and $\overline{RST}$ signals are initially pulled high through 10kΩ resistors and can be controlled by switch S1 or through J2.

The load DAC ($\overline{LDAC}$) pin is connected via jumper JP1 to either the J2.15 or J2.17 pin. Updating the DAC registers can be completed in two different ways. $\overline{LDAC}$ can either be tied to ground, in which case the input registers are immediately updated, or $\overline{LDAC}$ can be pulled high. Therefore, the DAC registers update when $\overline{LDAC}$ is taken low. Switch S1.1 can be closed to hold the $\overline{LDAC}$ low. See the DAC8734 data sheet for more information on updating the DAC.

4 Power Supplies

Samtec part numbers SSW-105-22-F-D-VS-K and TSM-105-01-T-DV-P provide a 5-pin, dual-row, header/socket combination at J3. Table 3 lists the configuration details for J3. The voltage inputs to the DAC can be applied directly to the device. The DAC8734 requires multiple power supplies to operate. AVDD, AVSS, DVDD, and IOVDD are required to properly power the DAC.

Table 3. J3 Configuration: Power-Supply Input

Pin No.	Pin Name	Function	Required
J3.1	+VA	+4.75V to +24V analog supply	Yes
J3.2	–VA	–18V to –4.75V analog supply	Yes
J3.3	+5VA	+5V analog supply	No
J3.4	–5VA	–5V analog supply	No
J3.5	DGND	Digital ground input	Yes
J3.6	AGND	Analog ground input	Yes
J3.7	+1.8VD	1.8V digital supply	Optional
J3.8	VD1	Not used	No
J3.9	+3.3VD	3.3V digital supply	Optional
J3.10	+5VD	+5V	Yes

The Digital and Analog ground inputs are short-circuited internally through a ground plane.

The dc logic voltage for the DAC8734 (IOVDD) is selectable between +3.3VD, +1.8VD, or +5VD via the JP8 jumper. These power-supply voltages are referenced to digital ground.

The DAC8734EVM is designed to work in either unipolar and bipolar mode. Each mode requires different power-supply connections. Consult the DAC8734 data sheet for the restrictions on the power supplies for the two operating modes.

5 Reference Voltage

The DAC8734EVM has the ability to use two different reference sources simultaneously for different output channels. REFA and REFB control the reference voltages for the DAC. Output channels V_{OUT}-0 and V_{OUT}-1 use REFA as a reference. REFB is used as a reference for output channels V_{OUT}-2 and V_{OUT}-3.

The evaluation module has three options for supplying reference voltages to the DAC8734. Switch S3 (REFA) and S2 (REFB) can select the reference voltage from the REF5050 (U5), REF5025 (U4) or use an external reference. The REF5050 supplies 5.0V to the reference. The REF5025 supplies 2.5V to the reference. These reference voltages are additionally filtered through an RC filter before connecting to the DAC8734. The TL751L08 is used to voltage regulate +VA to properly power the REF5025 and REF5050.

When using an external reference, make sure that the ground terminal (from the external source) is connected to the ground of the EVM board. There is a built-in diode in the DAC8734 that does not allow the RefGND-A/RefGND-B to have more than a 0.3V difference from the board AGND on the DAC. A jumper across pins 2 and 3 on JP6 and JP7 connects the RefGND-A and RefGND-B to the ground of the board.

Note that if an external reference voltage is input to J1.20, it will be filtered through a first-order, low-pass RC filter. To input your own reference signal without this filter, connect the reference signal directly to TP1 or TP2. Figure 1 shows the reference test points on the EVM.

Figure 1. Reference Test Points

6 EVM Operation

This section provides information on the analog input, digital control, and general operating conditions of the DAC8734EVM.

6.1 Analog Output

The DAC8734 has four analog outputs that are available through the J1 header or the J4 header. The J4 header is designed to use 90-degree Samtec pins (not installed) when multiple EVMs are stacked to be used in daisy-chain mode.

Jumpers J5-J8 control the gain of the individual output channels by connecting additional feedback resistors to the internal op amp buffer. See the DAC8734 data sheet for more information on setting the gain. Each analog output is able to swing ±16V in bipolar mode and 0 to 20V in unipolar mode.

The signal ground, SGND-N (for the output signals), are connected to header J1 and are short-circuited to the board ground. All of the output signals are referenced to the ground of the board.

V_{MON} is the channel monitor output. It can relay any of the four analog output signals or the A_{IN} signal. The V_{MON} signal is buffered and current-limited through the OPA227 (U2). By default, the V_{MON} pin is in 3-state mode, causing the op amp to saturate. In order to avoid the op amp saturating to a rail, a 200kΩ resistor is put in place. The resistor serves as a load for the op amp when the V_{MON} pin is in 3-state mode. However, as a result, there is an error of ~1% on the V_{MON_BUF} signal when relaying a signal.

6.2 Digital Control

The digital control signals can be applied directly to J1 (top or bottom side). The modular DAC8734EVM can also be connected directly to a DSP or microcontroller interface board.

No specific evaluation software is provided with this EVM; however, various code examples are available that show how to use EVMs with a variety of digital signal processors from Texas Instruments. Check the respective product folders or send an e-mail to dataconvapps@list.ti.com for a listing of available code examples. The EVM Gerber files are also available on request.

6.3 Default Jumper Settings and Switch Positions

Figure 2 shows the jumpers found on the EVM and the respective factory default conditions for each.

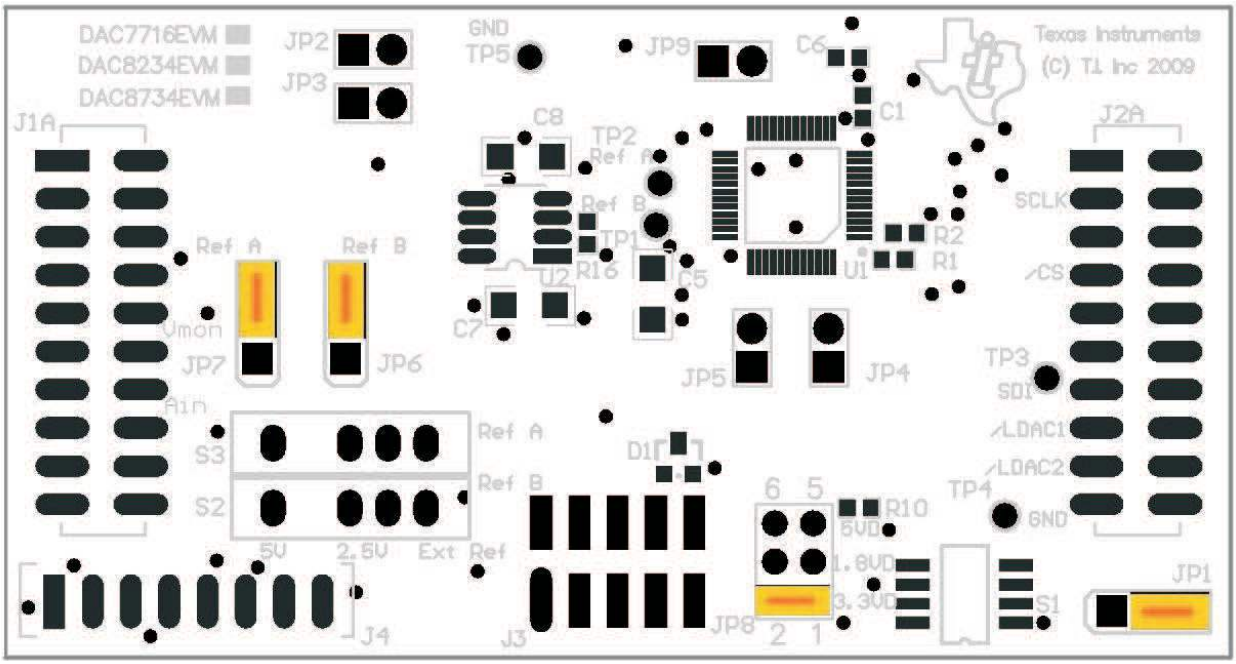

Figure 2. DAC8734EVM Default Jumper Locations

Jumper JP1 controls whether the $\overline{\text{LDAC}}$ signal is controlled by J2.15 or J2.17. By default, the $\overline{\text{LDAC}}$ signal is controlled by J2.17 but can be changed using JP1.

Jumpers JP2, JP3, JP4, and JP5 are used to control the gain of the individual DAC channels. By default, the jumpers are removed, resulting in each DAC channel having a gain of 4. The gain of the output channel is 2 when the corresponding jumper is in place.

JP6 and JP7 control the signals applied to REFGND-A and REFGND-B on the DAC8734. By default, a jumper is placed across JP6.2 and JP6.3 as well as JP7.2 and JP7.3. This jumper connects REFGND-A and REFGND-B to the ground of the board when an onboard reference is used. When an external reference source is used, it is recommended that this jumper stay in place and configure the external reference source to share a common ground with the EVM. See the *Reference Voltage* section for more information.

Jumper JP8 is used to control the digital voltage for IOVDD. By default, a jumper is in place to short-circuit pins JP8.1 and JP8.2 to use a 3.3V digital supply. If pins JP8.3 and JP8.4 are connected, a 1.8V digital supply will be used. If pins JP8.5 and JP8.6 are connected, a 5V digital supply will be used for IOVDD.

Jumper JP9 is not installed. If the user desires to disconnect RFB1 from V_{OUT1}, the trace between JP9 must be cut. JP9 can then be installed.

Switch S1 allows the user to pull down four control signals to ground. $\overline{\text{LDAC}}$, Uni/Bip B, $\overline{\text{RST}}$, and Uni/Bip A can be pulled low using the switch. By default, switch position S1.1 is open, causing $\overline{\text{LDAC}}$ to be connected to ground. Switches S1.2 and S1.4 are open to short-circuit Uni/Bip A and Uni/Bip B to ground. This configuration sets the DAC8734 to bipolar mode (default). Figure 3 shows the default settings for switch S1.

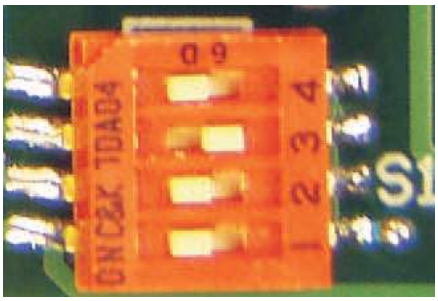

Figure 3. Default Settings for Switch S1 ($\overline{\text{LDAC}}$ Low)

Switch S2 controls the reference voltage selection for Ref B. When the switch is furthest left (position 1), the onboard 5V reference is used from the REF5050. When the switch is in the middle position (position 2), the onboard 2.5V reference is used from the REF5025. If the switch is moved to the right (position 3), Ref B is set up to use an external reference. Pins J1.18 (Ref–) and J1.20 (Ref+) are used to apply an external reference voltage.

Switch S3 controls the reference voltage selection for Ref A. The switch has the same functionality as switch S2. By default, switch S2 and switch S3 are set to use the 5V onboard reference, as Figure 4 shows.

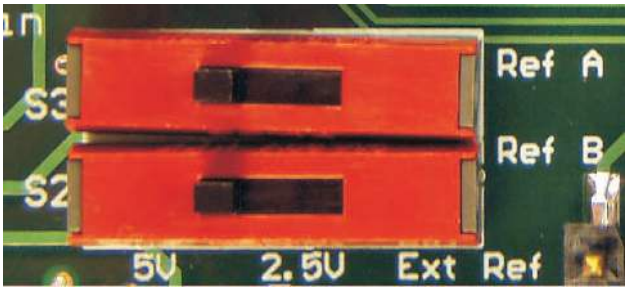

Figure 4. Default Settings for Switch S2 and S3

7 Schematics and Layout

Schematics for the DAC8734EVM are appended to this user's guide. The bill of materials is provided in Table 4.

7.1 Bill of Materials

NOTE: All components should be compliant with the European Union Restriction on Use of Hazardous Substances (RoHS) Directive. Some part numbers may be either leaded or RoHS. Verify that purchased components are RoHS-compliant. (For more information about TI's position on RoHS compliance, see the TI web site.)

Table 4. DAC8734EVM Bill of Materials[1]

Item No.	Qty	Ref Des	Description	Vendor	Mfr Part Number
1	1	N/A	Printed wiring board	Texas Instruments	6508538
2	6	C1, C6, C10, C11, C14, C15	Capacitor, Ceramic 1.0µF 16V X5R 10% 0603	TDK	C1608X5R1C105K
3	7	C2, C,3 C4, C5, C7, C8, C9	Capacitor, Ceramic 10µF 25V X5R 1206 10%	MuRata	GRM31CR61E106KA12L
4	4	C12, C13, C16, C17	Capacitor, Ceramic 10µF 10V 0603 X5R 20%	Panasonic	ECJ-1VB1A106M
5	0	D1	Do Not Install		
6	3	JP1, JP7, JP8	Header Strip, 3 pin (1x3)	Samtec	TSW-103-07-L-S
7	4	JP2, JP3, JP4, JP5	Header Strip, 2 pin (1x2)	Samtec	TSW-102-07-L-S
8	1	JP6	Header Strip, 8 pin (2x4)	Samtec	TSW-104-07-L-D
9	1	JP9	Header Strip, 6 pin (2x3)	Samtec	TSW-103-07-L-D
10	2	J1A, J2A (Top Side)	10 Pin, Dual Row, SM Header (20 Pos.)	Samtec	TSM-110-01-T-DV-P
11	0	J1B (Bottom Side)	DNI		
12	1	J2B (Bottom Side)	10 Pin, Dual Row, SM Header (20 Pos.)	Samtec	SSW-110-22-F-D-VS-K
13	1	J3A (Top Side)	5 Pin, Dual Row, SM Header (10 Pos.)	Samtec	TSM-105-01-T-DV-P
14	1	J3B (Bottom Side)[2]	5 Pin, Dual Row, SM Header (10 Pos.)	Samtec	SSW-105-22-F-D-VS-K
15	0	J4	Do Not Install		
16	5	R1, R2, R3, R4, R5	Resistor 33Ω 1/10W 5% 0603 SMD	Panasonic	ERJ-3GEYJ330V
17	6	R6, R7, R8, R9, R10, R11	Resistor 10kΩ 1/10W 5% 0603 SMD	Yageo	RC0603JR-0710KL
18	2	R12, R13	Resistor 1.0kΩ 1/10W 5% 0603 SMD	Panasonic	ERJ-3GEYJ102V
19	2	R14, R15	Resistor 1.0Ω 1/10W 5% 0603	Panasonic	ERJ-3GEYJ1R0V
20	1	R16	Resistor 200kΩ 1/10W 1% 0603 SMD	Panasonic	ERJ-3EKF2003V
21	1	S1	Switch Dip Tape (4 Pos)	C&K	TDA04H0SB1R
22	2	S2, S3	Switch Slide Ultra Mini SP3T TOP ACT	NKK	SS14MDP2
23	3	TP1, TP2, TP3	Test Point: Single .025 Pin, Red	Keystone	5000
24	2	TP4, TP5	Test Point:Single .025 Pin, Black	Keystone	5001
25	1	U1	Quad, 16-bit, High-Accuracy DAC, TQFP Package	Texas Instruments	DAC8734SPFB
26	1	U2	OPA227, Differential Operational Amplifier	Texas Instruments	OPA227UA
27	1	U3	Single output, 8V voltage regulator	Texas Instruments	TL750L08CD
28	1	U4	Precision Voltage reference 2.5V	Texas Instruments	REF5025AID
29	1	U5	Precision Voltage reference 5.0V	Texas Instruments	REF5050AID
30	8	N/A	0.100-mil Shunt, Black	Samtec	SNT-100-BK-T

(1) Manufacturer and part number for items may be substituted with electrically equivalent items.
(2) J3B parts are not shown in the schematic diagram. J3B is installed on the bottom side of the PWB opposite to J3A.

REVISION HISTORY

Changes from A Revision (February, 2010) to B Revision **Page**

- Updated Table 1; corrected descriptions and signals for J1.10 and J1.14 3
- Replaced schematic 8

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

REVISION HISTORY		
REV	ENGINEERING CHANGE NUMBER	APPROVED

IOVDD +VA -VA +5VD

C1 1uF, C2 10uF, C3 10uF, C4 10uF, C5 10uF, C6 1uF

LDAC SDO CS SCLK GPIO-0 GPIO-1 Uni/Bip Uni/Bip B RST

Serial Header Top
J2A

JP1
3POS_JUMPER

Serial Header Bottom
J2B

TP3

SDI CS SCLK

R6 10k, R7 10k, R8 10k, R9 10k, R10 10k, R11 10k

D1B D1A

R1 33, R2 33, R3 33, R4 33, R5 33

CS SCLK SDI SDO LDAC Uni/Bip A Uni/Bip B RST GPIO-0 GPIO-1

S1
DIPSWITCH-4

U1
DAC8734

IOVDD AVDD AVDD AVSS AVSS DVDD REF-A REFGND-A
DGND AGND GPIO-0 GPIO-1 REF-B REFGND-B

Vmon Ain NC NC NC NC NC NC NC RST
Vout-0 RFB1-0 RFB2-0 SGND-0
Vout-1 RFB1-1 RFB2-1 SGND-1
Vout-2 RFB1-2 RFB2-2 SGND-2
Vout-3 RFB1-3 RFB2-3 SGND-3

U2
OPA227
C7 10uF, C8 10uF, R16 200k

JP2 JP3 JP4 JP5 JP9

J1A
DAUGHTER-ANALOG
Analog to only be populated at top of board

A0(-) A1(-) A2(-) A3(-) AGND AGND AGND VCOM AGND
A0(+) A1(+) A2(+) A3(+) A4 A5 A6 A7 REF- REF+
Vout-0 Vout-1 Vout-2 Vout-3 Vmon_buf Ain ExtREF- ExtREF+

J4
HEADER-8

J1B
DAUGHTER ANALOG BOTTOM

JP6 and JP7 control the RefGND

JP7
3POS_JUMPER

JP6
3POS_JUMPER

TP4 TP5

+VA

U3
TL750L08
C9 10uF

U5
REF5050
C10 1uF, C14 1uF, C12 10uF, R14 1

U4
REF5025
C11 1uF, C15 1uF, C13 10uF, R15 1

R12 1k, R13 1k
C16 10uF, C17 10uF

S2 S3
NKK_SS14MDP2

TP1 TP2

ExtREF+

+3.3VD +1.8VD +5VA +VA -VA -5VA +5VD

J3
DAUGHTER-POWER
+VA +5VA DGND +1.8VD +3.3VD
-VA -5VA AGND VD1 +5VD

IOVDD

JP8
JPR-2X3

ENGINEER	T. Calabria		
DRAWN BY	T. Calabria		
DOCUMENT CONTROL NO	6508538	SIZE B	DATE / REV A
SHEET OF	FILE		

TEXAS INSTRUMENTS

PRECISION ANALOG PRODUCTS
HIGH-PERFORMANCE ANALOG DIVISION
SEMICONDUCTOR GROUP

5411 EAST WILLIAMS BOULEVARD, TUCSON, AZ 85711 USA

TITLE
DAC8734EVM

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EVM Warnings and Restrictions

It is important to operate this EVM within the input voltage range of –16.5V to +21V and the output voltage range of –15V to +15V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than +30° C. The EVM is designed to operate properly with certain components above +60° C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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