

# 74HC2G00-Q100; 74HCT2G00-Q100

Dual 2-input NAND gate

Rev. 2 — 20 November 2018

Product data sheet

## 1. General description

The 74HC2G00-Q100; 74HCT2G00-Q100 is a dual 2-input NAND gate. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of  $V_{CC}$ .

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

## 2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
  - Specified from -40 °C to +85 °C and from -40 °C to +125 °C
- Wide supply voltage range from 2.0 V to 6.0 V
- Input levels:
  - For 74HC2G00-Q100: CMOS level
  - For 74HCT2G00-Q100: TTL level
- Symmetrical output impedance
- High noise immunity
- Low power dissipation
- Balanced propagation delays
- ESD protection:
  - MIL-STD-883, method 3015 exceeds 2000 V
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V (C = 200 pF; R = 0 Ω)

## 3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC2G00DP-Q100	-40 °C to +125 °C	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm	SOT505-2
74HCT2G00DP-Q100				
74HC2G00DC-Q100	-40 °C to +125 °C	VSSOP8	plastic very thin shrink small outline package; 8 leads; body width 2.3 mm	SOT765-1
74HCT2G00DC-Q100				

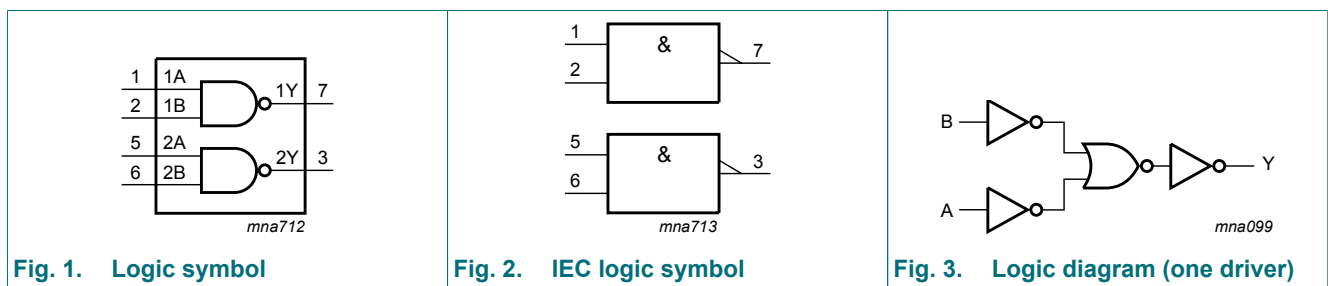
## 4. Marking

Table 2. Marking code

Type number	Marking code <sup>[1]</sup>
74HC2G00DP-Q100	H00
74HCT2G00DP-Q100	T00
74HC2G00DC-Q100	H00
74HCT2G00DC-Q100	T00

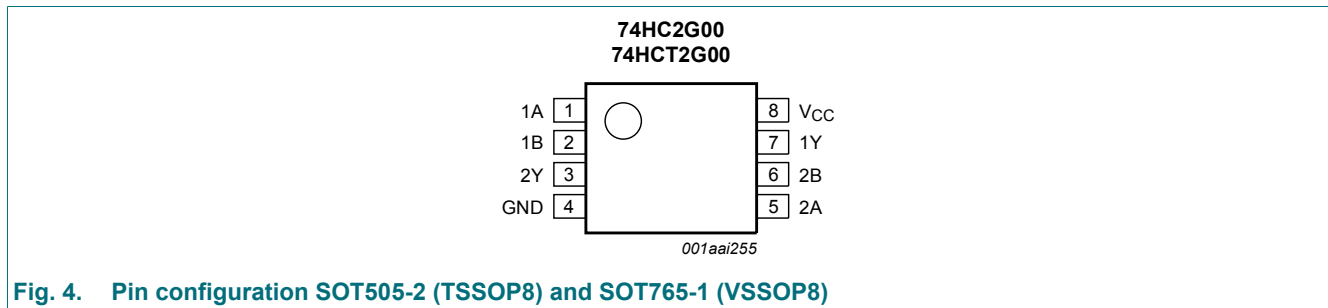
[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

## 5. Functional diagram



## 6. Pinning information

### 6.1. Pinning



### 6.2. Pin description

Table 3. Pin description

Symbol	Pin	Description
1A, 2A	1, 5	data input
1B, 2B	2, 6	data input
GND	4	ground (0 V)
1Y, 2Y	7, 3	data output
V <sub>CC</sub>	8	supply voltage

## 7. Functional description

**Table 4. Function table**

*H = HIGH voltage level; L = LOW voltage level.*

Input		Output
nA	nB	nY
L	L	H
L	H	H
H	L	H
H	H	L

## 8. Limiting values

**Table 5. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).*

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+7.0	V
$I_{IK}$	input clamping current	$V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$	[1]	-	±20 mA
$I_{OK}$	output clamping current	$V_O < -0.5\text{ V}$ or $V_O > V_{CC} + 0.5\text{ V}$	[1]	-	±20 mA
$I_O$	output current	$V_O = -0.5\text{ V}$ to $(V_{CC} + 0.5\text{ V})$	[1]	-	25 mA
$I_{CC}$	supply current		[1]	-	50 mA
$I_{GND}$	ground current		[1]	-50	- mA
$T_{stg}$	storage temperature		-65	+150	°C
$P_D$	dynamic power dissipation	$T_{amb} = -40\text{ °C}$ to $+125\text{ °C}$	[2]	-	300 mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For TSSOP8 package: above 55 °C the value of  $P_{tot}$  derates linearly with 2.5 mW/K.  
For VSSOP8 package: above 110 °C the value of  $P_{tot}$  derates linearly with 8 mW/K.

## 9. Recommended operating conditions

**Table 6. Recommended operating conditions**

*Voltages are referenced to GND (ground = 0 V).*

Symbol	Parameter	Conditions	74HC2G00-Q100			74HCT2G00-Q100			Unit
			Min	Typ	Max	Min	Typ	Max	
$V_{CC}$	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
$V_I$	input voltage		0	-	$V_{CC}$	0	-	$V_{CC}$	V
$V_O$	output voltage		0	-	$V_{CC}$	0	-	$V_{CC}$	V
$T_{amb}$	ambient temperature		-40	+25	+125	-40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 2.0\text{ V}$	-	-	625	-	-	-	ns/V
		$V_{CC} = 4.5\text{ V}$	-	1.67	139	-	1.67	139	ns/V
		$V_{CC} = 6.0\text{ V}$	-	-	83	-	-	-	ns/V

## 10. Static characteristics

**Table 7. Static characteristics**

Voltages are referenced to GND (ground = 0 V). All typical values are measured at  $T_{amb} = 25\text{ }^{\circ}\text{C}$ .

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	
<b>74HC2G00-Q100</b>								
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 2.0 V	1.5	1.2	-	1.5	-	V
		V <sub>CC</sub> = 4.5 V	3.15	2.4	-	3.15	-	V
		V <sub>CC</sub> = 6.0 V	4.2	3.2	-	4.2	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 2.0 V	-	0.8	0.5	-	0.5	V
		V <sub>CC</sub> = 4.5 V	-	2.1	1.35	-	1.35	V
		V <sub>CC</sub> = 6.0 V	-	2.8	1.8	-	1.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>						
		I <sub>O</sub> = -20 μA; V <sub>CC</sub> = 2.0 V	1.9	2.0	-	1.9	-	V
		I <sub>O</sub> = -20 μA; V <sub>CC</sub> = 4.5 V	4.4	4.5	-	4.4	-	V
		I <sub>O</sub> = -20 μA; V <sub>CC</sub> = 6.0 V	5.9	6.0	-	5.9	-	V
		I <sub>O</sub> = -4.0 mA; V <sub>CC</sub> = 4.5 V	4.13	4.32	-	3.7	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>						
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 2.0 V	-	0	0.1	-	0.1	V
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 4.5 V	-	0	0.1	-	0.1	V
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 6.0 V	-	0	0.1	-	0.1	V
		I <sub>O</sub> = 4.0 mA; V <sub>CC</sub> = 4.5 V	-	0.15	0.33	-	0.4	V
I <sub>I</sub>	input leakage current	I <sub>O</sub> = 5.2 mA; V <sub>CC</sub> = 6.0 V	5.63	5.81	-	5.2	-	V
		V <sub>I</sub> = V <sub>CC</sub> or GND; V <sub>CC</sub> = 6.0 V	-	-	±1.0	-	±1.0	μA
I <sub>CC</sub>	supply current	per input pin; V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 6.0 V	-	-	10	-	20	μA
C <sub>I</sub>	input capacitance		-	1.5	-	-	-	pF
<b>74HCT2G00-Q100</b>								
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>						
		I <sub>O</sub> = -20 μA; V <sub>CC</sub> = 4.5 V	4.4	4.5	-	4.4	-	V
		I <sub>O</sub> = -4.0 mA; V <sub>CC</sub> = 4.5 V	4.13	4.32	-	3.7	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>						
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 4.5 V	-	0	0.1	-	0.1	V
		I <sub>O</sub> = 4.0 mA; V <sub>CC</sub> = 4.5 V	-	0.15	0.33	-	0.4	V
I <sub>I</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND; V <sub>CC</sub> = 5.5 V	-	-	±1.0	-	±1.0	μA
I <sub>CC</sub>	supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 5.5 V	-	-	10	-	20	μA
ΔI <sub>CC</sub>	additional supply current	per input; V <sub>CC</sub> = 4.5 V to 5.5 V; V <sub>I</sub> = V <sub>CC</sub> - 2.1 V; I <sub>O</sub> = 0 A	-	-	375	-	410	μA
C <sub>I</sub>	input capacitance		-	1.5	-	-	-	pF

## 11. Dynamic characteristics

**Table 8. Dynamic characteristics**

Voltages are referenced to GND (ground = 0 V); all typical values are measured at  $T_{amb} = 25\text{ °C}$ ; for test circuit see Fig. 6.

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	
<b>74HC2G00-Q100</b>								
$t_{pd}$	propagation delay	nA and nB to nY; see Fig. 5 [1]						
		$V_{CC} = 2.0\text{ V}$	-	25	95	-	110	ns
		$V_{CC} = 4.5\text{ V}$	-	9	19	-	22	ns
		$V_{CC} = 6.0\text{ V}$	-	7	16	-	20	ns
$t_t$	transition time	see Fig. 5 [2]						
		$V_{CC} = 2.0\text{ V}$	-	18	95	-	125	ns
		$V_{CC} = 4.5\text{ V}$	-	6	19	-	25	ns
		$V_{CC} = 6.0\text{ V}$	-	5	16	-	20	ns
$C_{PD}$	power dissipation capacitance	$V_I = \text{GND to } V_{CC}$ [3]	-	10	-	-	-	pF
<b>74HCT2G00-Q100</b>								
$t_{pd}$	propagation delay	nA and nB to nY; see Fig. 5 [1]						
		$V_{CC} = 4.5\text{ V}$	-	12	24	-	29	ns
$t_t$	transition time	$V_{CC} = 4.5\text{ V}$ ; see Fig. 5 [2]	-	6	19	-	22	ns
$C_{PD}$	power dissipation capacitance	$V_I = \text{GND to } V_{CC} - 1.5\text{ V}$ [3]	-	10	-	-	-	pF

[1]  $t_{pd}$  is the same as  $t_{PLH}$  and  $t_{PHL}$ .

[2]  $t_t$  is the same as  $t_{TLH}$  and  $t_{THL}$ .

[3]  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

$f_i$  = input frequency in MHz;

$f_o$  = output frequency in MHz;

$C_L$  = output load capacitance in pF;

$V_{CC}$  = supply voltage in V;

$N$  = number of inputs switching;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$  = sum of outputs.

11.1. Waveforms and test circuit

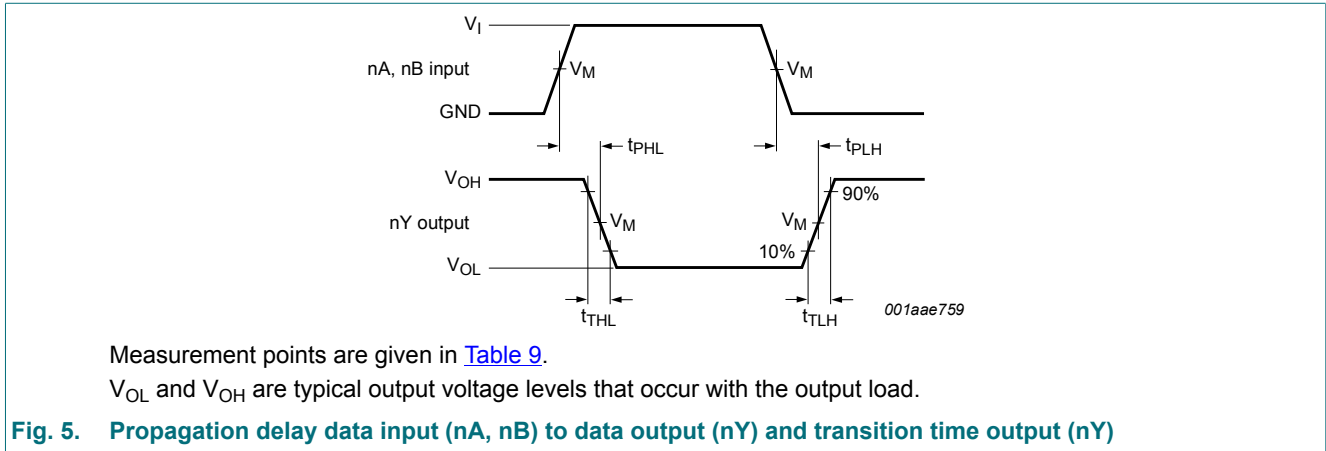


Table 9. Measurement points

Type	Input	Output
	$V_M$	$V_M$
74HC2G00-Q100	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
74HCT2G00-Q100	1.3 V	1.3 V

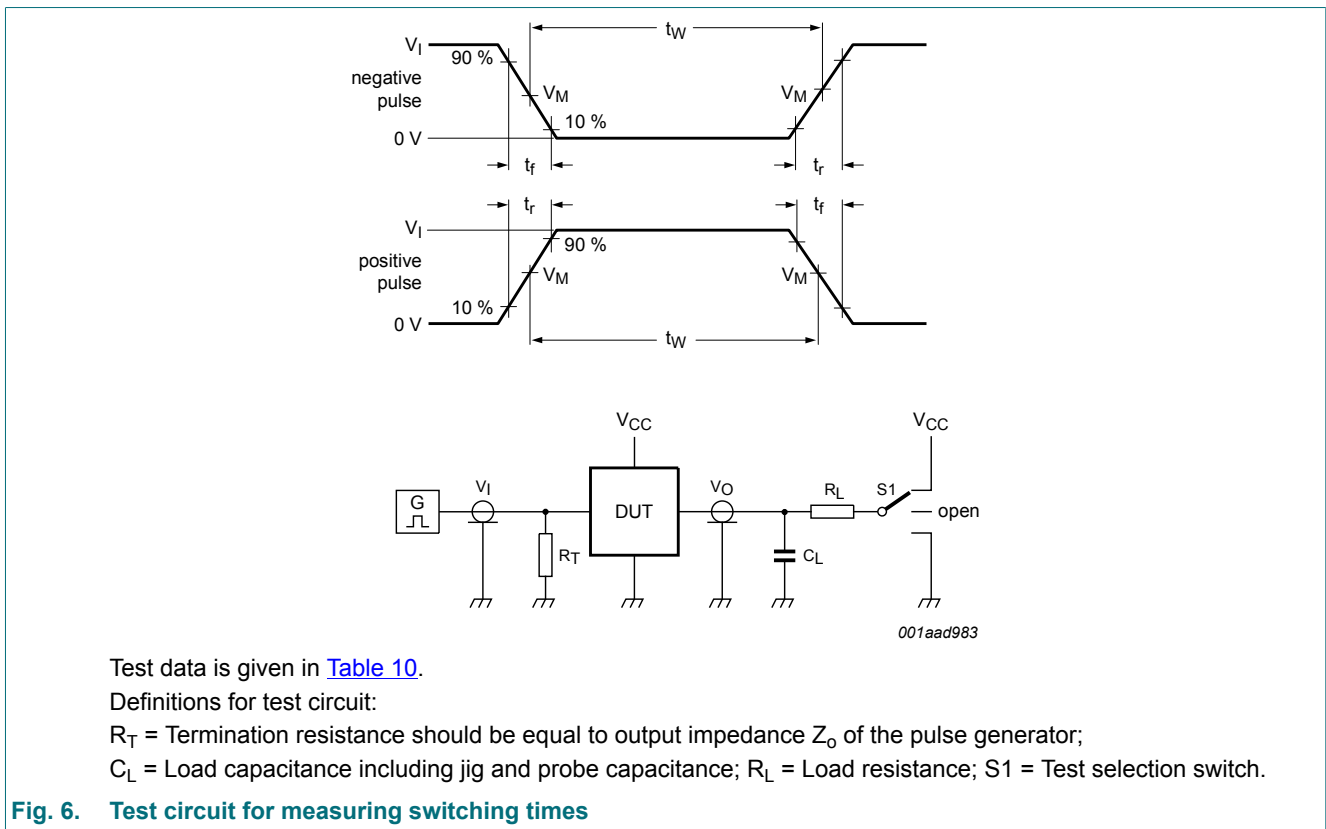
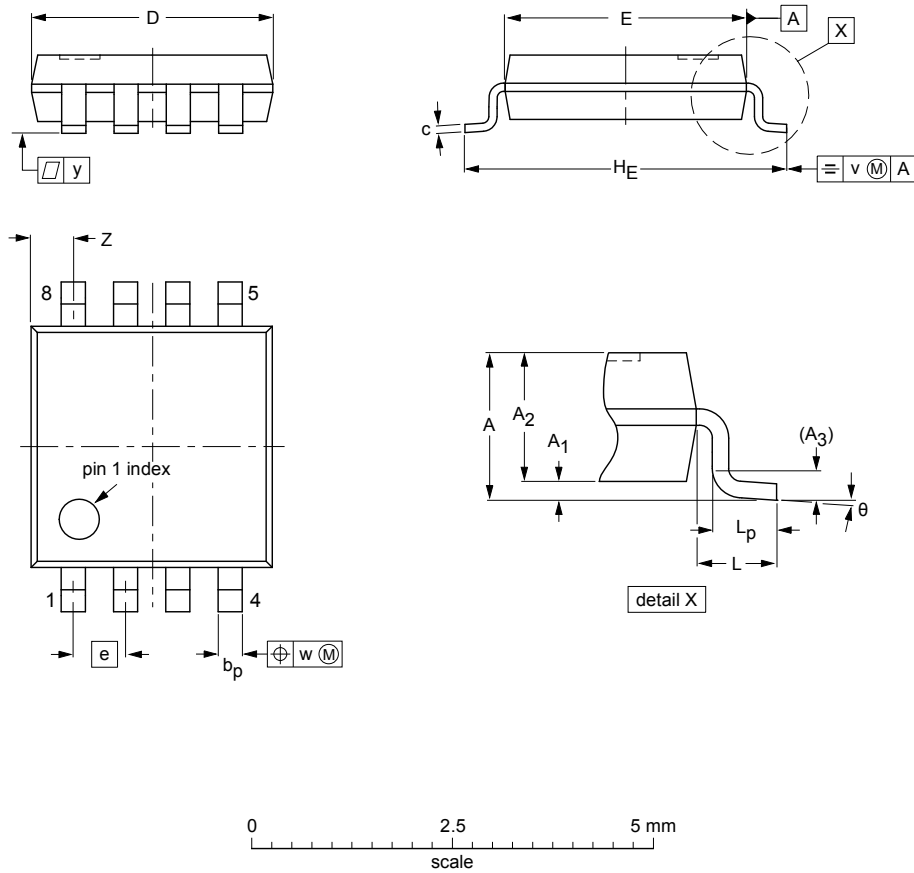


Table 10. Test data

Type	Input		Load		S1 position
	$V_I$	$t_r, t_f$	$C_L$	$R_L$	$t_{PHL}, t_{PLH}$
74HC2G00-Q100	$V_{CC}$	$\leq 6$ ns	50 pF	1 k $\Omega$	open
74HCT2G00-Q100	3 V	$\leq 6$ ns	50 pF	1 k $\Omega$	open

## 12. Package outline

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm SOT505-2



**DIMENSIONS** (mm are the original dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	v	w	y	Z <sup>(1)</sup>	θ
mm	1.1	0.15 0.00	0.95 0.75	0.25	0.38 0.22	0.18 0.08	3.1 2.9	3.1 2.9	0.65	4.1 3.9	0.5	0.47 0.33	0.2	0.13	0.1	0.70 0.35	8° 0°

**Note**

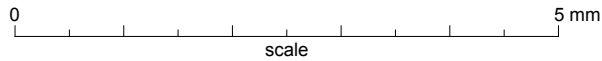
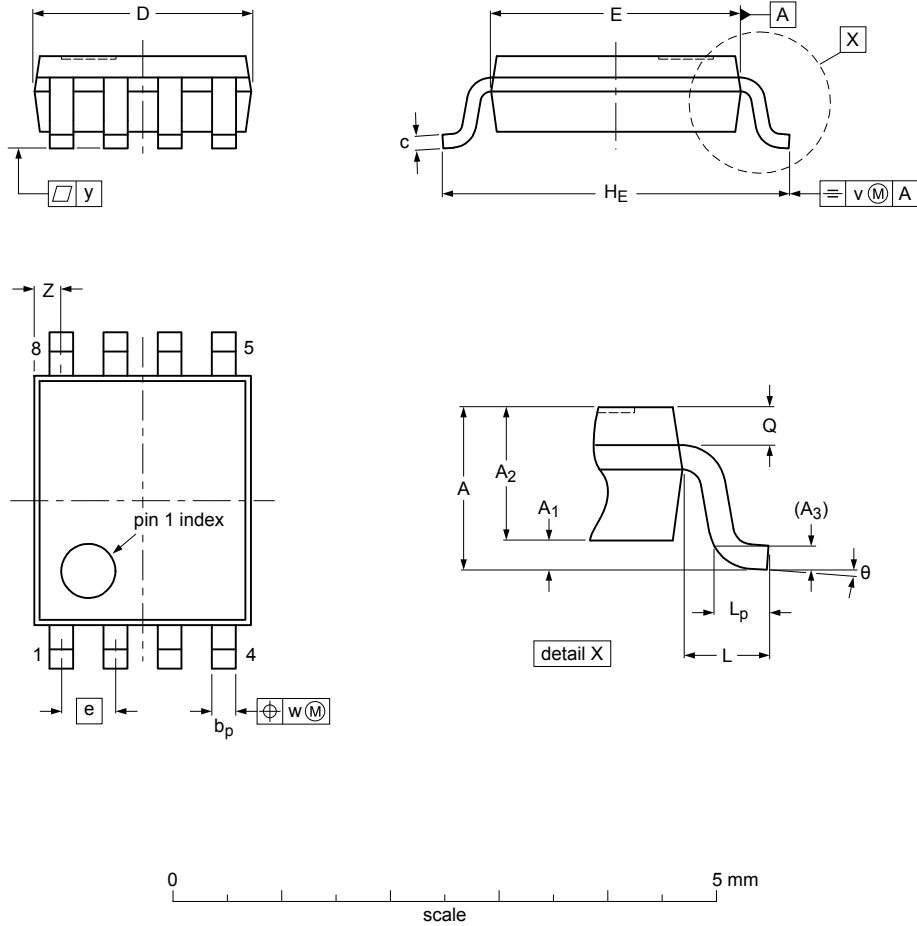
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT505-2		---				02-01-16

**Fig. 7. Package outline SOT505-2 (TSSOP8)**

VSSOP8: plastic very thin shrink small outline package; 8 leads; body width 2.3 mm

SOT765-1



Dimensions (mm are the original dimensions)

Unit	A <sup>A</sup> max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(2)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
max		0.15	0.85		0.27	0.23	2.1	2.4		3.2		0.40	0.21				0.4	8°
mm	nom	1		0.12					0.5		0.4			0.2	0.08	0.1		
	min		0.00	0.60	0.17	0.08	1.9	2.2		3.0		0.15	0.19				0.1	0°

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

sot765-1\_po

Outline version	References			European projection	Issue date
	IEC	JEDEC	JEITA		
SOT765-1		MO-187			07-06-02-16-05-31

Fig. 8. Package outline SOT765-1 (VSSOP8)



## 13. Abbreviations

**Table 11. Abbreviations**

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
ESD	ElectroStatic Discharge
HBM	Human Body Model
MIL	Military
MM	Machine Model
TTL	Transistor-Transistor Logic

## 14. Revision history

**Table 12. Revision history**

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT2G00_Q100 v.2	20181120	Product data sheet	-	74HC_HCT2G00_Q100 v.1
Modifications:	<ul style="list-style-type: none"><li>The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li><li>Legal texts have been adapted to the new company name where appropriate.</li></ul>			
74HC_HCT2G00_Q100 v.1	20131107	Product data sheet	-	-

## 15. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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