LOW VOLTAGE PLL CLOCK DRIVER

IDT5V9351

PRODUCT DISCONTINUATION NOTICE - LAST TIME BUY EXPIRES OCTOBER 28, 2014

FEATURES:

- Fully integrated PLL
- Output frequency up to 200MHz
- 2.5V and 3.3V Compatible
- Compatible with PowerPC™, Intel, and high performance RISC microprocessors
- Output frequency configurable
- Cycle-to-cycle jitter max. 22ps RMS
- Compatible with MPC9351
- Available in TQFP package
- Use replacement part 87951AYI-147LF

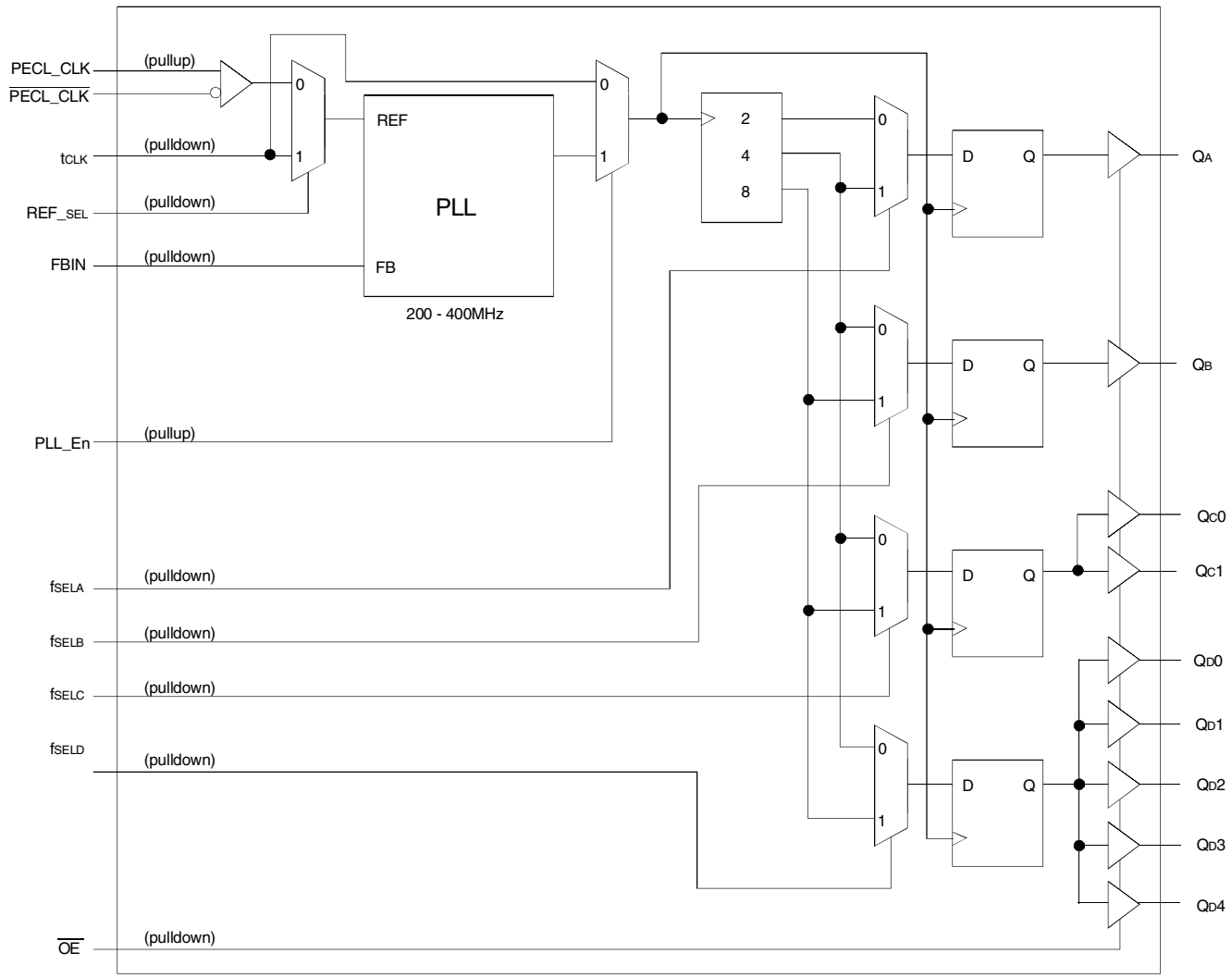
DESCRIPTION:

The IDT5V9351 is a high performance, zero delay, low skew, phase-lock loop (PLL) clock driver. It has four banks of configurable outputs. The IDT5V9351 uses a differential PECL reference input and an external feedback input. These features allow the IDT5V9351 to be used as a zero delay, low skew fan-out buffer. REF_SEL allows selection between PECL input or TCLK, a CMOS clock driver input.

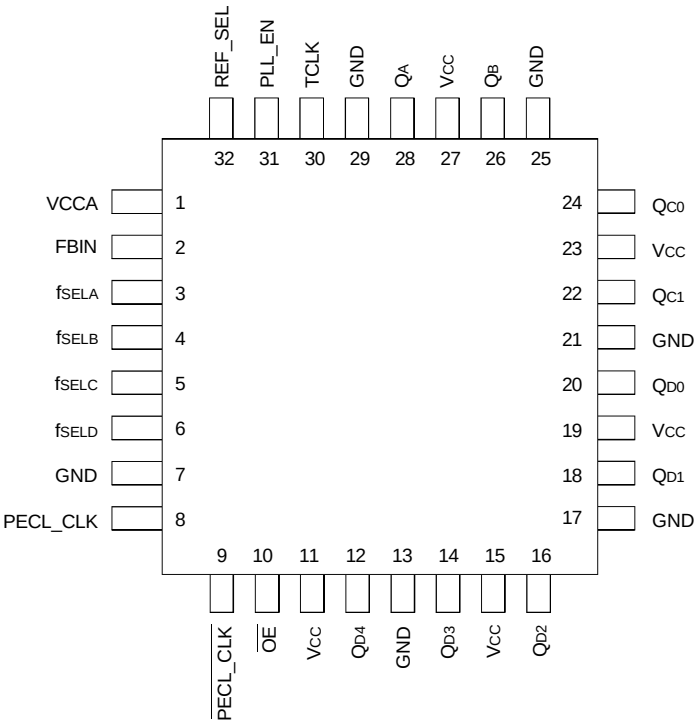
If PLL_EN is set to low and REF_SEL to high, it will bypass the PLL. By doing so, the IDT5V9351 will be in clock buffer mode. Any clock applied to TCLK will be divided down to four output banks.

When PLL_EN is set high, PLL is enabled. Any clock applied to TCLK will be clocked in both phase and frequency to FBIN. PECL clock is activated by setting REF_SEL to low.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



TQFP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Description	Max.	Unit
V_{CC}	Supply Voltage	–0.3 to +4.6	V
V_I	Input Voltage	–0.3 to V_{CC}+0.3	V
V_O	DC Output Voltage	–0.3 to V_{CC}+0.3	V
I_{IN}	Input Current	±20	mA
I_O	DC Output Current	±50	mA
T_{STG}	Storage Temperature	–55 to +150	°C

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

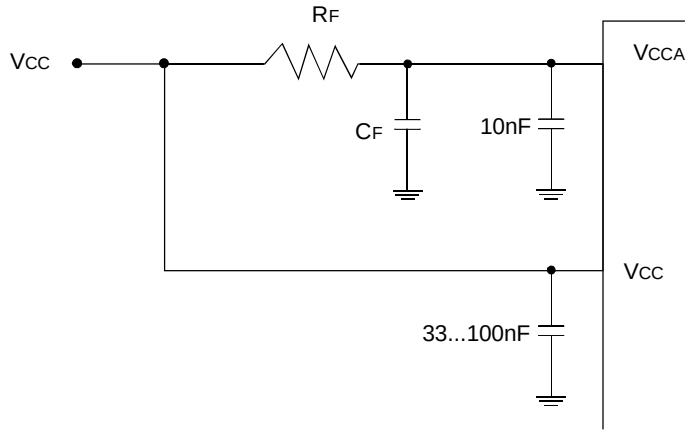
CAPACITANCE (T_A = +25°C, F = 1.0MHz)

Symbol	Parameter	Min.	Typ.	Max.	Unit
C_{IN}	Input Capacitance	—	4	—	pF
C_{PD}	Power Dissipation Capacitance	—	10	—	pF

GENERAL SPECIFICATIONS

Symbol	Description	Min.	Typ.	Max.	Unit
V_{TT}	Output Termination Voltage		V_{CC}/2		V
HBM	ESD (Human Body Model)	2000			V
LU	Latch-Up Immunity	200			mA

LOGIC DIAGRAM(1,2)



NOTES:
1. IDT5V9351 requires an external RC filter for the analog power supply pin V_{CCA}.
2. For V_{CC} = 2.5V, R_F = 9-10Ω, C_F = 22µF.
   For V_{CC} = 3.3V, R_F = 5-15Ω, C_F = 22µF.

PIN DESCRIPTION

Terminal			
Name	No.	Type	Description
PECL-CLK $\overline{\text{PECL-CLK}}$	8, 9	I	Differential clock reference, LOW voltage positive ECL input
TCLK	30	I	Single-ended reference clock signal or test clock
FBIN	2	I	Feedback signal input
REF_SEL	32	I	Reference clock input
$f_{SEL(D:A)}$	3, 4, 5, 6	I	Frequency control pin
$\overline{OE}$	10	I	Output enable/disable
Q_A	28	O	Bank A clock output
Q_B	26	O	Bank B clock output
$Q_{C(1:0)}$	22, 24	O	Bank C clock output
$Q_{D(4:0)}$	12, 14, 16, 18, 20	O	Bank D clock output
V_{CCA}	1	PWR	Positive power supply for PLL
V_{CC}	11, 15, 19, 23, 27	PWR	Positive power supply for I/O and core
GND	7, 13, 17, 21, 25, 29	Ground	Negative power supply
PLL_EN	31	I	PLL enable input. When set HIGH, PLL is enabled. When set LOW, PLL is disabled.

FUNCTIONALITY

Control	Default	0	1
REF_SEL	0	Selects PECL_CLK as reference clock	Selects TCLK as reference clock
PLL_EN	1	Test mode with PLL Disabled	PLL Enabled
OE	0	Outputs enabled	Outputs disabled
FSELA	0	$Q_A = V_{CO} \div 2$	$Q_A = V_{CO} \div 4$
FSELB	0	$Q_B = V_{CO} \div 4$	$Q_B = V_{CO} \div 8$
FSELC	0	$Q_C = V_{CO} \div 4$	$Q_C = V_{CO} \div 8$
FSELD	0	$Q_D = V_{CO} \div 4$	$Q_D = V_{CO} \div 8$

NOTE:
1. Output frequency relationship with respect to input reference frequency CLK. QC1 is connected to FBIN.

FUNCTION TABLE(1)

INPUTS				OUTPUTS			
f_{SELA}	f_{SELB}	f_{SELC}	f_{SELD}	Q_A	Q_B	Q_C	Q_D
0	0	0	0	2 * CLK	CLK	CLK	CLK
0	0	0	1	2 * CLK	CLK	CLK	CLK ÷ 2
0	0	1	0	4 * CLK	2 * CLK	CLK	2 * CLK
0	0	1	1	4 * CLK	2 * CLK	CLK	CLK
0	1	0	0	2 * CLK	CLK ÷ 2	CLK	CLK
0	1	0	1	2 * CLK	CLK ÷ 2	CLK	CLK ÷ 2
0	1	1	0	4 * CLK	CLK	CLK	2 * CLK
0	1	1	1	4 * CLK	CLK	CLK	CLK
1	0	0	0	CLK	CLK	CLK	CLK
1	0	0	1	CLK	CLK	CLK	CLK ÷ 2
1	0	1	0	2 * CLK	2 * CLK	CLK	2 * CLK
1	0	1	1	2 * CLK	2 * CLK	CLK	CLK
1	1	0	0	CLK	CLK ÷ 2	CLK	CLK
1	1	0	1	CLK	CLK ÷ 2	CLK	CLK ÷ 2
1	1	1	0	2 * CLK	CLK	CLK	2 * CLK
1	1	1	1	2 * CLK	CLK	CLK	CLK

NOTE:
1. Output frequency relationship with respect to input reference frequency CLK. QC1 is connected to FBIN.

DC ELECTRICAL CHARACTERISTICS

T_A = -40°C to +85°C, V_{CC} = 3.3V ± 5%

Symbol	Parameter	Test Conditions	Min.	Typ.	Max	Unit
V_{IH}	Input HIGH Voltage	LVCMOS Inputs	2	—	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage	LVCMOS Inputs	—	—	0.8	V
V_{PP}	Peak-to-Peak Input Voltage	PECL_CLK	250	—	—	mV
V_{CMR}	Common Mode(1)	PECL_CLK	1	—	V_{CC} - 0.6	V
V_{OH}	Output HIGH Voltage(2)	I_{OH} = -24mA	2.4	—	—	V
V_{OL}	Output LOW Voltage(2)	I_{OL} = 24mA	—	—	0.55	V
		I_{OL} = 12mA	—	—	0.3	
Z_{OUT}	Output Impedance		—	14 - 17	—	Ω
I_{IN}	Input Leakage Current		—	—	±150	µA
I_{CC}	Maximum Quiescent Supply Current	All V_{CC} Pins	—	—	1	mA
I_{CCPLL}	Maximum PLL Supply Current	V_{CCA} Only	—	3	5	mA

NOTES:
1. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} range and the input swing lies within the V_{PP} (DC) specification.
2. The IDT5V9351 outputs can drive series or paralell terminated 50Ω (or 50Ω to V_{CC}/2) transmission lines on the incident edge.

PLL INPUT REFERENCE CHARACTERISTICS

V_{CC} = 3.3V ± 5%, T_A = -40°C to +85°C

Symbol	Parameter		Min.	Max	Unit
t_R, t_F	TCLK Input Rise/Fall Levels, 0.8V to 2V		—	1	ns
f_{REF}	Reference Input Frequency[1]	÷2 feedback	100	200	MHz
		÷4 feedback	50	100	
		÷8 feedback	25	50	
	Static Test Mode		0	300	
$f_{REF}DC$	Reference Input Duty Cycle		25	75	%

NOTE:

1. Maximum and minimum input reference is limited by the VCO lock range and the feedback divider for the TCLK or PECL_CLK inputs.

AC ELECTRICAL CHARACTERISTICS[1]

T_A = -40°C to +85°C, V_{CC} = 3.3V ± 5%

Symbol	Parameter	Conditions		Min.	Typ.	Max	Unit
t_R, t_F	Output Rise/Fall Time	0.55V to 2.4V		0.1	—	1	ns
V_{PP}	Peak-to-Peak Input Voltage	LVPECL		500	—	1000	mV
V_{CMR}	Common Mode Range[2]	LVPECL		1.2	—	V_{CC} - 0.9	V
t_{PW}	Output Duty Cycle	100-200 MHz		45	50	55	%
		50-100 MHz		47.5	50	52.5	
		25-50 MHz		48.75	50	51.75	
$t_{SK(O)}$	Output to Output Skew			—	—	150	ps
f_{VCO}	PLL VCO Lock Range			200	—	400	MHz
f_{MAX}	Maximum Output Frequency	÷2 output		100	—	200	MHz
		÷4 output		50	—	100	
		÷8 output		25	—	50	
t_{PD}	Propagation Delay (Static Phase Offset)	TCLK to FBIN		-50	—	150	ps
		PECL_CLK to FBIN		25	—	325	
t_{PLZ}, t_{PHZ}	Output Disable Time			—	—	10	ns
t_{PZL}, t_{PZH}	Output Enable Time			—	—	10	ns
BW	PLL Closed Loop Bandwidth	÷2 feedback	-3db point of	—	9 - 20	—	MHz
		÷4 feedback	PLL transfer	—	3 - 9.5	—	
		÷8 feedback	characteristic	—	1.2 - 2.1	—	
t_J	Cycle-to-Cycle Jitter ÷4 feedback (Single Output Frequency Configuration)	RMS Value		—	10	22	ps
$t_{JIT(PER)}$	Period Jitter ÷4 feedback (Single Output Frequency Configuration)	RMS Value		—	8	15	ps
$t_{JIT(\phi)}$	I/O Phase Jitter	RMS Value		—	4 - 17	—	ps
t_{LOCK}	Maximum PLL Lock Time			—	—	1	ms

NOTES:

1. AC Characteristics apply for parallel output termination of 50Ω to V_{TT}.
2. $V_{CMR(AC)}$ is the crosspoint of the differential input signal. Normal AC operation is obtained when the crosspoint is within the V_{CMR} range and the input swing lies within $V_{PP(AC)}$ specifications.

DC ELECTRICAL CHARACTERISTICS

T_A = -40°C to +85°C, V_{CC} = 2.5V ± 5%

Symbol	Parameter	Test Conditions	Min.	Typ.	Max	Unit
V_{IH}	Input HIGH Voltage	LVCMOS Inputs	1.7	—	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage	LVCMOS Inputs	—	—	0.7	V
V_{PP}	Peak-to-Peak Input Voltage	PECL_CLK	250	—	—	mV
V_{CMR}	Common Mode(1)	PECL_CLK	1	—	V_{CC} - 0.6	V
V_{OH}	Output HIGH Voltage(2)	I_{OH} = -15mA	1.8	—	—	V
V_{OL}	Output LOW Voltage(2)	I_{OL} = 15mA	—	—	0.6	V
I_{IN}	Input Current		—	—	±150	µA
C_{IN}	Input Capacitance		—	4	—	pF
Z_{OUT}	Output Impedance		—	17 - 20	—	Ω
C_{PD}	Power Dissipation Capacitance		—	10	—	pF
I_{CC}	Maximum Quiescent Supply Current	All V_{CC} Pins	—	—	1	mA
I_{CCPLL}	Maximum PLL Supply Current	V_{CCA} Only	—	3	5	mA

NOTES:

1. V_{CMR} is the difference from the most positive side of the differential input signal. Normal operation is obtained when the HIGH input is within the V_{CMR} range and the input swing lies within the V_{PP} specification.
2. The IDT5V9351 outputs can drive series or paralell terminated 50Ω (or 50Ω to V_{CC}/2) transmission lines on the incident edge.

PLL INPUT REFERENCE CHARACTERISTICS

V_{CC} = 2.5V ± 5%, T_A = -40°C to +85°C

Symbol	Parameter		Min.	Max	Unit
t_R, t_F	TCLK Input Rise/Fall Levels, 0.7V to 1.7V		—	1	ns
f_{REF}	Reference Input Frequency(1)	÷2 feedback	100	200	MHz
		÷4 feedback	50	100	
		÷8 feedback	25	50	
f_{REF}DC	Reference Input Duty Cycle		25	75	%

NOTE:

1. Maximum and minimum input reference is limited by the VCO lock range and the feedback divider for the TCLK or PECL_CLK inputs.

AC ELECTRICAL CHARACTERISTICS(1)

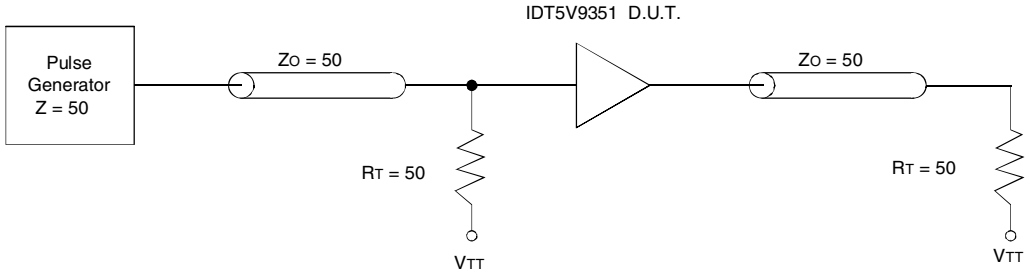
T_A = -40°C to +85°C, V_{CC} = 2.5V ± 5%

Symbol	Parameter	Conditions		Min.	Typ.	Max	Unit
t_R, t_F	Output Rise/Fall Time	0.6V to 1.8V		0.1	—	1	ns
V_{PP}	Peak-to-Peak Input Voltage	LVPECL		500	—	1000	mV
V_{CMR}	Common Mode Range(2)	LVPECL		1.2	—	V_{CC} - 0.6	V
t_{PW}	Output Duty Cycle	100-200 MHz		45	50	55	%
		50-100 MHz		47.5	50	52.5	
		25-50 MHz		48.75	50	51.75	
$t_{SK(O)}$	Output to Output Skew			—	—	150	ps
f_{VCO}	PLL VCO Lock Range			200	—	400	MHz
f_{MAX}	Maximum Output Frequency	÷2 output		100	—	200	MHz
		÷4 output		50	—	100	
		÷8 output		25	—	50	
t_{PD}	Input to FBIN Delay	TCLK to FBIN		-100	—	100	ps
		PECL_CLK to FBIN		0	—	300	
t_{PLZ}, t_{PHZ}	Output Disable Time			—	—	12	ns
t_{PZL}, t_{PZH}	Output Enable Time			—	—	12	ns
BW	PLL Closed Loop Bandwidth	÷2 feedback	-3db point of	—	4 - 15	—	MHz
		÷4 feedback	PLL to transfer	—	2 - 7	—	
		÷8 feedback	characteristic	—	0.7 - 2	—	
t_J	Cycle-to-Cycle Jitter ÷4 feedback (Single Output Frequency Configuration)	RMS Value		—	10	22	ps
$t_{JIT(PER)}$	Period Jitter ÷4 feedback (Single Output Frequency Configuration)	RMS Value		—	8	15	ps
$t_{JIT(\phi)}$	I/O Phase Jitter	RMS Value		—	6 - 25	—	ps
t_{LOCK}	Maximum PLL Lock Time			—	—	1	ms

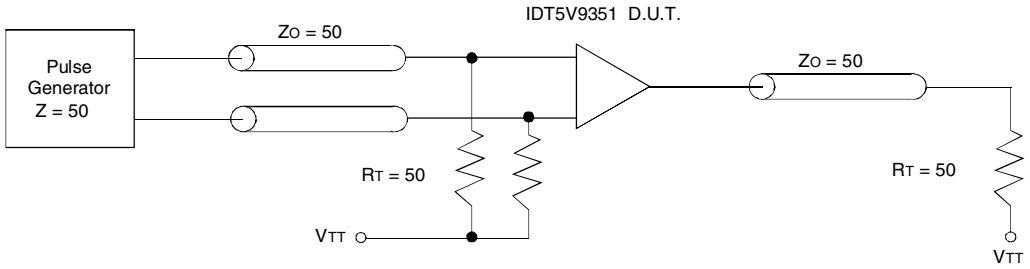
NOTES:

1. AC Characteristics apply for parallel output termination of 50Ω to V_{TT}.
2. $V_{CMR(AC)}$ is the crosspoint of the differential input signal. Normal AC operation is obtained when the crosspoint is within the V_{CMR} range and the input swing lies within $V_{PP(AC)}$ specifications.

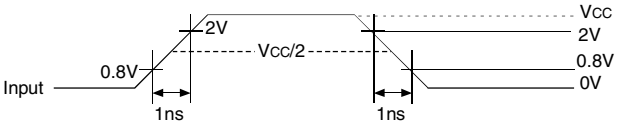
TEST CIRCUITS AND WAVEFORMS



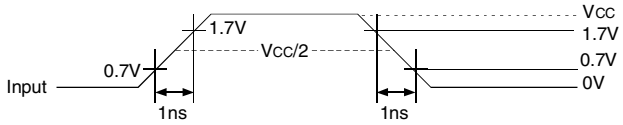
TCLK AC Test Reference for VCC = 2.5V and VCC = 3.3V



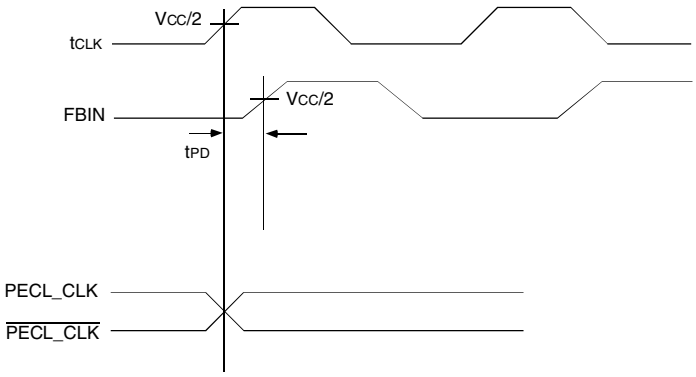
PECL_CLK AC Test Reference



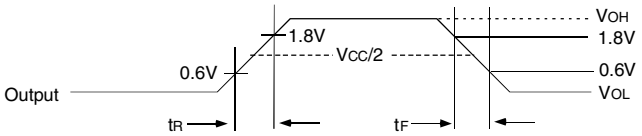
Input Characteristics for 3.3V



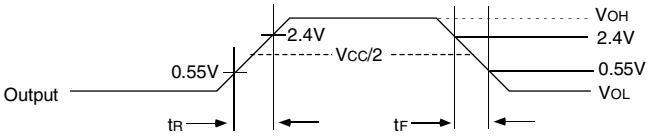
Input Characteristics for 2.5V



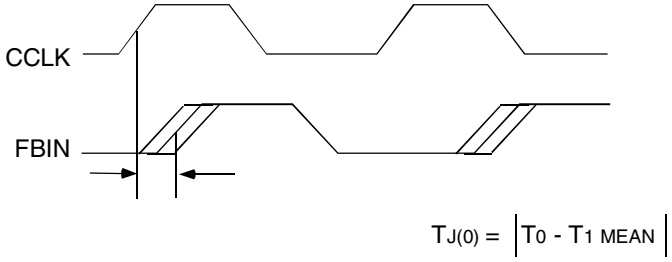
Prop Delay



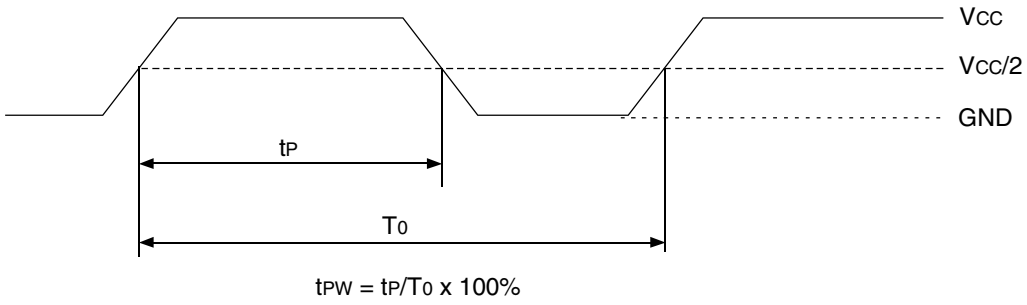
Output Test Conditions for VCC = 2.5V ± 5%



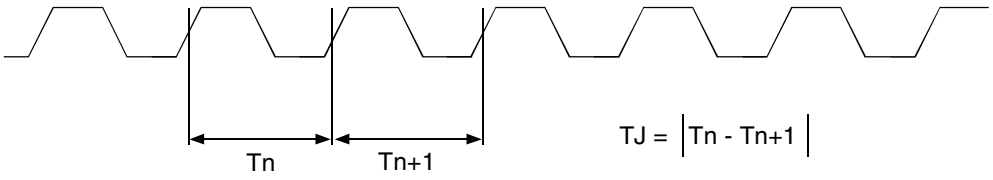
Output Test Conditions for VCC = 3.3V ± 5%



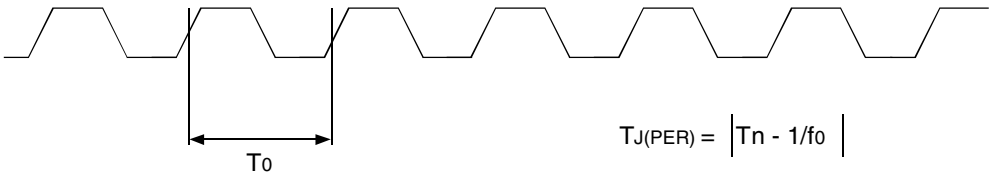
I/O Jitter



Output Duty Cycle

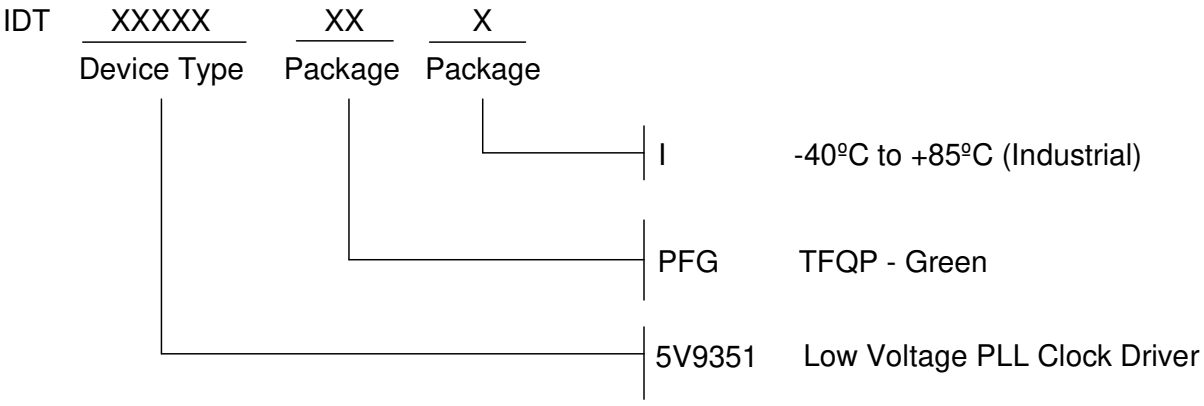


Cycle-to-Cycle Jitter



Period Jitter

ORDERING INFORMATION



REVISION HISTORY

Rev	Table	Page	Discription of Change	Date
A		1	NRND - Not Recommended for New Designs	5/20/13
A		1	Product Discontinuation Notice - Last Time Buy Expires October 28, 2014 - PDN# CQ-13-02	12/19/13

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