Angle Sensor

GMR-Based Angle Sensor

TLI5012B E1000

Data Sheet

Rev. 1.1, 2015-09

Sense & Control

Revision History	
Page or Item	**Subjects (major changes since previous revision)**
Rev. 1.1, 2015-09	
Chapter 1.4	Disclaimer modified

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Last Trademarks Update 2011-11-11

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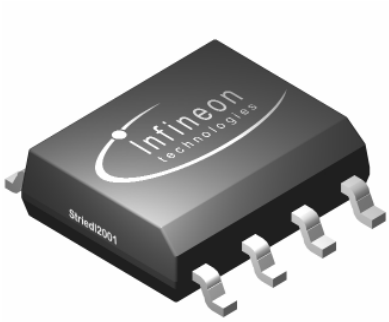

Figure 1-1 PG-DSO-8 package

1.1 Overview

The TLI5012B E1000 is a 360° angle sensor that detects the orientation of a magnetic field. This is achieved by measuring sine and cosine angle components with monolithic integrated Giant Magneto Resistance (iGMR) elements. These raw signals (sine and cosine) are digitally processed internally to calculate the angle orientation of the magnetic field (magnet).

The TLI5012B E1000 is a pre-calibrated sensor. The calibration parameters are stored in laser fuses. At start-up the values of the fuses are written into flip-flops, where these values can be changed by the application-specific parameters. Further precision of the angle measurement over a wide temperature range and a long lifetime are improved with the internal autocalibration algorithm.

Data communications are accomplished with a bi-directional Synchronous Serial Communication (SSC) that is SPI-compatible. The sensor configuration is stored in registers, which are accessible by the SSC interface. Additionally the TLI5012B E1000 has Incremental Interface (IIF),

Table 1-1 Derivate Ordering codes

Product Type	Marking	Ordering Code	Package
TLI5012B E1000	I12B1000	SP001415550	PG-DSO-8

1.2 Features

The TLI5012B E1000 has the following features and pre-configuration. The configuration can be changed via SSC interface.

- **G**iant **M**agneto **R**esistance (GMR)-based principle.
- Integrated magnetic field sensing for angle measurement.
- 360° angle measurement with revolution counter and angle speed measurement.
- Max. 1.9° angle error over lifetime and temperature-range with activated auto-calibration
- Synchronous Serial Communication (SSC) with 15 bit representation of absolute angle value (0.01° resolution)
- Incremental Interface (IIF) with 12 bit resolution of angle value on the output (one count per 0.088° angle step).
- Incremental Interface (IIF) in A/B mode with absolut count enabled (provides absolute value at output)
- Fast angle update period (42.7µs).
- Autocalibration mode 1 enabled.
- Prediction disabled.
- Hysteresis set to 0.703°.
- Bus mode operation of multiple sensors on one line is possible with SSC in open-drain configuration.
- Diagnostic functions and status information.
- IFA/IFB/IFC pins set to push-pull output.
- Bi-directional SSC interface. DATA pin set to push-pull output with 8Mbit/s baud rate (2Mbit/s in open-drain).
- IFA/IFB/IFC pins set to strong driver, DATA pin set to strong driver, fast edge.
- Voltage spike filter on input pads disabled.
- Two separate highly accurate single bit SD-ADC.
- RoHS compliant (Pb-free package).
- Halogen-free.

1.3 Application Example

The TLI5012B E1000 GMR-based angle sensor is designed for angular position sensing in industrial and consumer applications such as electrical commutated motor (e.g. BLDC), fans or pumps.

1.4 Disclaimer

The qualification of this product is based on JEDEC JESD47 and may reference existing qualification results of similar products. Such referring is justified by the structural similarity of the products. The product is not qualified and manufactured according to the requirements of Infineon Technologies with regard to automotive applications.

2 Functional Description

2.1 Block Diagram

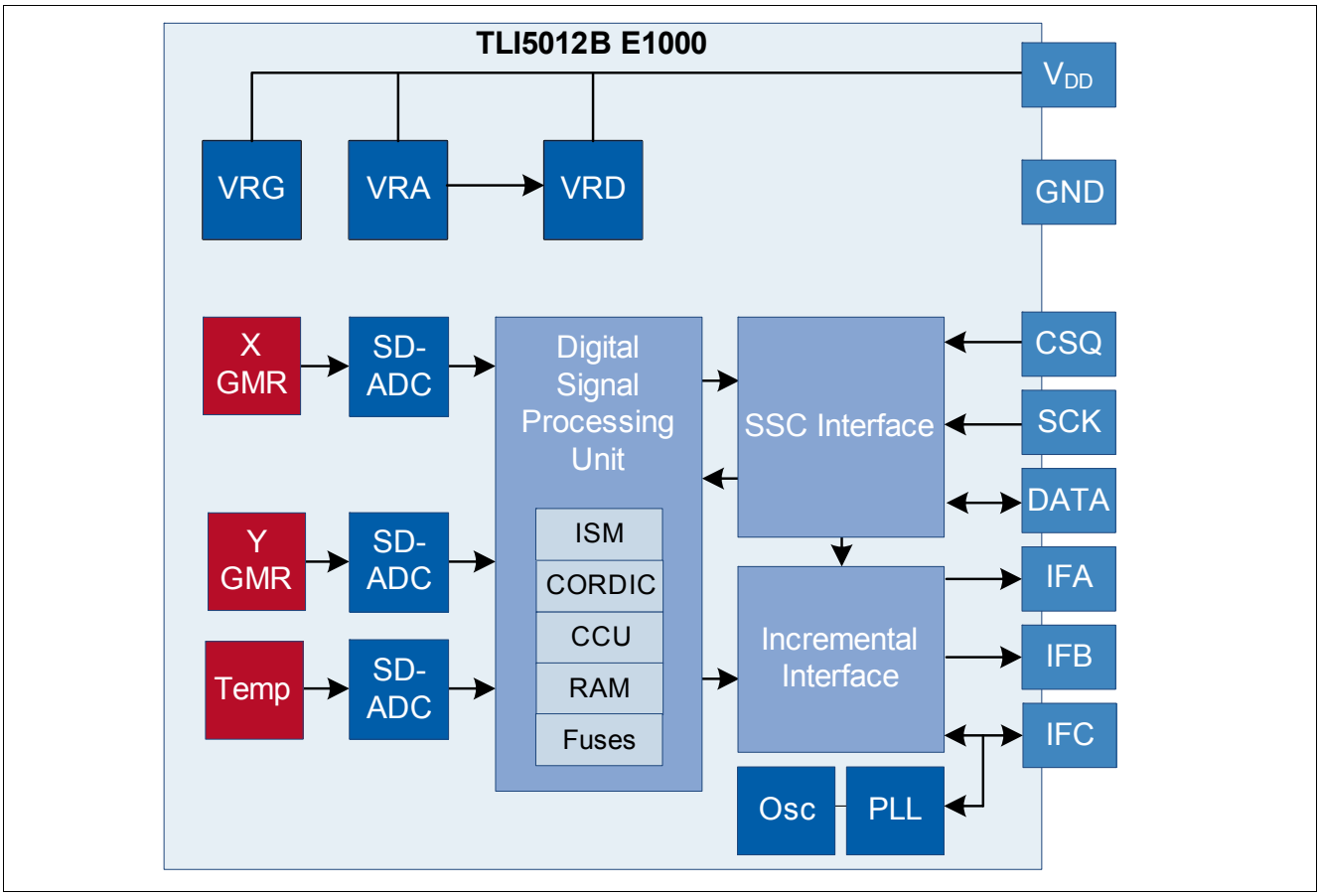

Figure 2-1 TLI5012B E1000 block diagram

2.2 Functional Block Description

2.2.1 Internal Power Supply

The internal stages of the TLI5012B E1000 are supplied with several voltage regulators:

- GMR Voltage Regulator, VRG
- Analog Voltage Regulator, VRA
- Digital Voltage Regulator, VRD (derived from VRA)

These regulators are directly connected to the supply voltage V_{DD}.

2.2.2 Oscillator and PLL

The digital clock of the TLI5012B E1000 is given by the Phase-Locked Loop (PLL), which is by default fed by an internal oscillator. In order to synchronize the TLI5012B E1000 with other ICs in a system, the TLI5012B E1000

can be configured via SSC interface to use an external clock signal supplied on the IFC pin as source for the PLL, instead of the internal clock. External clock mode is only available in PWM or SPC interface configuration.

2.2.3 SD-ADC

The **S**igma-**D**elta **A**nalog-**D**igital-**C**onverters (**SD-ADC**) transform the analog GMR voltages and temperature voltage into the digital domain.

2.2.4 Digital Signal Processing Unit

The Digital Signal Processing Unit (DSPU) contains the:

- **I**ntelligent **S**tate **M**achine (**ISM**), which does error compensation of offset, offset temperature drift, amplitude synchronicity and orthogonality of the raw signals from the GMR bridges, and performs additional features such as auto-calibration, prediction and angle speed calculation
- **CO**ordinate **R**otation **DI**gital **C**omputer (**CORDIC**), which contains the trigonometric function for angle calculation
- **C**apture **C**ompare **U**nit (**CCU**), which is used to generate the PWM and SPC signals
- **R**andom **A**ccess **M**emory (**RAM**), which contains the configuration registers
- Laser Fuses, which contain the calibration parameters for the error-compensation and the IC default configuration, which is loaded into the RAM at startup

2.2.5 Interfaces

Bi-directional communication with the TLI5012B E1000 is enabled by a three-wire SSC interface. In parallel to the SSC interface, an Incremental Interface (IIF) can be selected, which is available on the IFA, IFB, IFC pins.

2.3 Sensing Principle

The Giant Magneto Resistance (GMR) sensor is implemented using vertical integration. This means that the GMR-sensitive areas are integrated above the logic part of the TLI5012B E1000 device. These GMR elements change their resistance depending on the direction of the magnetic field.

Four individual GMR elements are connected to one Wheatstone sensor bridge. These GMR elements sense one of two components of the applied magnetic field:

- X component, V_x (cosine) or the
- Y component, V_y (sine)

With this full-bridge structure the maximum GMR signal is available and temperature effects cancel out each other.

In **Figure 2-2**, the arrows in the resistors represent the magnetic direction which is fixed in the reference layer. If the external magnetic field is parallel to the direction of the Reference Layer, the resistance is minimal. If they are anti-parallel, resistance is maximal.

The output signal of each bridge is only unambiguous over 180° between two maxima. Therefore two bridges are oriented orthogonally to each other to measure 360°.

With the trigonometric function ARCTAN2, the true 360° angle value is calculated out of the raw X and Y signals from the sensor bridges.

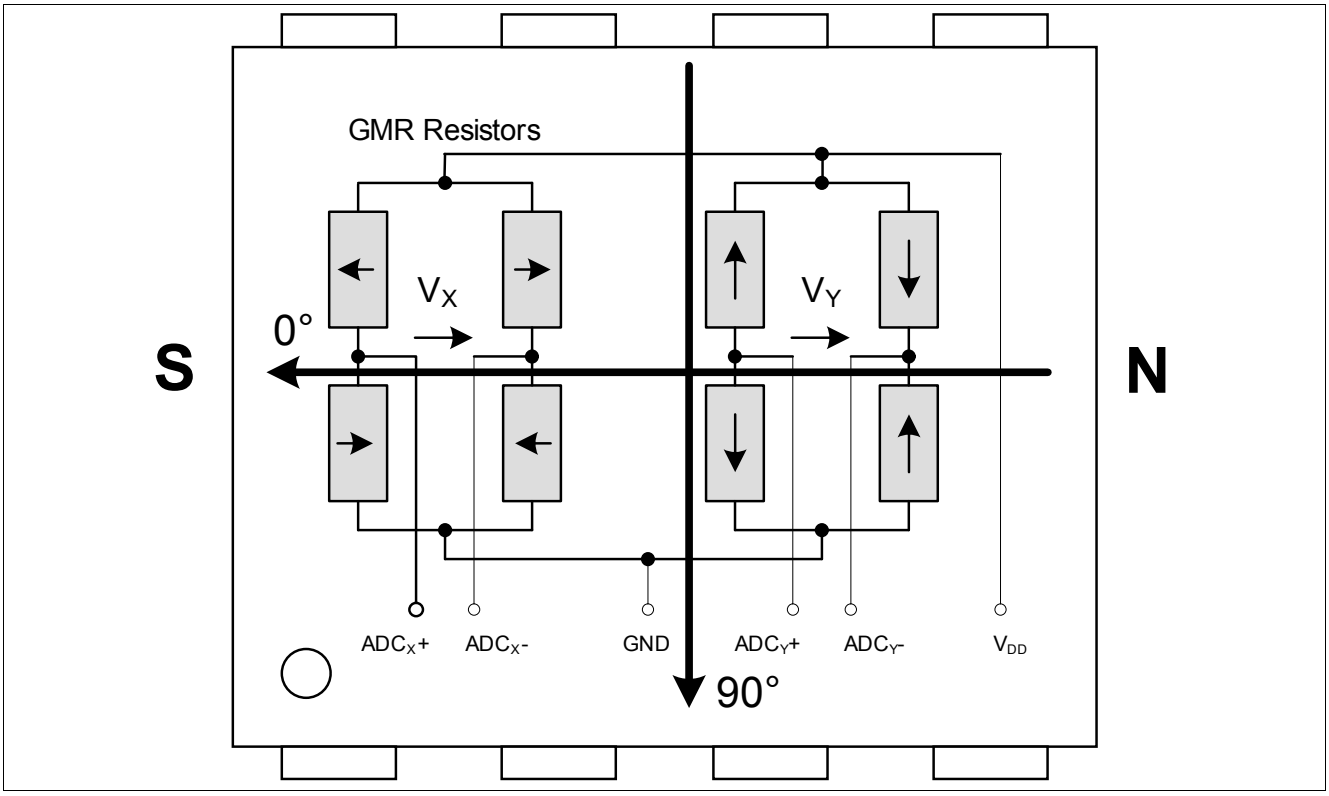

Figure 2-2 Sensitive bridges of the GMR sensor (not to scale)

Attention: Due to the rotational placement inaccuracy of the sensor IC in the package, the sensors 0° position may deviate by up to 3° from the package edge direction indicated in Figure 2-2.

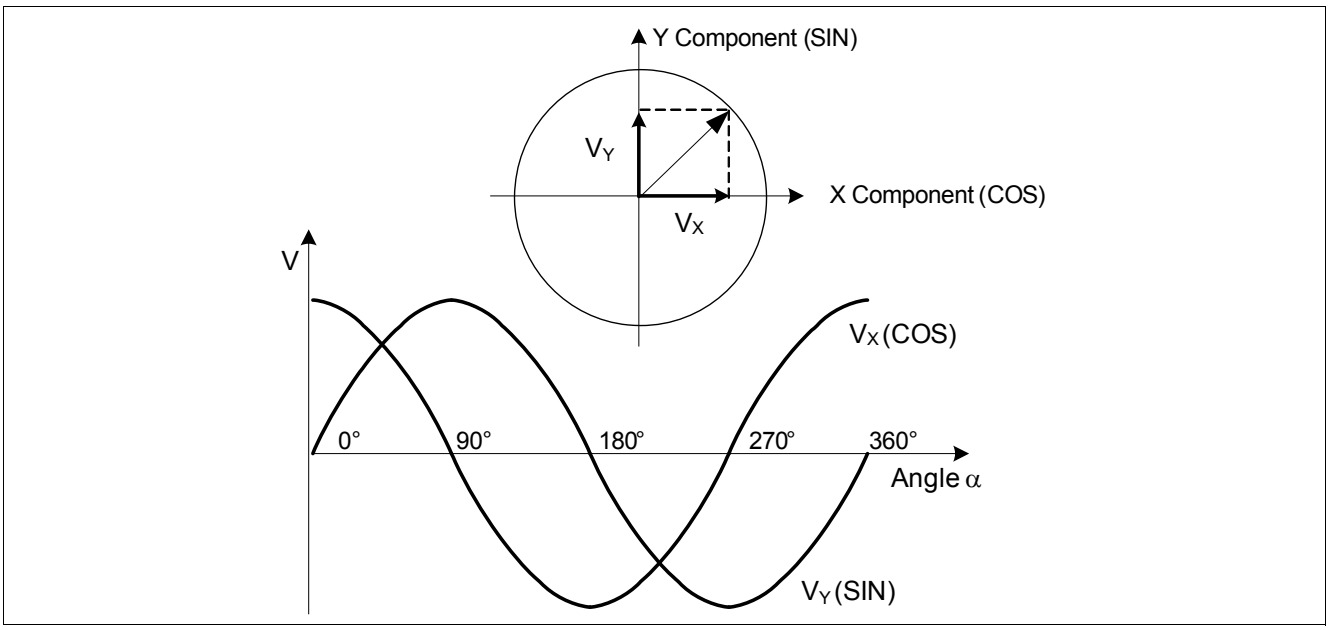

Figure 2-3 Ideal output of the GMR sensor bridges

2.4 Pin Configuration

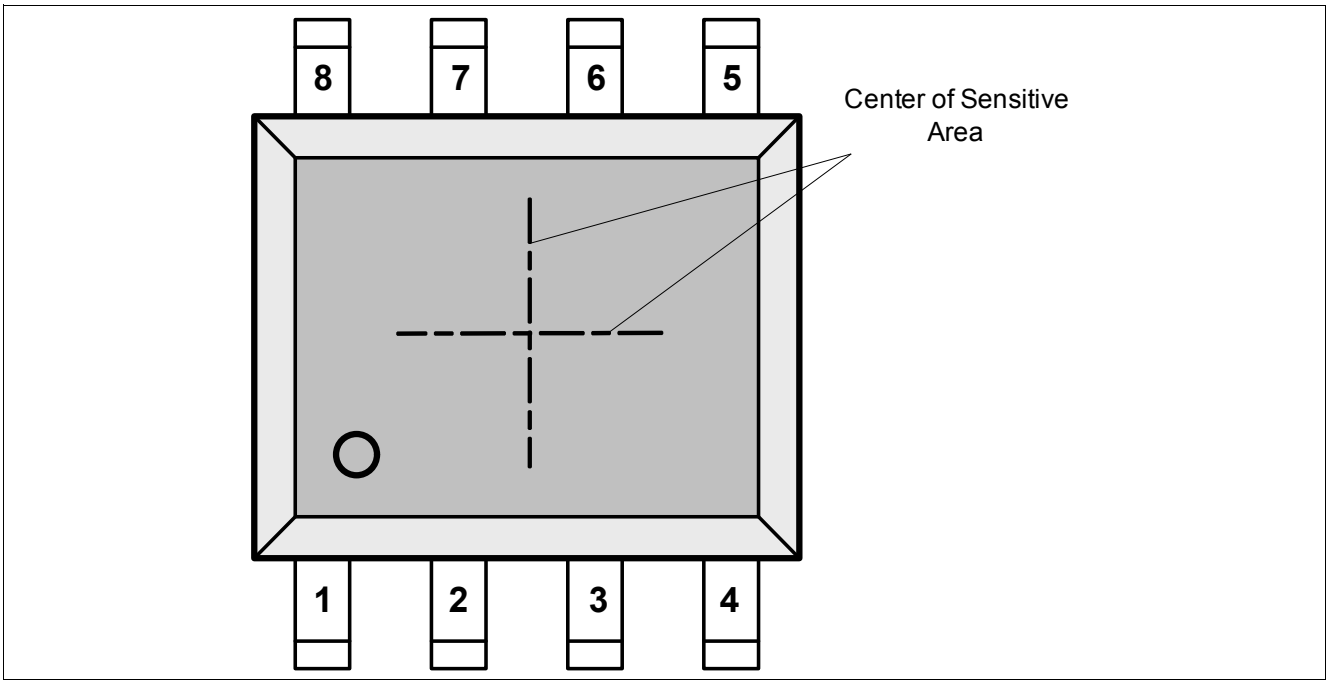

Figure 2-4 Pin configuration (top view)

2.5 Pin Description

Table 2-1 Pin Description

Pin No.	Symbol	In/Out	Function
1	IFC (IIF_IDX)	O	Interface C: IIF Index
2	SCK	I	SSC Clock
3	CSQ	I	SSC Chip Select
4	DATA	I/O	SSC Data
5	IFA (IIF_A)	O	Interface A: IIF Phase A
6	V_{DD}	-	Supply Voltage
7	GND	-	Ground
8	IFB (IIF_B)	O	Interface B: IIF Phase B

3 Application Circuits

The application circuits in this chapter show the various communication possibilities of the TLI5012B E1000. The pin output mode configuration is device-specific and it can be either push-pull or open-drain. The bit IFAB_OD (register IFAB, $0D_H$) indicates the output mode for the IFA, IFB and IFC pins. The SSC pins are by default push-pull (bit SSC_OD, register MOD_3, 09_H).

Figure 3-1 shows a basic block diagram of a TLI5012B E1000 with Incremental Interface and SSC configuration. The derivate TLI5012B E1000 is by default configured with push-pull IFA (IIF_A), IFB (IIF_ B) and IFC (IIF_IDX) pins.

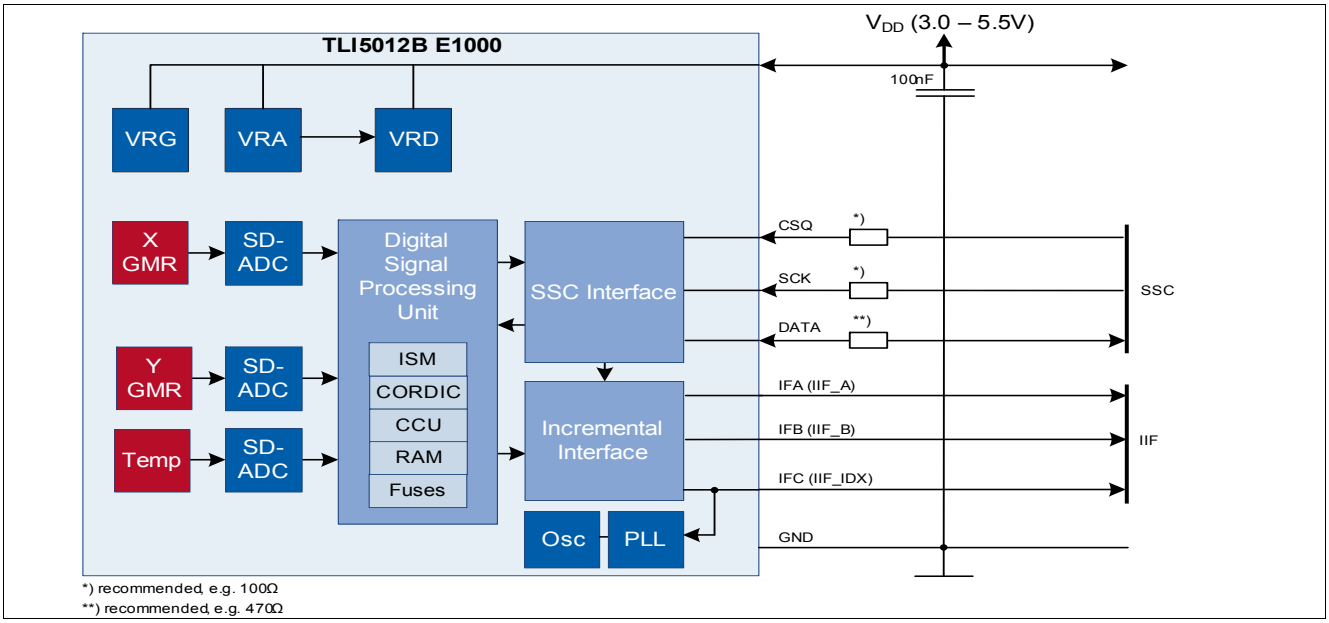

Figure 3-1 Application circuit for TLI5012B E1000 with IIF interface and SSC (using internal CLK)

In case that the IFA, IFB and IFC pins are configurated via the SSC interface as open-drain pins, three resistors (one for each line) between output line and V_{DD} would be recommended (e.g. 2.2kΩ).

Synchronous Serial Communication (SSC) configuration

In **Figure 3-1** the SSC interface has the default push-pull configuration (see details in **Figure 3-2**). Series resistors on the DATA, SCK (serial clock signal) and CSQ (chip select) lines are recommended to limit the current in the erroneous case that either the sensor pushes high and the microcontroller pulls low at the same time or vice versa. The resistors in the SCK and CSQ lines are only necessary in case of disturbances or noise.

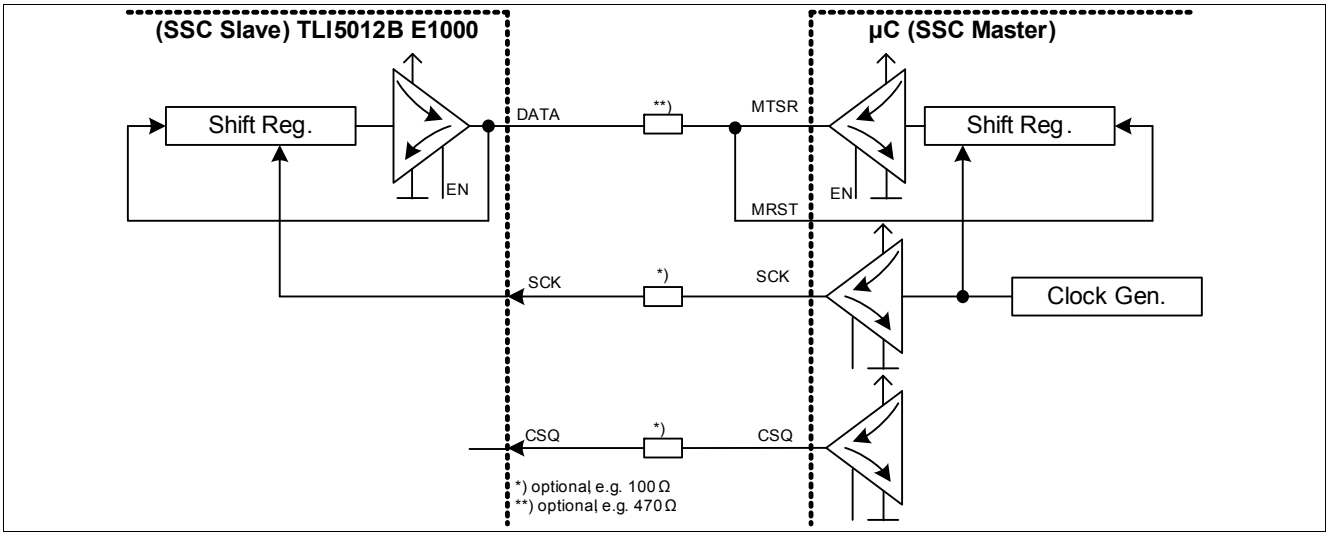

Figure 3-2 SSC configuration in sensor-slave mode with push-pull outputs (high-speed application)

It is also possible to use an open-drain setup for the DATA, SCK and CSQ lines. This setup is designed to communicate with a microcontroller in a bus system, together with other SSC slaves (e.g. two TLI5012B E1000 devices for redundancy reasons). This mode can be activated using the bit SSC_OD.

The open-drain configuration can be seen in **Figure 3-3**. Series resistors on the DATA, SCK, and CSQ lines are recommended to limit the current in case either the microcontroller or the sensor are accidentally switched to push-pull. A pull-up resistor of typ. 1 kΩ is required on the DATA line.

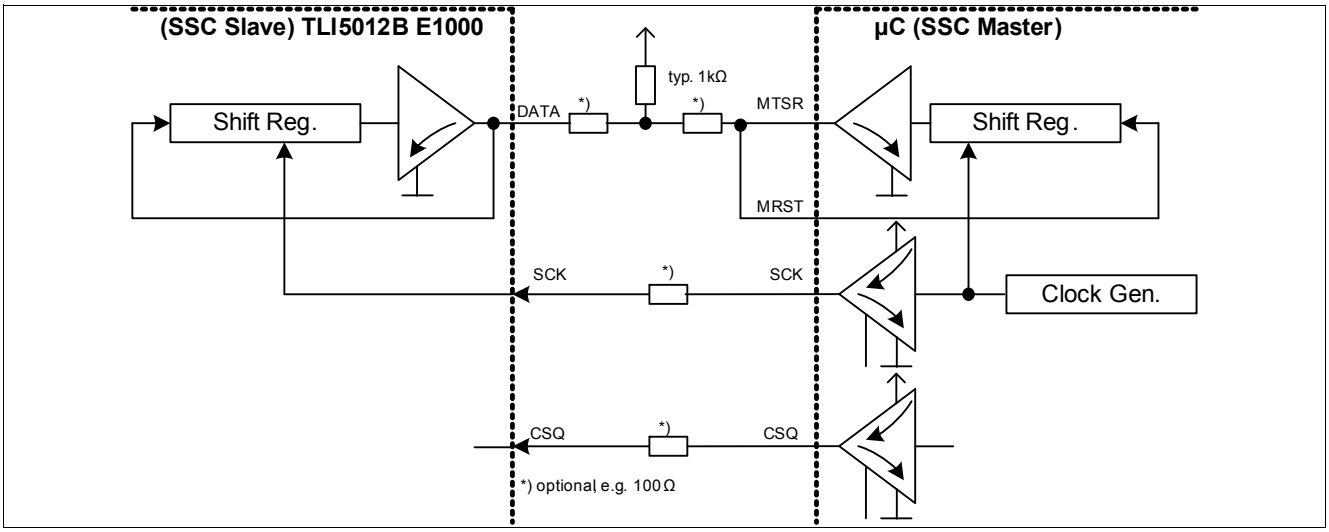

Figure 3-3 SSC configuration in sensor-slave mode and open-drain (bus systems)

4 Specification

4.1 Absolute Maximum Ratings

Table 4-1 Absolute maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Voltage on V_{DD} pin with respect to ground (V_{SS})	V_{DD}	-0.5		6.5	V	Max 40 h/Lifetime
Voltage on any pin with respect to ground (V_{SS})	V_{IN}	-0.5		6.5	V	
				V_{DD} + 0.5	V	
Junction temperature	T_J	-40		125	°C	
Magnetic field induction	B			200	mT	Max. 5 min @ T_A = 25°C
				150	mT	Max. 5 h @ T_A = 25°C
Storage temperature	T_{ST}	-40		125	°C	Without magnetic field

Attention: Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the device.

4.2 Operating Range

The following operating conditions must not be exceeded in order to ensure correct operation of the TLI5012B E1000. All parameters specified in the following sections refer to these operating conditions, unless otherwise noted. **Table 4-2** is valid for -40°C < T_J < 125°C unless otherwise noted.

Table 4-2 Operating range and parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply voltage	V_{DD}	3.0	5.0	5.5	V	[1]
Supply current	I_{DD}		14	16	mA	
Magnetic induction at T_J = 25°C[2][3]	B_{XY}	30		50	mT	-40°C < T_J < 125°C
		30		60	mT	-40°C < T_J < 100°C
		30		70	mT	-40°C < T_J < 85°C
Extended magnetic induction range at T_J = 25°C[2][3]	B_{XY}	25		30	mT	Additional angle error of 0.1°
Angle range	Ang	0		360	°	
POR level	V_{POR}	2.0		2.9	V	Power-on reset
POR hysteresis	V_{PORhy}		30		mV	

Table 4-2 Operating range (cont'd)**and parameters**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Power-on time[4)]	t_{Pon}		5	7	ms	$V_{DD} > V_{DDmin}$;
Fast Reset time[5)]	t_{Rfast}			0.5	ms	Fast reset is triggered by disabling startup BIST (S_BIST = 0), then enabling chip reset (AS_RST = 1)

1) Directly blocked with 100-nF ceramic capacitor
2) Values refer to a homogeneous magnetic field (B_{XY}) without vertical magnetic induction (B_Z = 0mT).
3) See **Figure 4-1**
4) During "Power-on time," write access is not permitted (except for the switch to External Clock which requires a readout as a confirmation that external clock is selected)
5) Not subject to production test - verified by design/characterization

The field strength of a magnet can be selected within the colored area of **Figure 4-1**. By limitation of the junction temperature, a higher magnetic field can be applied. In case of a maximum temperature T_J = 100°C, a magnet with up to 60mT at T_J = 25°C is allowed.

It is also possible to widen the magnetic field range for higher temperatures. In that case, additional angle errors have to be considered.

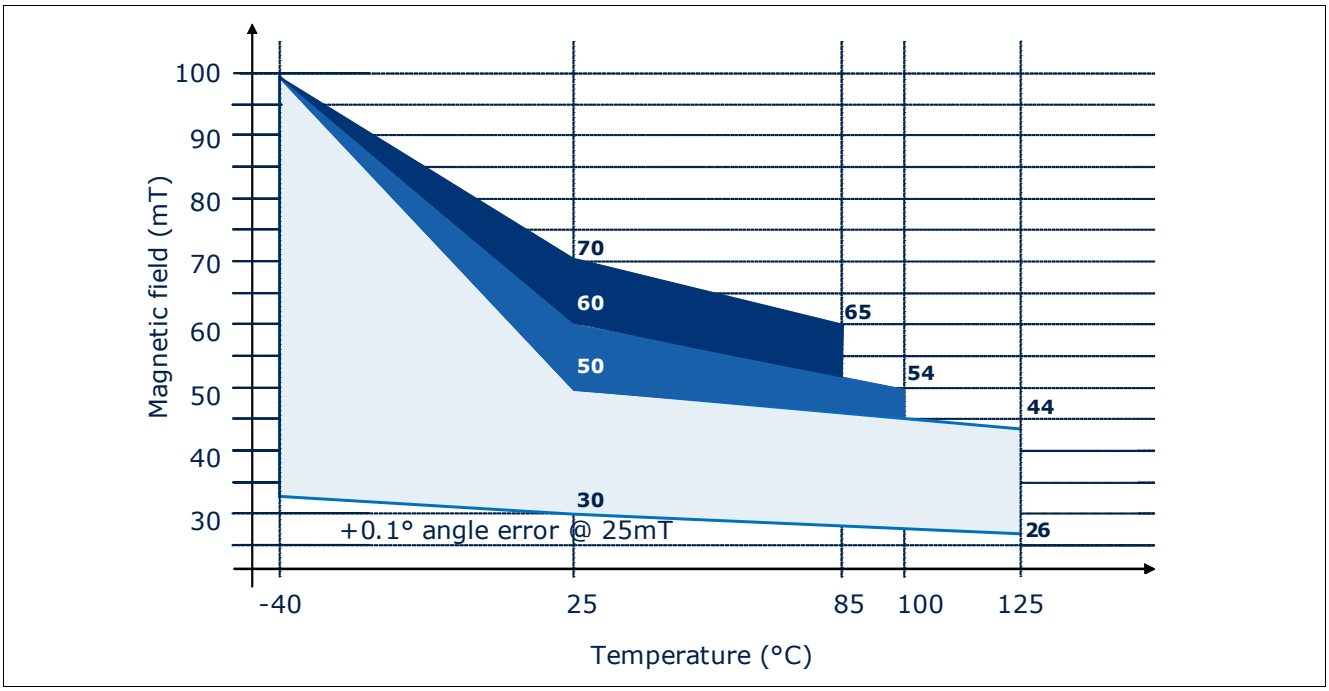

Figure 4-1 Allowed magnetic field range as function of junction temperature.

4.3 Characteristics

4.3.1 Input/Output characteristics

The indicated parameters apply to the full operating range, unless otherwise specified. The typical values correspond to a supply voltage V_{DD} = 5.0 V and 25 °C, unless individually specified. All other values correspond to -40 °C < T_J < 125°C.

Within the register MOD_3, the driver strength and the slope for push-pull communication can be varied depending on the sensor output. The driver strength is specified in **Table 4-3** and the slope fall and rise time in **Table 4-4**.

Table 4-3 Input voltage and output currents

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input voltage	V_{IN}	-0.3		5.5	V	
				V_{DD}+ 0.3	V	
Output current (DATA-Pad)	I_Q			-25	mA	PAD_DRV =’0x’, sink current[1)2)]
				-5	mA	PAD_DRV =’10’, sink current[1)2)]
				-0.4	mA	PAD_DRV =’11’, sink current[1)2)]
Output current (IFA / IFB / IFC - Pad)	I_Q			-15	mA	PAD_DRV =’0x’, sink current[1)2)]
				-5	mA	PAD_DRV =’1x’, sink current[1)2)]

1) Max. current to GND over open-drain output

2) At V_{DD} = 5 V

Table 4-4 Driver strength characteristic

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Output rise/fall time	t_{fall}, t_{rise}			8	ns	DATA, 50 pF, PAD_DRV=’00’[1)2)]
				28	ns	DATA, 50 pF, PAD_DRV=’01’[1)2)]
				45	ns	DATA, 50 pF, PAD_DRV=’10’[1)2)]
				130	ns	DATA, 50 pF, PAD_DRV=’11’[1)2)]
				15	ns	IFA/IFB, 20 pF, PAD_DRV=’0x’[1)2)]
				30	ns	IFA/IFB, 20 pF, PAD_DRV=’1x’[1)2)]

1) Valid for push-pull output

2) Not subject to production test - verified by design/characterization

Table 4-5 Electrical parameters for 4.5 V < V_{DD} < 5.5 V

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input signal low-level	V_{L5}			0.3 V_{DD}	V	
Input signal high level	V_{H5}	0.7 V_{DD}			V	
Output signal low-level	V_{OL5}			1	V	DATA; I_Q = -25 mA (PAD_DRV='0x'), I_Q = -5 mA (PAD_DRV='10'), I_Q = -0.4 mA (PAD_DRV='11')
				1	V	IFA,B,C; I_Q = -15 mA (PAD_DRV='0x'), I_Q = -5 mA (PAD_DRV='1x')
Pull-up current[1)]	I_{PU}	-10		-225	µA	CSQ
		-10		-150	µA	DATA
Pull-down current[2)]	I_{PD}	10		225	µA	SCK
		10		150	µA	IFA, IFB, IFC

1) Internal pull-ups on CSQ and DATA pin are always enabled.

2) Internal pull-downs on IFA, IFB and IFC are enabled during startup and in open-drain mode, internal pull-down on SCK is always enabled.

Table 4-6 Electrical parameters for 3.0 V < V_{DD} < 3.6 V

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input signal low-level	V_{L3}			0.3 V_{DD}	V	
Input signal high level	V_{H3}	0.7 V_{DD}			V	
Output signal low-level	V_{OL3}			0.9	V	DATA; I_Q = -15 mA (PAD_DRV='0x'), I_Q = -3 mA (PAD_DRV='10'), I_Q = -0.24 mA (PAD_DRV='11')
				0.9	V	IFA,IFB; I_Q = - 10 mA (PAD_DRV='0x'), I_Q = -3 mA (PAD_DRV='1x')
Pull-up current[1)]	I_{PU}	-3		-225	µA	CSQ
		-3		-150	µA	DATA
Pull-down current[2)]	I_{PD}	3		225	µA	SCK
		3		150	µA	IFA, IFB, IFC

1) Internal pull-ups on CSQ and DATA pin are always enabled.

2) Internal pull-downs on IFA, IFB and IFC are enabled during startup and in open-drain mode, internal pull-down on SCK is always enabled.

4.3.2 ESD Protection

Table 4-7 ESD protection

Parameter	Symbol	Values		Unit	Notes
		Min.	Max.		
ESD voltage	V_{HBM}		±4.0	kV	1)
	V_{CDM}		±0.5	kV	2)

1) Human Body Model (HBM) according to ANSI/ESDA/JEDEC JS-001
2) Charged Device Model (CDM) according to JESD22-C101

4.3.3 GMR Parameters

All parameters apply over B_{XY} = 30mT and T_A = 25°C, unless otherwise specified.

Table 4-8 Basic GMR parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
X, Y output range	RG_{ADC}			±23230	digits	Operating range[1]
X, Y amplitude[2]	A_X, A_Y	6000	9500	15781	digits	At ambient temperature
		3922		20620	digits	Operating range[1]
X, Y synchronicity[3]	k	87.5	100	112.49	%	
X, Y offset[4]	O_X, O_Y	-2048	0	+2047	digits	
X, Y orthogonality error	φ	-11.25	0	+11.24	°	
X, Y amplitude without magnet	X_0, Y_0			+4096	digits	Operating range[1]

1) Not subject to production test - verified by design/characterization
2) See **Figure 4-2**
3) $k = 100*(A_X/A_Y)$
4) $O_Y=(Y_{MAX} + Y_{MIN}) / 2$; $O_X = (X_{MAX} + X_{MIN}) / 2$

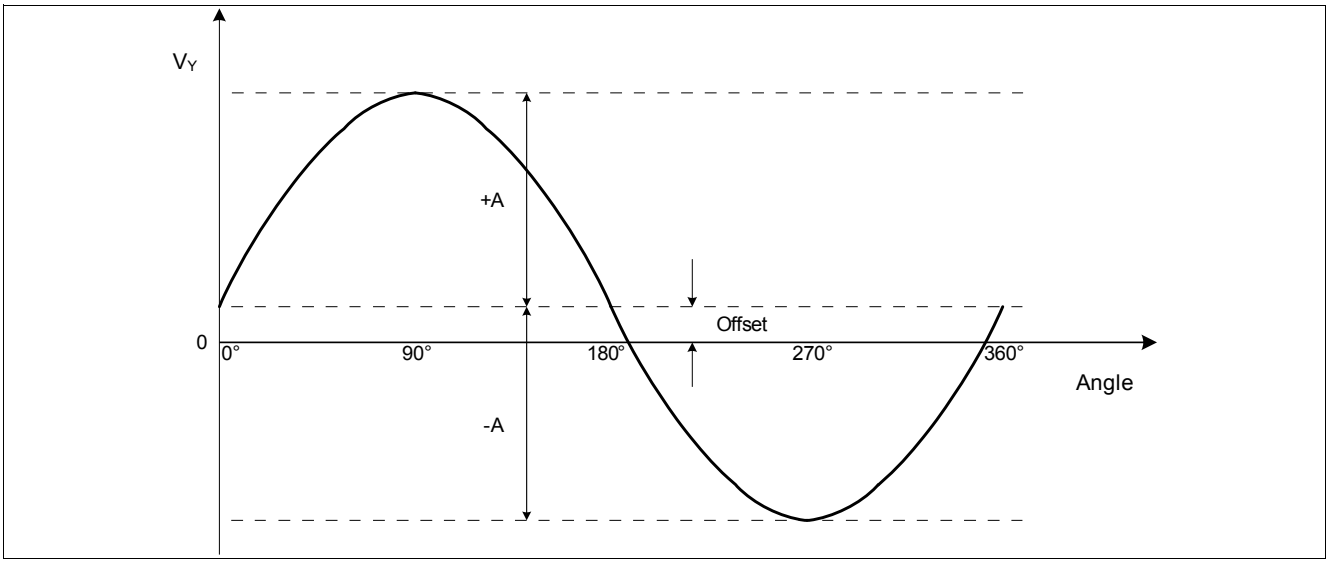

Figure 4-2 Offset and amplitude definition

4.3.4 Angle Performance

After internal calculation, the sensor has a remaining error, as shown in **Table 4-9**. The error value refers to B_Z= 0mT and the operating conditions given in **Table 4-2 "Operating range and parameters" on Page 16**.

The overall angle error represents the relative angle error. This error describes the deviation from the reference line after zero-angle definition. It is valid for a static magnetic field. If the magnetic field is rotating during the measurement, an additional propagation error is caused by the angle delay time (see **Table 4-10 "Signal processing" on Page 23**), which the sensor needs to calculate the angle from the raw sine and cosine values from the MR bridges. In fast-turning applications, prediction can be enabled to reduce this propagation error.

Table 4-9 Angle performance

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Overall angle error at 25°C	α_{Err}			1.0	°	Including lifetime drift[1)2)3)].
Overall angle error -40°C...125°C	α_{Err}			1.9	°	Including temperature & lifetime drift[1)2)3)4)]

1) Including hysteresis error, caused by revolution direction change
2) Relative error after zero angle definition
3) With autocalibration (pre-configured by default). No temperature changes >5 Kelvin within 1.5 revolutions considered.
4) Not subject to production test - verified by design/characterization

Autocalibration enables online parameter calculation and therefore reduces the angle error due to temperature and lifetime drifts. The TLI5012B E1000 needs 1.5 revolutions to generate new autocalibration parameters. These parameters are continuously updated. The parameters are updated in a smooth way (one Least-Significant Bit within the chosen range or time) to avoid an angle jump on the output.

If the temperature changes by more than 5 Kelvin during 1.5 revolutions an additional error has to be added to the specified angle error in **Table 4-9**. This error depends on the temperature change (Delta Temperature) as well as from the initial temperature (Tstart) as shown in **Figure 4-3**. Once the temperature stabilizes and the application completes 1.5 revolutions, then the angle error is as specified in **Table 4-9**.

For negative Delta Temperature changes (from higher to lower temperatures) the additional angle error will be smaller than the corresponding positive Delta Temperature changes (from lower to higher temperatures) shown in **Figure 4-3**. The **Figure 4-3** applies to the worst case.

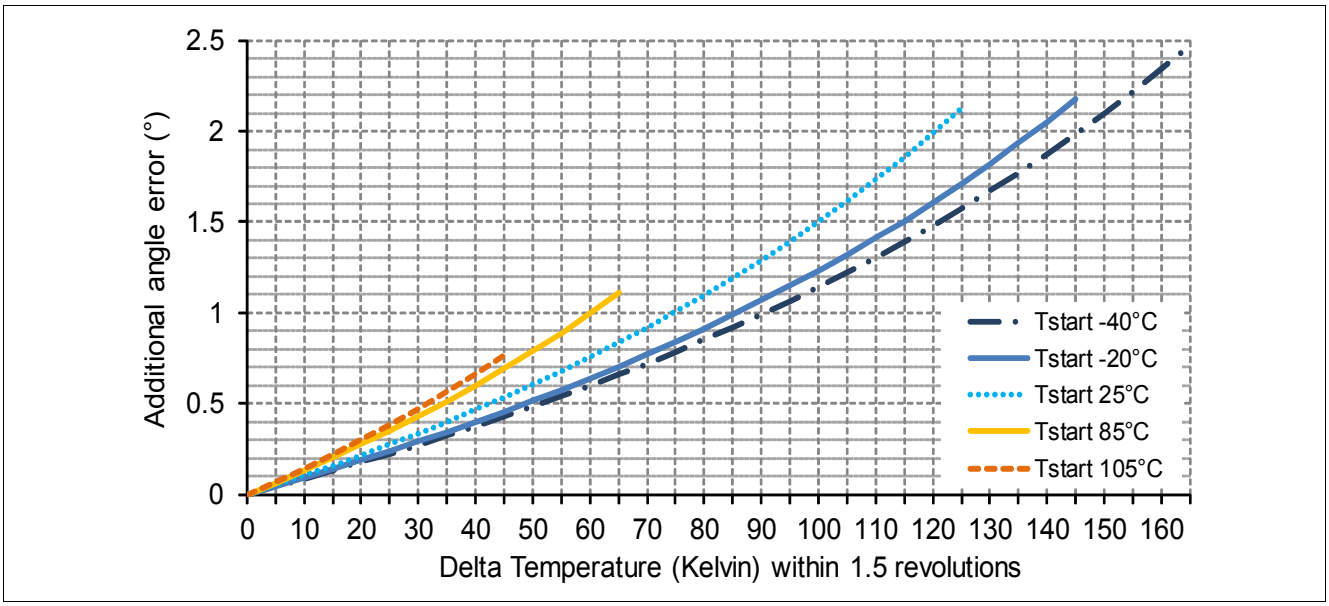

Figure 4-3 Additional angle error for temperature changes above 5 Kelvin within 1.5 revolutions

4.3.5 Signal Processing

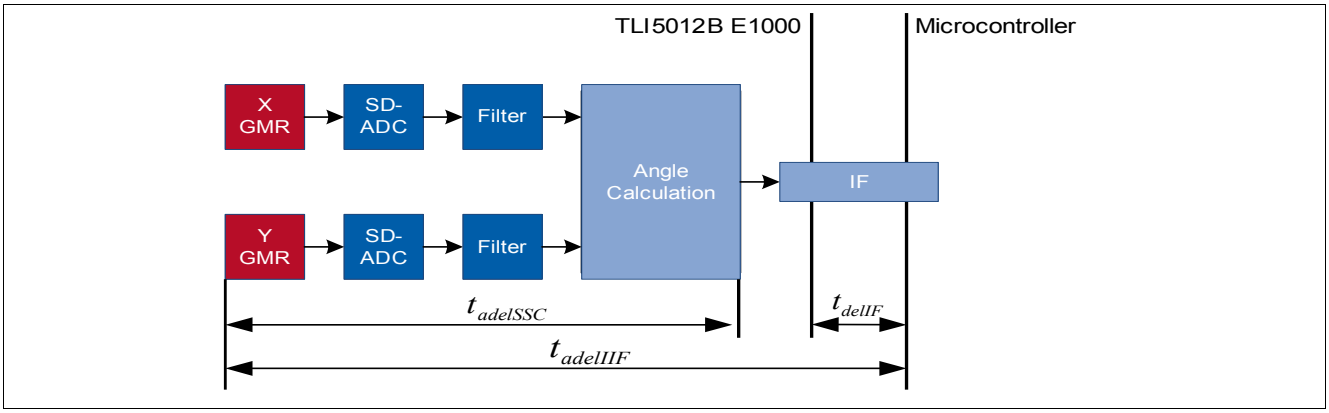

Figure 4-4 Signal path

The signal path of the TLI5012B E1000 is depicted in **Figure 4-4**. It consists of the GMR-bridge, ADC, filter and angle calculation. The delay time between a physical change in the GMR elements and a signal on the output depends on the filter and interface configurations. In fast turning applications, this delay causes an additional rotation speed dependent angle error.

The TLI5012B E1000 has an optional prediction feature, which serves to reduce the speed dependent angle error in applications where the rotation speed does not change abruptly. Prediction uses the difference between current and last two angle values to approximate the angle value which will be present after the delay time (see **Figure 4-5**). The output value is calculated by adding this difference to the measured value, according to **Equation (4.1)**.

$$\alpha(t+1) = \alpha(t) + \alpha(t-1) - \alpha(t-2) \tag{4.1}$$

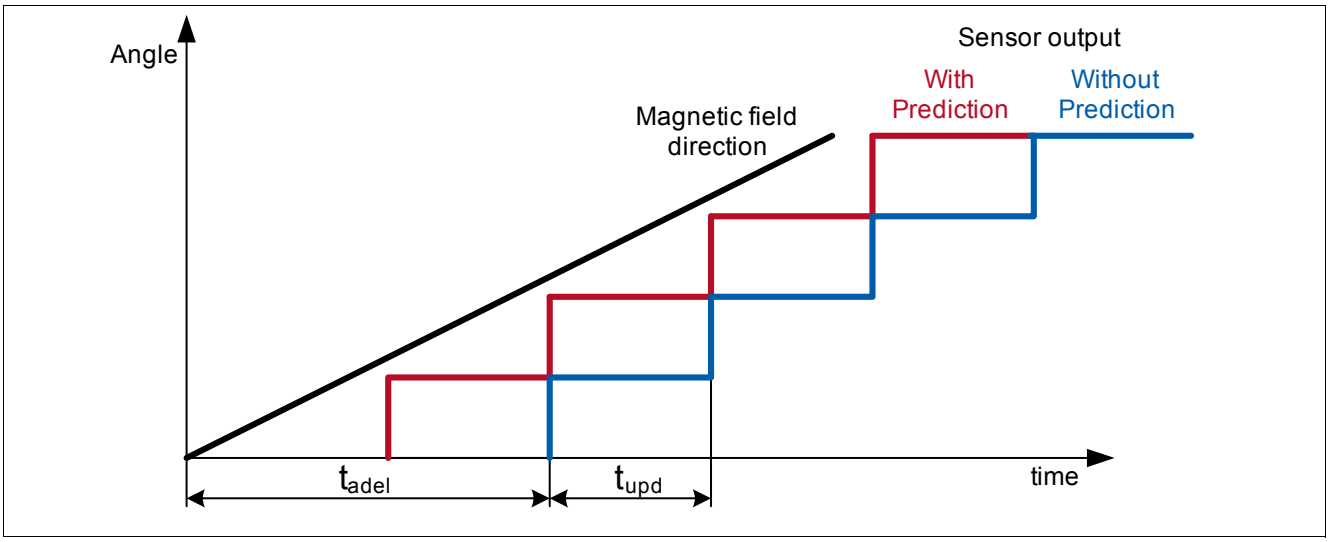

Figure 4-5 Delay of sensor output

Table 4-10 Signal processing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Filter update period	t_{upd}		42.7		µs	FIR_MD = 1 (default)[1]
			85.3		µs	FIR_MD = 2[1]
			170.6		µs	FIR_MD = 3[1]
Angle delay time without prediction[2]	$t_{adelSSC}$		85	95	µs	FIR_MD = 1[1]
			150	165	µs	FIR_MD = 2[1]
			275	300	µs	FIR_MD = 3[1]
	$t_{adelIIF}$		120	135	µs	FIR_MD = 1[1]
			180	200	µs	FIR_MD = 2[1]
			305	330	µs	FIR_MD = 3[1]
Angle delay time with prediction[2]	$t_{adelSSC}$		45	50	µs	FIR_MD = 1; PREDICT = 1[1]
			65	70	µs	FIR_MD = 2; PREDICT = 1[1]
			105	115	µs	FIR_MD = 3; PREDICT = 1[1]
	$t_{adelIIF}$		75	90	µs	FIR_MD = 1; PREDICT = 1[1]
			95	110	µs	FIR_MD = 2; PREDICT = 1[1]
			135	150	µs	FIR_MD = 3; PREDICT = 1[1]
Angle noise (RMS)	N_{Angle}		0.08		°	FIR_MD = 1[1]
			0.05		°	FIR_MD = 2[1](default)
			0.04		°	FIR_MD = 3[1]

1) Not subject to production test - verified by design/characterization

2) Valid at constant rotation speed

All delay times specified in **Table 4-10** are valid for an ideal internal oscillator frequency of 24 MHz. For the exact timing, the variation of the internal oscillator frequency has to be taken into account (see **Chapter 4.3.6**)

4.3.6 Clock Supply (CLK Timing Definition)

The internal clock supply of the TLI5012B E1000 is subject to production-specific variations, which have to be considered for all timing specifications.

Table 4-11 Internal clock timing specification

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Digital clock	f_{DIG}	22.3	24	26.3	MHz	
Internal oscillator frequency	f_{CLK}	3.7	4.0	4.4	MHz	

4.3.6.1 External clock operation

In order to fix the IC timing and synchronize the TLI5012B E1000 with other ICs in a system, it can be switched to operate with an external clock signal supplied to the IFC pin. The clock input signal must fulfill certain requirements:

- The high or low pulse width must not exceed the specified values, because the PLL needs a minimum pulse width and must be spike-filtered.
- The duty cycle factor should typically be 50%, but it can vary between 30% and 70%.
- The PLL is triggered at the positive edge of the clock. If more than 2 edges are missing, a chip reset is generated automatically and the sensor restarts with the internal clock. This is indicated by the S_RST, and CLK_SEL bits, and additionally by the Safety Word (see **Chapter 4.4.2.2**).

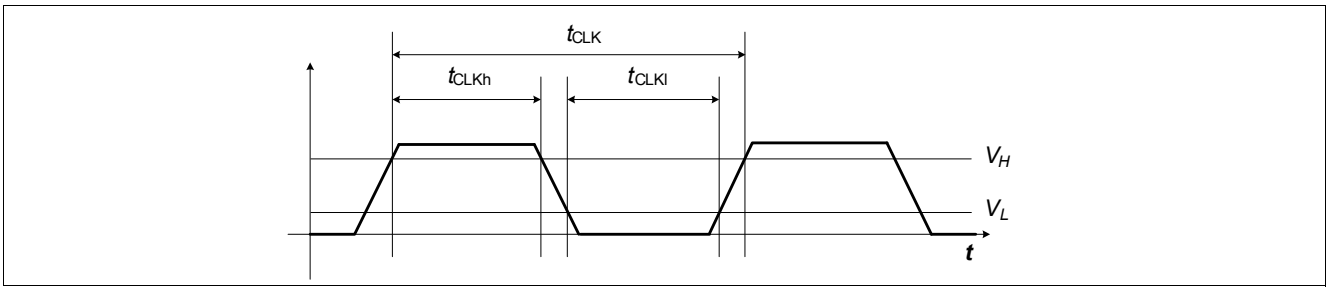

Figure 4-6 External CLK timing definition

Table 4-12 External Clock Specification

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input frequency	f_{CLK}	3.7	4.0	4.4	MHz	
CLK duty cycle[1)2)]	CLK_{DUTY}	30	50	70	%	
CLK rise time	t_{CLKr}			30	ns	From V_L to V_H
CLK fall time	t_{CLKf}			30	ns	From V_H to V_L

1) Minimum duty cycle factor: $t_{CLKh(min)}$ / t_{CLK} with t_{CLK}= 1 / f_{CLK}

2) Maximum duty cycle factor: $t_{CLKh(max)}$ / t_{CLK} with t_{CLK}= 1 / f_{CLK}

4.4 Interfaces

4.4.1 Incremental Interface (IIF)

The **I**ncremental **I**nter**f**ace (**IIF**) emulates the operation of an optical quadrature encoder with a 50% duty cycle. It transmits a square pulse per angle step, where the width of the steps can be configured from 9bit (512 steps per full rotation) to 12bit (4096 steps per full rotation) within the register MOD_4 (IFAB_RES). The rotation direction is given either by the phase shift between the two channels IFA and IFB (A/B mode) or by the level of the IFB channel (Step/Direction mode), as shown in **Figure 4-7** and **Figure 4-8**. The incremental interface can be configured for A/B mode or Step/Direction mode in register MOD_1 (IIF_MOD).

Using the Incremental Interface requires an up/down counter on the microcontroller, which counts the pulses and thus keeps track of the absolute position. The counter can be synchronized periodically by using the SSC interface in parallel. The angle value (AVAL register) read out by the SSC interface can be compared to the stored counter value. In case of a non-synchronization, the microcontroller adds the difference to the actual counter value to synchronize the TLI5012B E1000 with the microcontroller.

After startup, the IIF transmits a number of pulses which correspond to the actual absolute angle value. Thus, the microcontroller gets the information about the absolute position. The Index Signal that indicates the zero crossing is available on the IFC pin.

Sensors with preset IIF are available as TLI5012B E1000.

A/B Mode

The phase shift between phases A and B indicates either a clockwise (A follows B) or a counterclockwise (B follows A) rotation of the magnet.

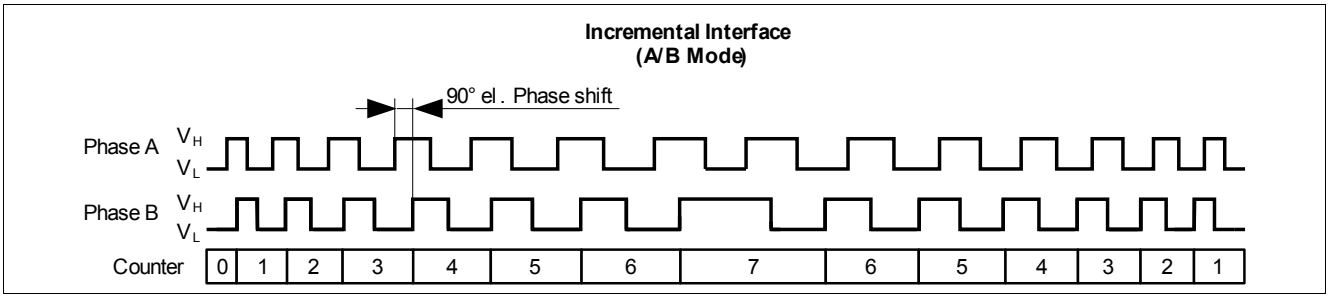

Figure 4-7 Incremental interface with A/B mode

Step/Direction Mode

Phase A pulses out the increments and phase B indicates the direction.

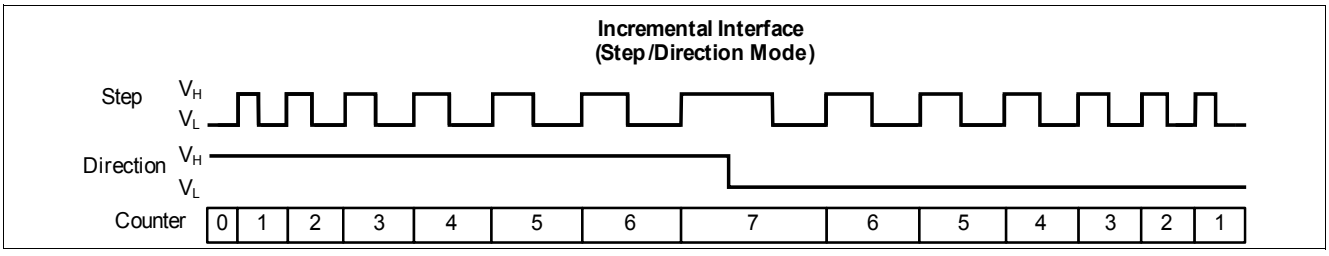

Figure 4-8 Incremental interface with Step/Direction mode

Table 4-13 Incremental Interface

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Incremental output frequency	f_{Inc}			1.0	MHz	Frequency of phase A and phase B[1)]
Index pulse width	$t_{0°}$		5		µs	0°[1)]

1) Not subject to production test - verified by design/characterization

4.4.2 Synchronous Serial Communication (SSC)

The 3-pin SSC interface consists of a bi-directional push-pull (tri-state on receive) or open-drain data pin (configurable with SSC_OD bit) and the serial clock and chip-select input pins. The SSC Interface is designed to communicate with a microcontroller peer-to-peer for fast applications.

4.4.2.1 SSC Timing Definition

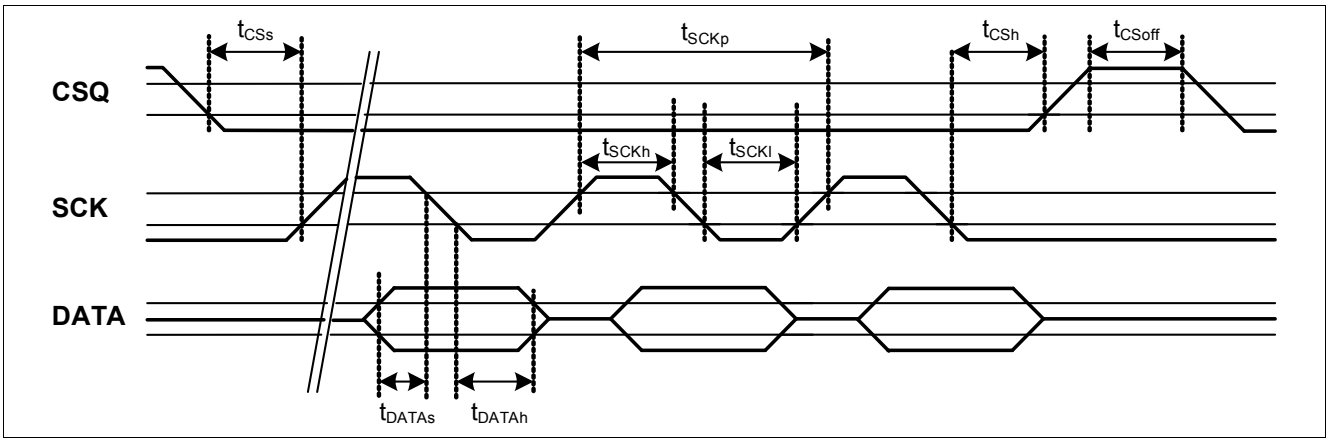

Figure 4-9 SSC timing

SSC Inactive Time (CS_{off})

The SSC inactive time defines the delay time after a transfer before the TLI5012B E1000 can be selected again.

Table 4-14 SSC push-pull timing specification

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SSC baud rate	f_{SSC}		8.0		Mbit/s	1)
CSQ setup time	t_{CSs}	105			ns	1)
CSQ hold time	t_{CSh}	105			ns	1)
CSQ off	t_{CSoff}	600			ns	SSC inactive time 1)
SCK period	t_{SCKp}	120	125		ns	1)
SCK high	t_{SCKh}	40			ns	1)
SCK low	t_{SCKl}	30			ns	1)
DATA setup time	t_{DATAs}	25			ns	1)
DATA hold time	t_{DATAh}	40			ns	1)
Write read delay	t_{wr_delay}	130			ns	1)
Update time	$t_{CSupdate}$	1			µs	See Figure 4-13 1)
SCK off	t_{SCKoff}	170			ns	1)

1) Not subject to production test - verified by design/characterization

Table 4-15 SSC open-drain timing specification

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SSC baud rate	f_{SSC}		2.0		Mbit/s	Pull-up Resistor = 1kΩ[1)]
CSQ setup time	t_{CSs}	300			ns	[1)]
CSQ hold time	t_{CSh}	400			ns	[1)]
CSQ off	t_{CSoff}	600			ns	SSC inactive time[1)]
SCK period	t_{SCKp}	500			ns	[1)]
SCK high	t_{SCKh}		190		ns	[1)]
SCK low	t_{SCKl}		190		ns	[1)]
DATA setup time	t_{DATAs}	25			ns	[1)]
DATA hold time	t_{DATAh}	40			ns	[1)]
Write read delay	t_{wr_delay}	130			ns	[1)]
Update time	$t_{CSupdate}$	1			µs	See Figure 4-13[1)]
SCK off	t_{SCKoff}	170			ns	[1)]

1) Not subject to production test - verified by design/characterization

4.4.2.2 SSC Data Transfer

The SSC data transfer is word-aligned. The following transfer words are possible:

- Command Word (to access and change operating modes of the TLI5012B E1000)
- Data words (any data transferred in any direction)
- Safety Word (confirms the data transfer and provides status information)

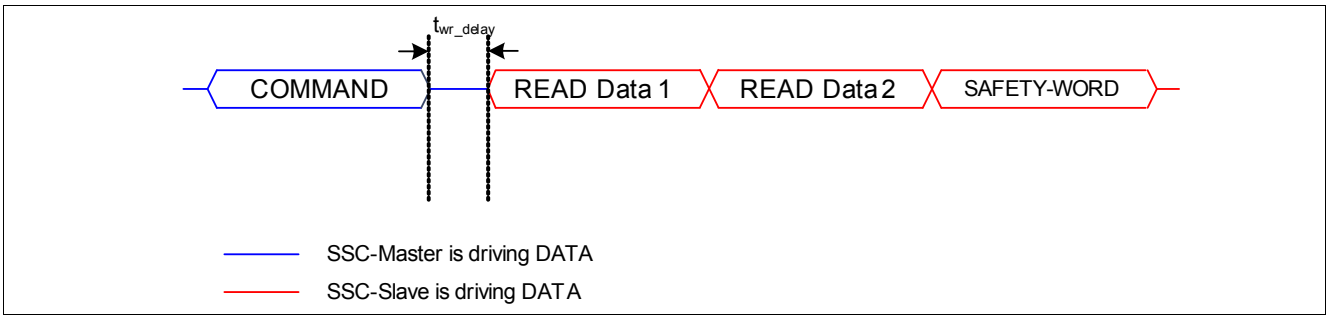

Figure 4-10 SSC data transfer (data-read example)

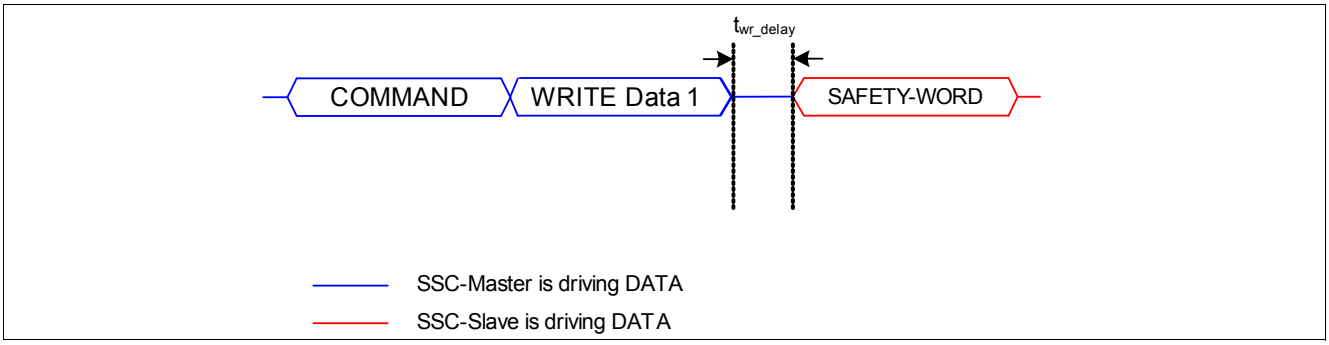

Figure 4-11 SSC data transfer (data-write example)

Command Word

SSC Communication between the TLI5012B E1000and a microcontroller is initiated by a command word. The structure of the command word is shown in **Table 4-16**. If an update is triggered by shortly pulling low CSQ without a clock on SCK a snapshot of all system values is stored in the update registers simultaneously. A read command with the UPD bit set then allows to readout this consistent set of values instead of the current values. Bits with an update buffer are marked by an “u” in the Type column in register descriptions.

Table 4-16 Structure of the Command Word

Name	Bits	Description
RW	[15]	Read - Write 0: Write 1: Read
Lock	[14..11]	4-bit Lock Value 0000_B: Default operating access for addresses 0x00:0x04 1010_B: Configuration access for addresses 0x05:0x11
UPD	[10]	Update-Register Access 0: Access to current values 1: Access to values in update buffer
ADDR	[9..4]	6-bit Address
ND	[3..0]	4-bit Number of Data Words

Safety Word

The safety word consists of the following bits:

Table 4-17 Structure of the Safety Word

Name	Bits	Description
STAT[1)]	Chip and Interface Status	
	[15]	Indication of chip reset or watchdog overflow (resets after readout) via SSC 0: Reset occurred 1: No reset
	[14]	System error (e.g. overvoltage; undervoltage; V_{DD}-, GND- off; ROM;...) 0: Error occurred (S_VR; S_DSPU; S_OV; S_XYOL: S_MAGOL; S_FUSE; S_ROM; S_ADCT) 1: No error
	[13]	Interface access error (access to wrong address; wrong lock) 0: Error occurred 1: No error
	[12]	Valid angle value (NO_GMR_A = 0; NO_GMR_XY = 0) 0: Angle value invalid 1: Angle value valid
RESP	[11..8]	Sensor number response indicator The sensor number bit is pulled low and the other bits are high
CRC	[7..0]	Cyclic Redundancy Check (CRC)

1) When an error occurs, the corresponding status bit in the safety word remains “low” until the STAT register (address 00_H) is read via SSC interface.

Bit Types

The types of bits used in the registers are listed here:

Table 4-18 Bit Types

Abbreviation	Function	Description
r	Read	Read-only registers
w	Write	Read and write registers
u	Update	Update buffer for this bit is present. If an update is issued and the Update-Register Access bit (UPD in Command Word) is set, the immediate values are stored in this update buffer simultaneously. This allows a snapshot of all necessary system parameters at the same time.

Data communication via SSC

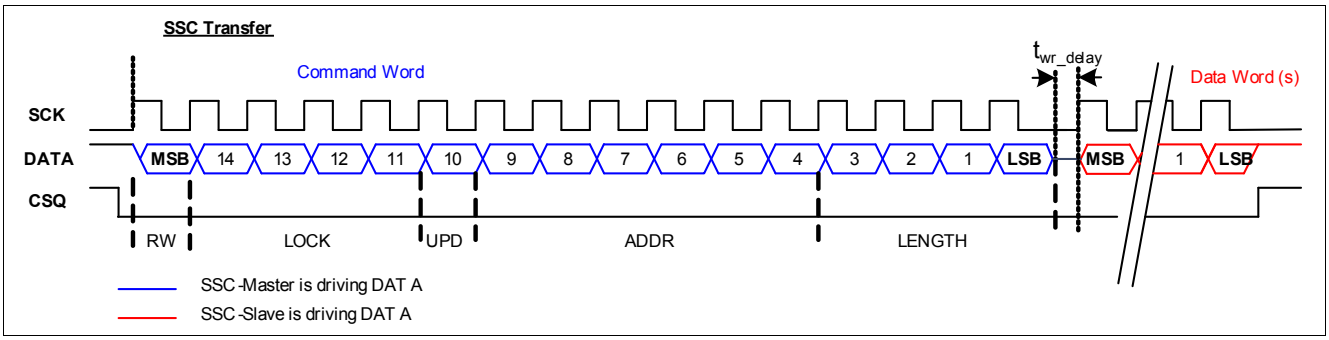

Figure 4-12 SSC bit ordering (read example)

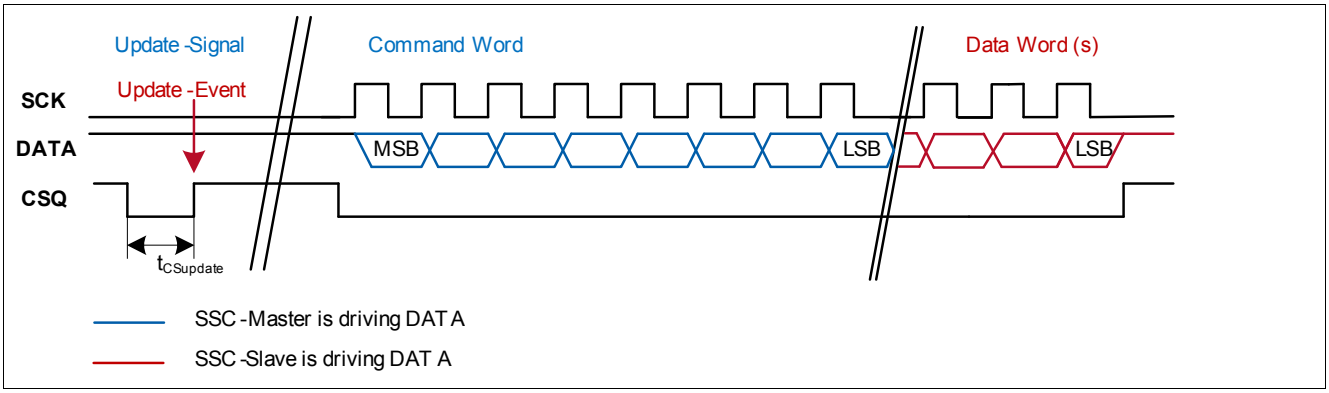

Figure 4-13 Update of update registers

The data communication via SSC interface has the following characteristics:

- The data transmission order is Most-Significant Bit (MSB) first, Last-Significant Bit (LSB) last.
- Data is put on the data line with the rising edge on SCK and read with the falling edge on SCK.
- The SSC Interface is word-aligned. All functions are activated after each transmitted word.
- After every data transfer with ND ≥ 1, the 16-bit Safety Word is appended by the TLI5012B E1000.
- A “high” condition on the Chip Select pin (CSQ) of the selected TLI5012B E1000 interrupts the transfer immediately. The CRC calculator is automatically reset.
- After changing the data direction, a delay t_{wr_delay} (see **Table 4-15**) has to be implemented before continuing the data transfer. This is necessary for internal register access.
- If in the Command Word the number of data is greater than 1 (ND > 1), then a corresponding number of consecutive registers is read, starting at the address given by ADDR.

- In case an overflow occurs at address $3F_H$, the transfer continues at address 00_H.
- If in the Command Word the number of data is zero (ND = 0), the register at the address given by ADDR is read, but no Safety Word is sent by the TLI5012B E1000. This allows a fast readout of one register.
- At a rising edge of CSQ without a preceding data transfer (no SCK pulse, see **Figure 4-13**), the content of all registers which have an update buffer is saved into the buffer. This procedure serves to take a snapshot of all relevant sensor parameters at a given time. The content of the update buffer can then be read by sending a read command for the desired register and setting the UPD bit of the Command Word to “1”.
- After sending the Safety Word, the transfer ends. To start another data transfer, the CSQ has to be deselected once for at least t_{CSoff}.
- By default, the SSC interface is set to push-pull. The push-pull driver is active only if the TLI5012B E1000 has to send data, otherwise the DATA pin is set to high-impedance.

Cyclic Redundancy Check (CRC)

- This CRC is according to the J1850 Bus Specification.
- Every new transfer restarts the CRC generation.
- Every Byte of a transfer will be taken into account to generate the CRC (also the sent command(s)).
- Generator polynomial: X8+X4+X3+X2+1, but for the CRC generation the fast-CRC generation circuit is used (see **Figure 4-14**)
- The seed value of the fast CRC circuit is ’11111111_B’.
- The remainder is inverted before transmission.

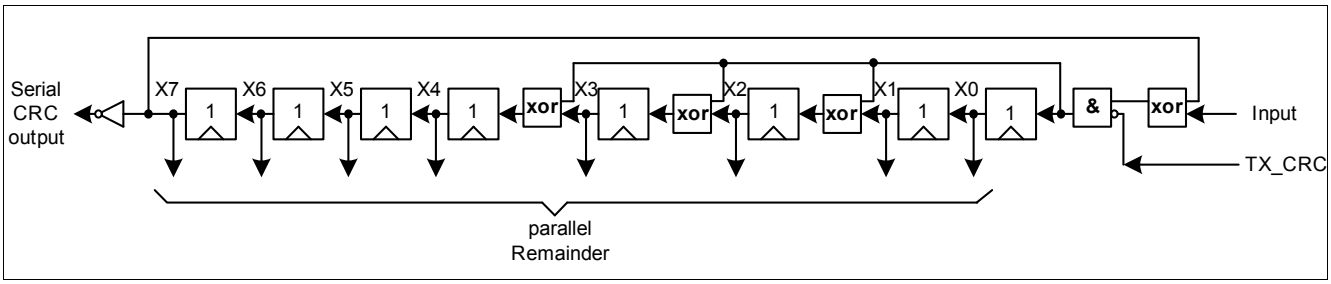

Figure 4-14 Fast CRC polynomial division circuit

4.4.3 Supply Monitoring

The internal voltage nodes of the TLI5012B E1000 are monitored by a set of comparators in order to ensure error-free operation. An over- or undervoltage condition must be active at least 256 periods of the digital clock to set the corresponding error bits in the Status register. This works as digital spike suppression.

Over- or undervoltage errors trigger the S_VR bit of Status register. This error condition is signaled via the in the Safety Word of the SSC protocol, the status nibble of the SPC interface or the lower diagnostic range of the PWM interface.

Table 4-19 Test comparator threshold voltages

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Overvoltage detection	V_{OVG}		2.80		V	1)
	V_{OVA}		2.80		V	1)
	V_{OVD}		2.80		V	1)
V_{DD} overvoltage	V_{DDOV}		6.05		V	1)
V_{DD} undervoltage	V_{DDUV}		2.70		V	1)
GND - off voltage	V_{GNDoff}		-0.55		V	1)
V_{DD} - off voltage	V_{VDDoff}		0.55		V	1)
Spike filter delay	t_{DEL}		10		µs	1)

1) Not subject to production test - verified by design/characterization

4.4.3.1 Internal Supply Voltage Comparators

Every voltage regulator has an overvoltage (OV) comparator to detect malfunctions. If the nominal output voltage of 2.5 V is larger than V_{OVG}, V_{OVA} and V_{OVD}, then this overvoltage comparator is activated.

4.4.3.2 V_{DD} Overvoltage Detection

The overvoltage detection comparator monitors the external supply voltage at the V_{DD} pin.

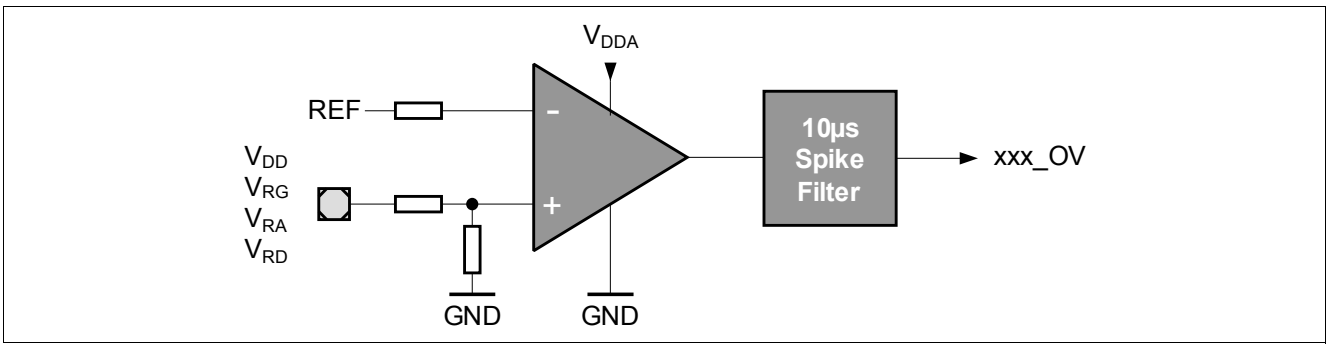

Figure 4-15 Overvoltage comparator

4.4.3.3 GND - Off Comparator

The GND - Off comparator is used to detect a voltage difference between the GND pin and SCK. This circuit can detect a disconnection of the supply GND Pin.

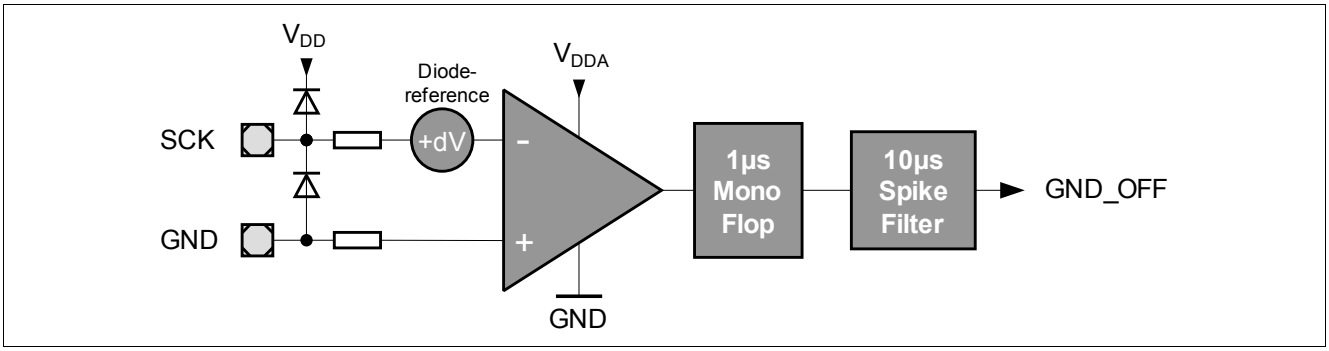

Figure 4-16 GND - off comparator

4.4.3.4 V_{DD} - Off Comparator

The V_{DD} - Off comparator detects a disconnection of the VDD pin supply voltage. In this case, the TLI5012B E1000 is supplied by the SCK and CSQ input pins via the ESD structures.

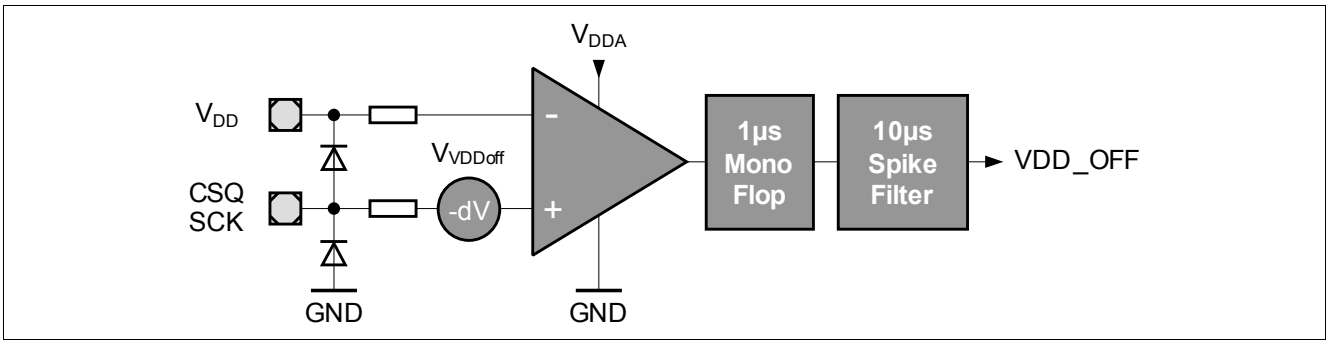

Figure 4-17 V_{DD} - off comparator

5 Package Information

5.1 Package Parameters

Table 5-1 Package Parameters

Parameter	Symbol	Limit Values			Unit	Notes
		Min.	Typ.	Max.		
Thermal resistance	R_{thJA}		150	200	K/W	Junction to air[1)]
	R_{thJC}			75	K/W	Junction to case
	R_{thJL}			85	K/W	Junction to lead
Soldering moisture level	MSL 3					260°C
Lead Frame	Cu					
Plating	Sn 100%					> 7 µm

1) according to Jedec JESD51-7

5.2 Package Outline

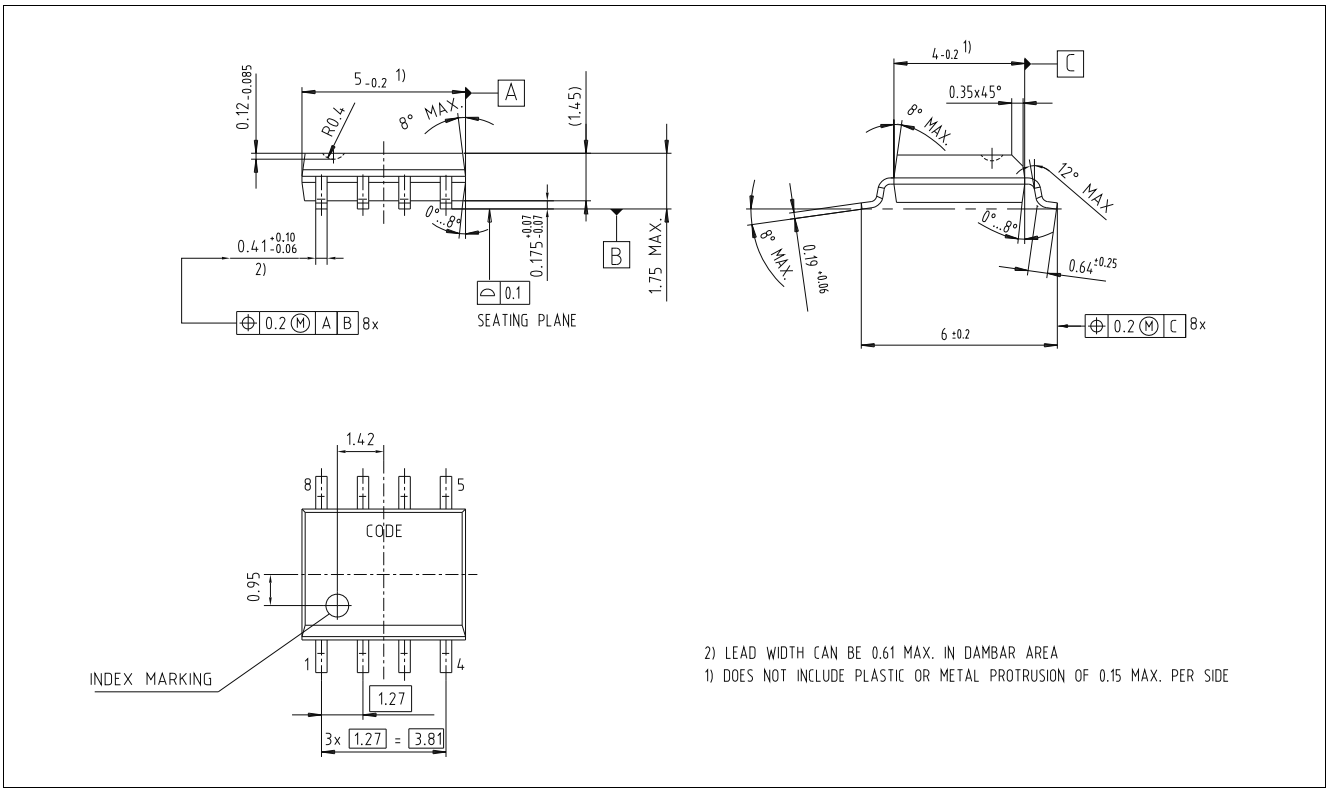

Figure 5-1 PG-DSO-8 package dimension

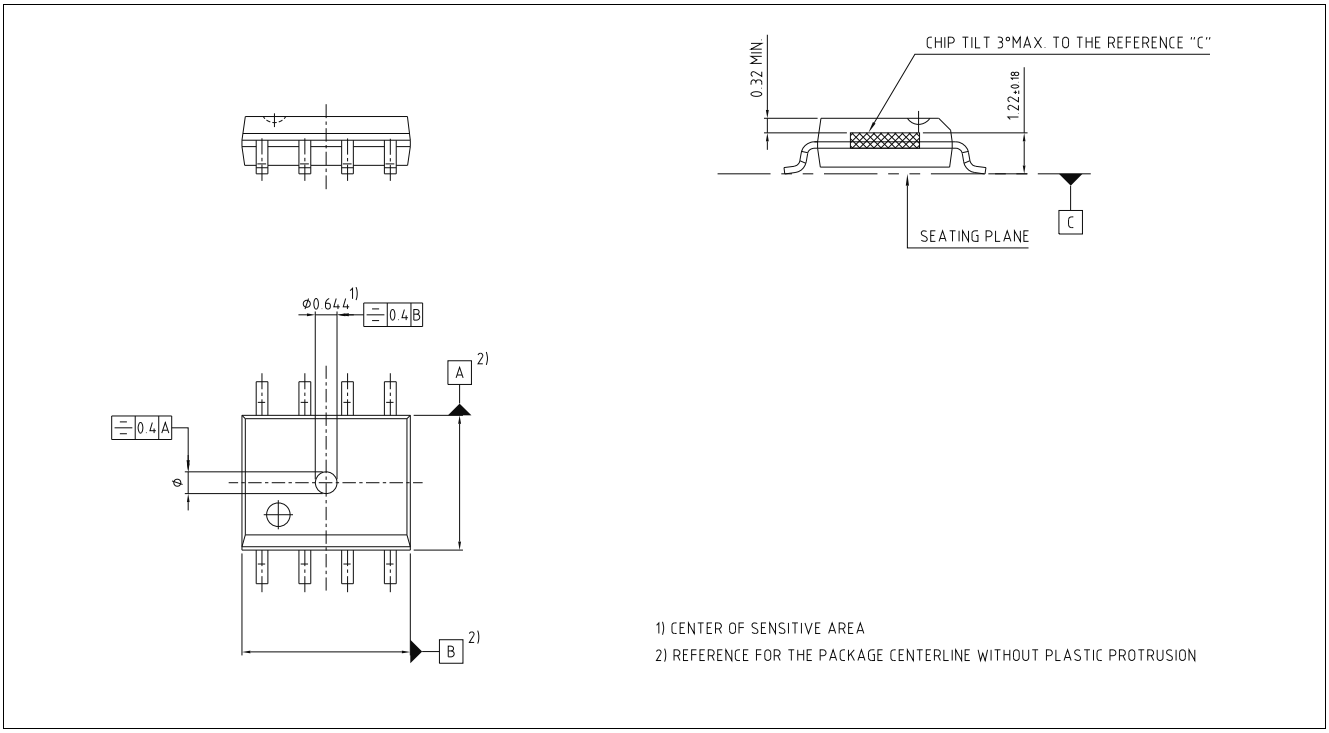

Figure 5-2 Position of sensing element

Table 5-2 Sensor IC placement tolerances in package

Parameter	Values		Unit	Notes
	Min.	Max.		
position eccentricity	-200	200	µm	in X- and Y-direction
rotation	-3	3	°	affects zero position offset of sensor
tilt	-3	3	°	

5.3 Footprint

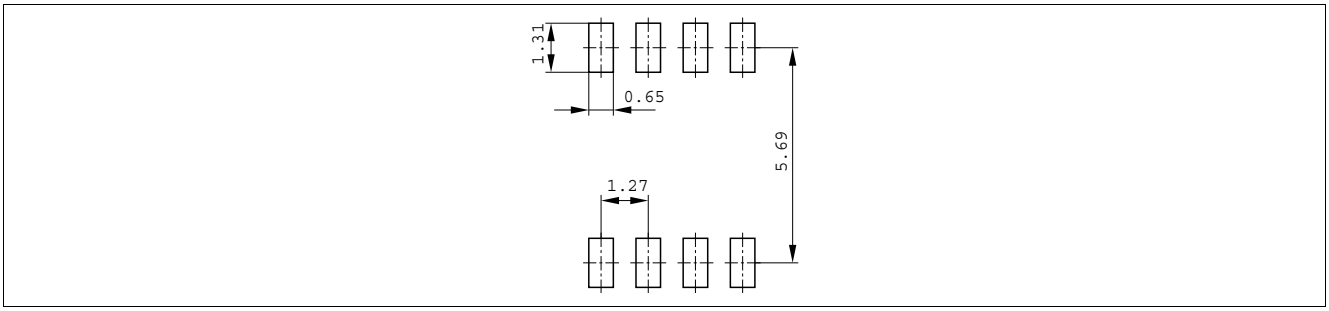

Figure 5-3 Footprint of PG-DSO-8

5.4 Packing

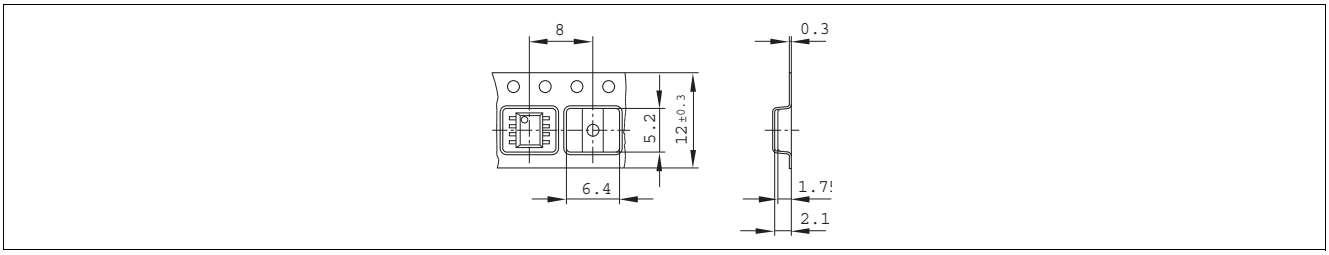

Figure 5-4 Tape and Reel

5.5 Marking

Position	Marking	Description
1st Line	I12B1000	See ordering table on **Page 8**
2nd Line	xxx	Lot code
3rd Line	Gxxxx	G..green, 4-digit..date code

Processing

Note: For processing recommendations, please refer to Infineon's Notes on processing

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