TPS74901EVM-210

This user's guide describes the characteristics, operation, and use of the TPS74901EVM-210 evaluation module (EVM). This EVM contains the TPS74901 low-dropout linear regulator IC. This document includes EVM specifications, recommended test setup, test results, bill of materials (BOM), and a schematic diagram.

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1 Introduction

The Texas Instruments TPS74901EVM-210 evaluation module uses the TPS74901 low-dropout linear regulator IC. These regulators require a low-power bias voltage, V_{BIAS}, and a power input voltage, V_{IN}. The regulator is capable of providing output voltages down to 0.8 V, output currents up to 3 A and has an integrated supervisory circuit with open-drain output that goes to high impedance when the output voltage reaches regulation (power good or PG). The goal of the EVM is to facilitate evaluation of the TPS74901 IC.

1.1 Performance Specification Summary

Table 1 provides a summary of the TPS74901EVM-210 performance specifications. All specifications are given for an ambient temperature of 25°C.

Table 1. Typical Performance Specification Summary

	CONDITION	VOLTAGE RANGE (V)			CURRENT RANGE (mA)		
		MIN	TYP	MAX	MIN	TYP	MAX
V_{BIAS} supply	I_O = 3 A and V_{IN} = V_{BIAS}	2.99 [1]	5	5.5		2000	
V_{IN} supply	I_O = 3 A and V_{BIAS} - V_O > 3.25 V	1.52 [1]		5.5 [2]			3000
V_{OUT}		1.16 [3]	1.20	1.24 [3]			3000 [2]

(1) This is the minimum voltage to provide the maximum output current in the table assuming the typical V_{BIAS} voltage is applied. Lower output currents are achievable with lower V_{IN} and V_{BIAS} voltages. See the data sheet for V_{IN} to V_{OUT} and V_{BIAS} to V_{OUT} dropout data.

(2) Linear regulator power dissipation is computed as $P_D = (V_{IN} - V_{OUT}) \times I_{OUT}$. As specified in the data sheet, the regulator's package has a finite power dissipation rating depending on the ambient temperature, board type, and airflow. Using V_{IN} and/or V_{OUT} voltages other than the typical voltages recommended in the table or using the EVM in an environment with an ambient temperature higher than 25°C significantly reduces the maximum allowed output current. See the data sheet for the regulator package's thermal resistance data, and see the application report *Digital Designer's Guide to Linear Voltage Regulators and Thermal Management* (SLVA118) for a full explanation.

(3) The EVM uses ±1% feedback resistors. Therefore, the EVM output tolerance is the ±2% internal reference tolerance plus $2 \times (1 - V_{REF}/V_{OUT}) \times TOL_{FBRES} = 2 \times (1 - 0.8V/1.2V) \times \pm 2\% = 1.3\%$ or ±3.3%. For tighter output tolerance, tighter tolerance feedback resistors must be used.

1.2 Modifications

To aid user customization of the EVM, the board was designed with devices having 0603 or larger footprints. A real implementation likely occupies less total board space.

Changing components can improve or degrade EVM performance. For example, adding a larger output capacitor reduces output voltage undershoot but lengthens response time after a load transient event.

2 Input/Output Connector Descriptions

J1–VIN/GND This terminal block has both a positive and ground return connection to the power input (V_{IN}) supply. The leads to the input supply should be twisted and kept as short as possible.

J2–GND This header is the return connection for the bias (V_{BIAS}) supply.

J3–VIN This header is a positive connection to the power input supply (V_{IN}). Its use is recommended for low power (i.e., $I_{IN} = I_{OUT} < 1$ A) evaluation or as a voltage test point.

J4–VBIAS This header is the positive connection for the bias (V_{BIAS}) supply.

J5–GND This header is a ground return connection to the power input (V_{IN}) supply. Its use is recommended for low power (i.e., $I_{IN} = I_{OUT} < 1$A) evaluation or as a ground test point.

J6–VOUT This header is the positive connection for the output load on V_{OUT}. Its use is recommended for low power (i.e., $I_{IN} = I_{OUT} < 1$ A) evaluation only or as a voltage test point.

J7–GND This header is the ground return connection for the output load. Its use is recommended for low power (i.e., $I_{IN} = I_{OUT} < 1$ A) evaluation or as a ground test point.

J8–VOUT/GND This terminal block has both a positive and ground return connection for the output load. The leads to the output load should be twisted and kept as short as possible.

JP1– EN When this jumper is installed, the enable pin (EN) is tied to VIN, thereby enabling the device. When this jumper is removed, EN is pulled to ground by resistor R4, thereby disabling the device.

S1 - This switch connects to the EN pin of the IC and allows the user to turn the IC ON or OFF by connecting enable to either V_{BIAS} or ground through a pulldown resistor.

TP1 – This is a Kelvin test point to V_{IN}.

TP2 – This is a Kelvin test point to IC ground.

TP3 – This is a Kelvin test point to V_{OUT}.

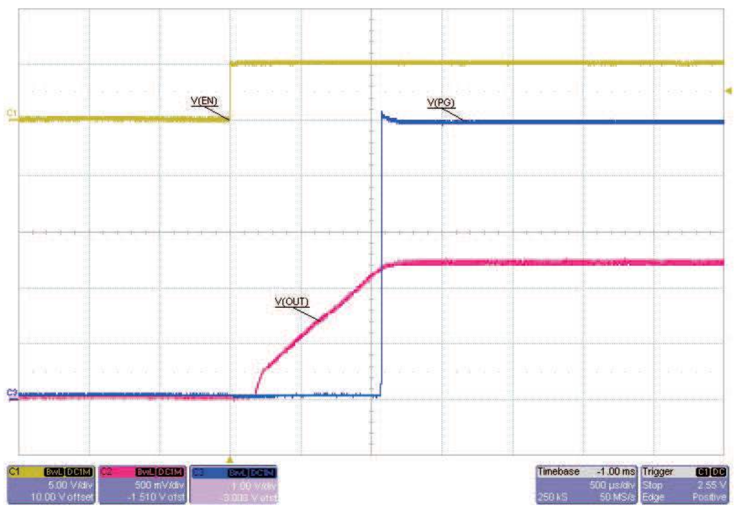
TP4 – This is a test point to measure the power good (PG) signal which is pulled up to V_{BIAS}.

2.1 Test Setup

The absolute maximum voltage allowed on the IN or EN pins is 6 V. The TPS74901 device is designed to operate with V_{IN} and V_{BIAS} less than or equal to 5.5 V. In order to enable the device, install jumper JP1. When connecting external loads above 1 A, use short, twisted leads connected to the screw terminals in order to minimize DC drop at the connector and/or inductive voltage dip after a transient load is removed.

2.2 Test Results

Figure 1 shows the test results at T_A = 25°C using this EVM:



A V_{IN} = 5 V, V_{BIAS} = 3.3 V, I_{OUT} = 1.5 A.

Figure 1. TPS74901 Start-up and PG

3 Board Layout

Board layout is critical for all switch-mode power supplies. Figure 2, Figure 3, and Figure 4 show the board layout for the HPA210 PWB. The switching nodes with high-frequency noise are isolated from the noise-sensitive feedback circuitry, and careful attention has been given to the routing of high-frequency current loops. See the data sheet for more specific layout guidelines.

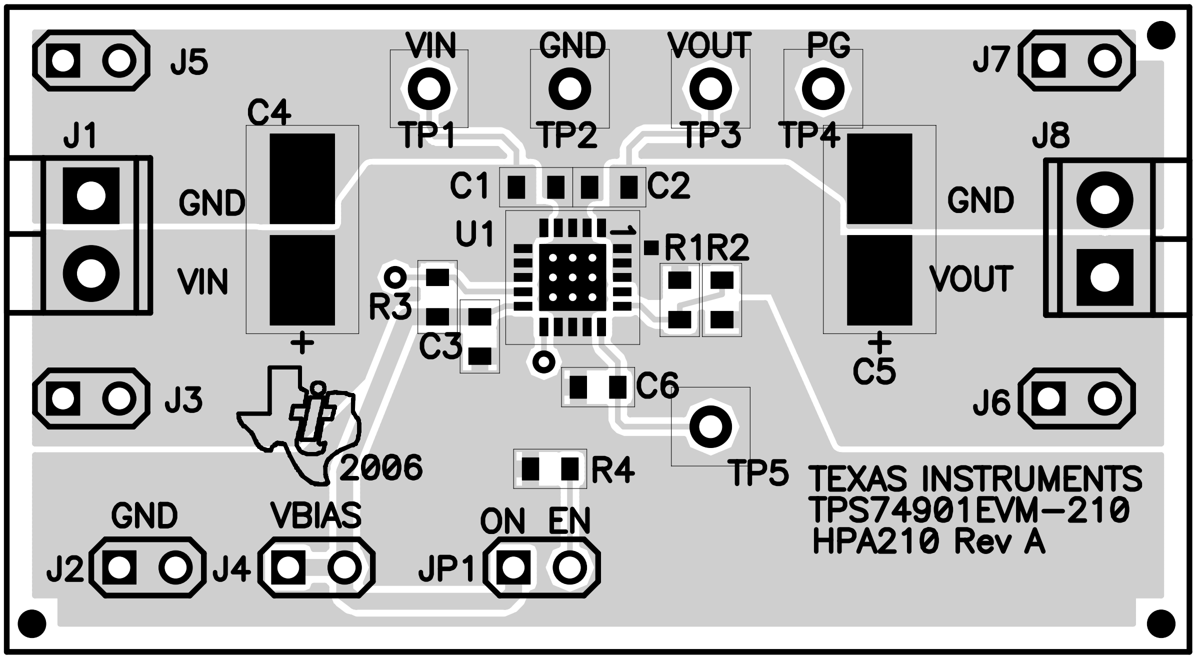


Figure 2. Top Assembly Layer

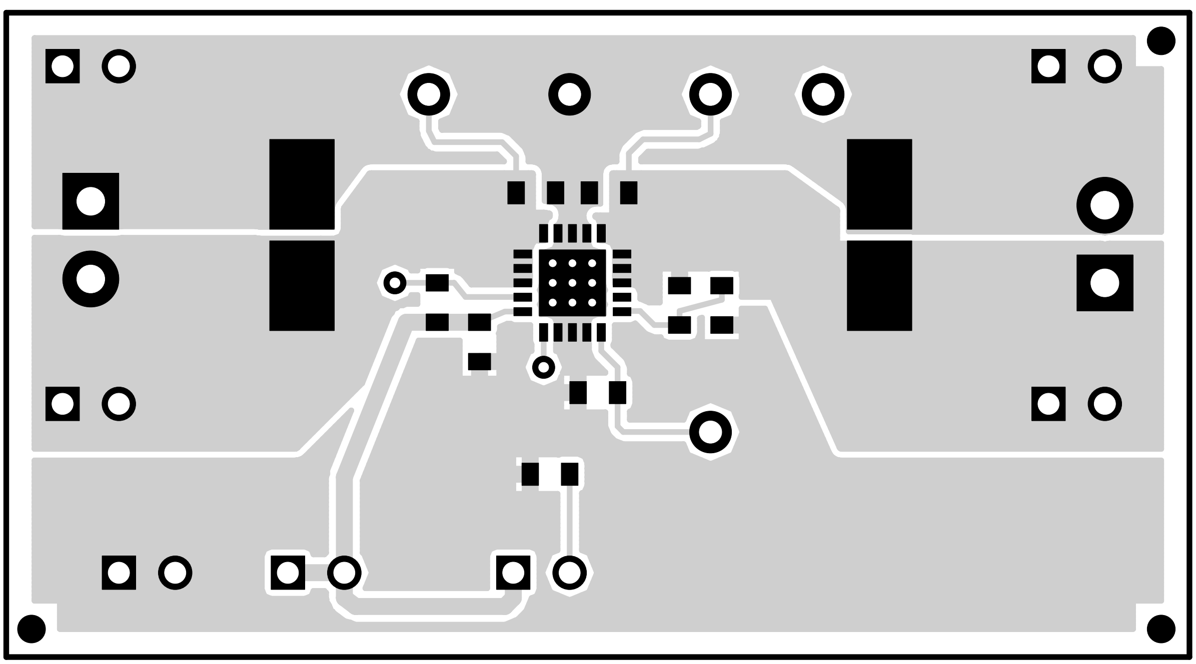


Figure 3. Top Layer

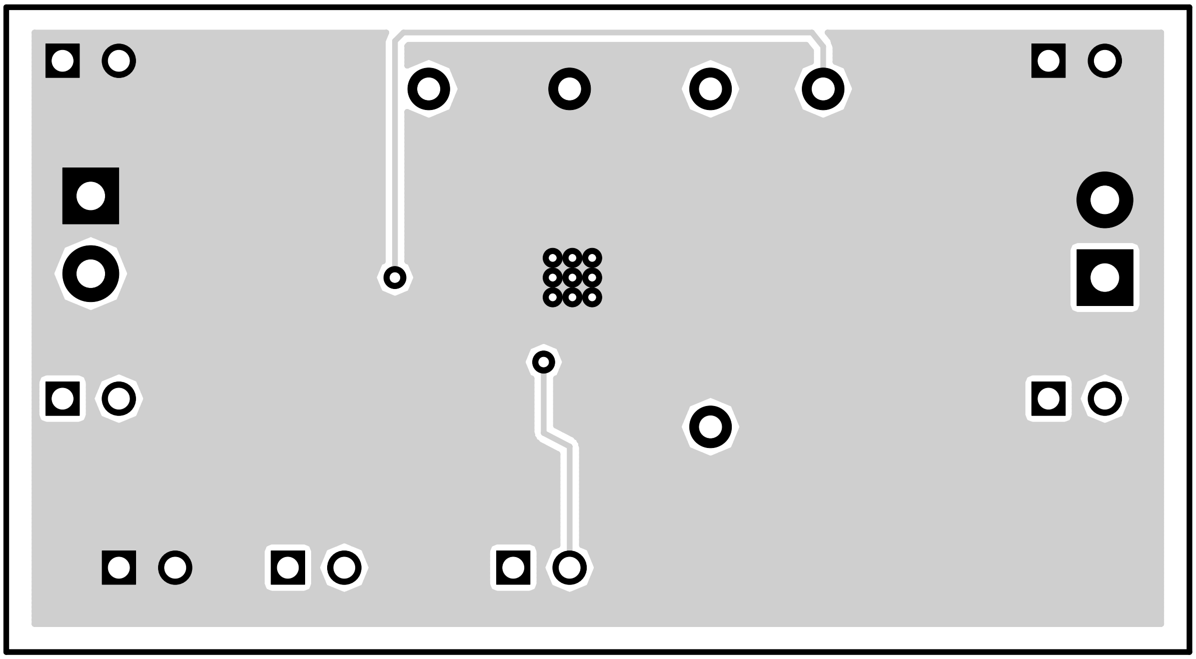


Figure 4. Bottom Layer

4 Bill of Materials and Schematic

4.1 Bill of Materials

Table 2. HPA210 Bill of Materials

Count	Reference Designator	Value	Description	Size	Part Number	MFR
1	C1	1.0 µF	Capacitor, Ceramic, 25V, X5R, 10%	0603	C1608X5R1E105K	TDK
1	C2	2.2 µF	Capacitor, Ceramic, 6.3V, X5R, 20%	0603	C1608X5R0J225M	TDK
1	C3	1.0 µF	Capacitor, Ceramic, 10V, X5R,10%	0603	C1608X5R1A105K	TDK
0	C4, C5	Open	Capacitor, Multi-pattern, 603-D case	7343 (D)		
1	C6	560 pF	Capacitor, Ceramic, 50V, C0G, 5%	0603	C1608C0G1H561J	TDK
2	J1, J8		Terminal Block, 2 pin, 6A, 3.5mm	0.27 x 0.25	ED1514	OST
6	J2 - J7		Header, 2 pin, 100mil spacing, (36-pin strip)	0.100 x 2	PTC36SAAN	Sullins
1	JP1		Header, 2 pin, 100mil spacing, (36-pin strip)	0.100 x 2	PTC36SAAN	Sullins
1	R1	2.49 kΩ	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R2	2.49 kΩ	Resistor, Chip, 1/16W, 1%	0603	Std	Std
2	R3, R4	100 kΩ	Resistor, Chip, 1/16W, 1%	0603	Std	Std
4	TP1 - TP4		Test Point, Red, Thru Hole Color Keyed	0.100 x 0.100	5000	Keystone
0	TP5		Test Point, Red, Thru Hole Color Keyed	0.100 x 0.100		
1	U1		IC, 3A LDO With Low Dropout	QFN-20	TPS74901RGW	TI
1	–		PCB, 2.1 In x 1.145 In x 0.062 In		HPA210	Any
1	–		Shunt, 100mil, Black	0.100	929950-00	3M

4.2 Schematic Drawing

Figure 5 is the schematic for the TPS74901EVM-210.

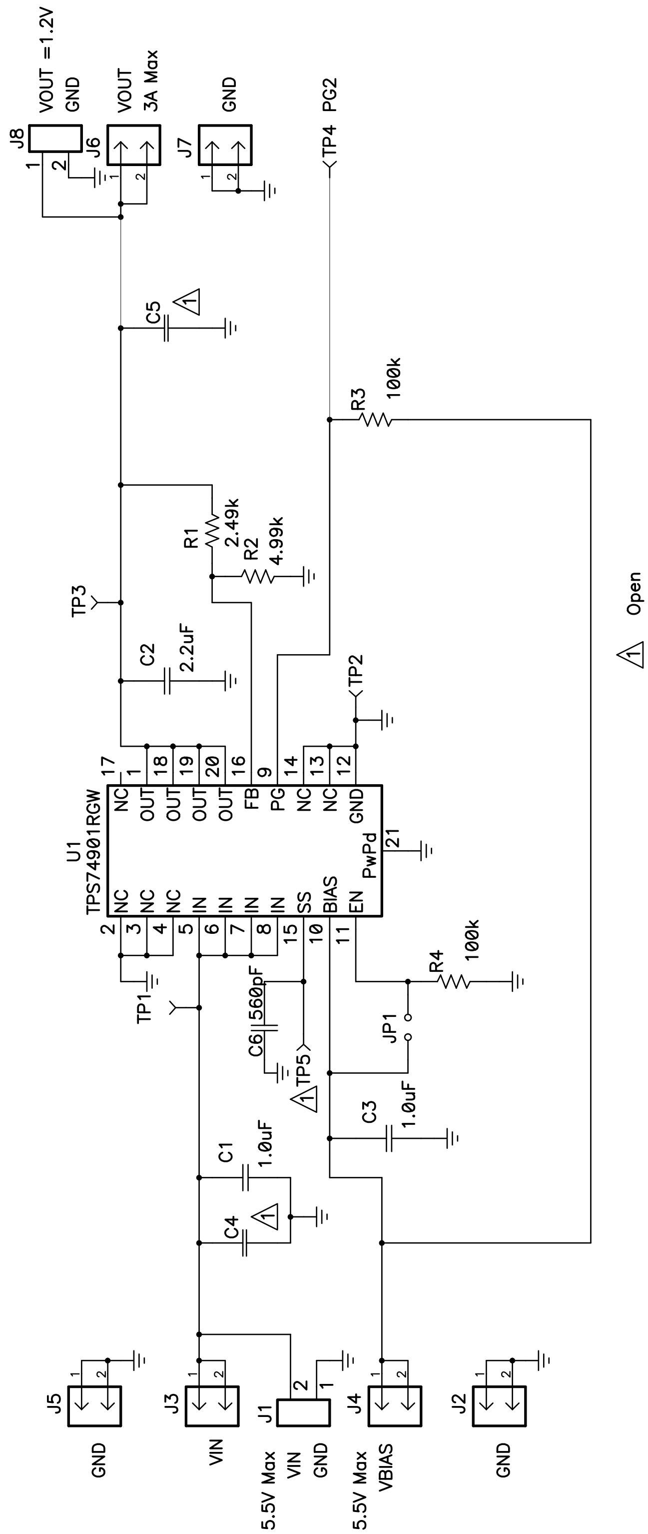


Figure 5. Schematic

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of 3 V to 5 V and the output voltage range of 3 V to 3.3 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 25°C. The EVM is designed to operate properly with certain components above 25°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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