LM2717 Dual Step-Down DC/DC Converter

Check for Samples: LM2717

FEATURES

- **Fixed 3.3V Output Buck Converter with a 2.2A, 0.16Ω, Internal Switch**
- **Adjustable Buck Converter with a 3.2A, 0.16Ω, Internal Switch**
- **Operating Input Voltage Range of 4V to 20V**
- **Input Undervoltage Protection**
- **300kHz to 600kHz Pin Adjustable Operating Frequency**
- **Over Temperature Protection**
- **Small 24-Lead TSSOP Package**

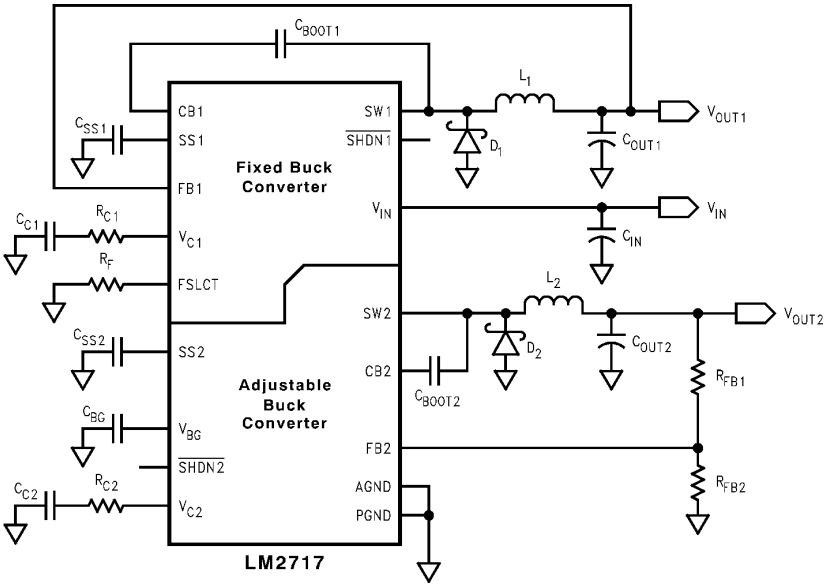
APPLICATIONS

- **TFT-LCD Displays**
- **Handheld Devices**
- **Portable Applications**
- **Laptop Computers**

DESCRIPTION

The LM2717 is composed of two PWM DC/DC buck (step-down) converters. The first converter is used to generate a fixed output voltage of 3.3V. The second converter is used to generate an adjustable output voltage. Both converters feature low R_{DSON} (0.16Ω) internal switches for maximum efficiency. Operating frequency can be adjusted anywhere between 300kHz and 600kHz allowing the use of small external components. External soft-start pins for each enables the user to tailor the soft-start times to a specific application. Each converter may also be shut down independently with its own shutdown pin. The LM2717 is available in a low profile 24-lead TSSOP package ensuring a low profile overall solution.

Typical Application Circuit



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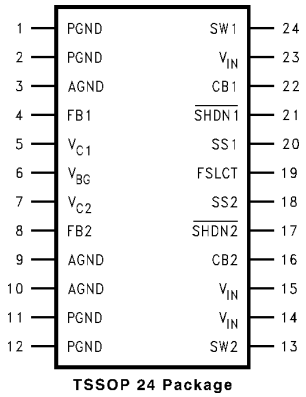
Connection Diagram

Top View



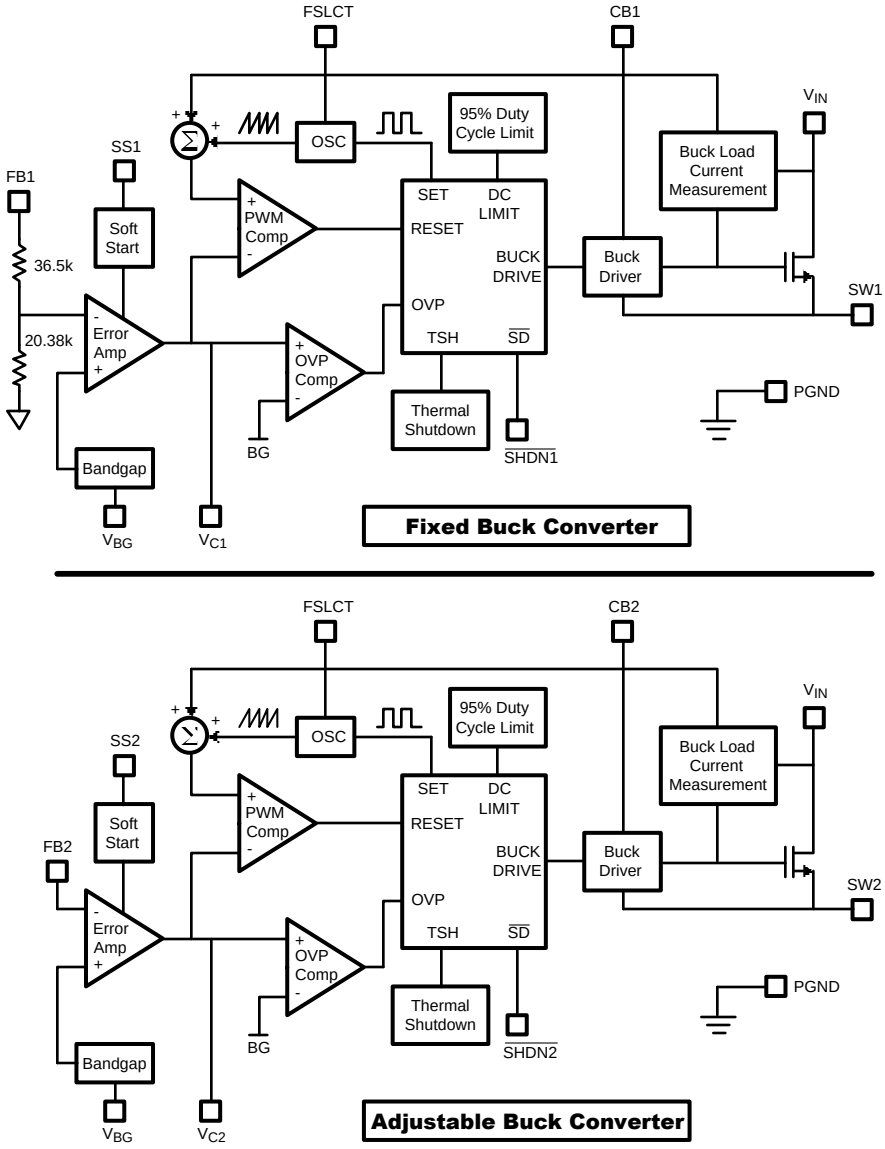
TSSOP 24 Package

Figure 1. 24-Lead TSSOP
See Package Number PW0024A

PIN DESCRIPTIONS

Pin	Name	Function
1	PGND	Power ground. PGND and AGND pins must be connected together directly at the part.
2	PGND	Power ground. PGND and AGND pins must be connected together directly at the part.
3	AGND	Analog ground. PGND and AGND pins must be connected together directly at the part.
4	FB1	Fixed buck output voltage feedback input.
5	V_{C1}	Fixed buck compensation network connection. Connected to the output of the voltage error amplifier.
6	V_{BG}	Bandgap connection.
7	V_{C2}	Adjustable buck compensation network connection. Connected to the output of the voltage error amplifier.
8	FB2	Adjustable buck output voltage feedback input.
9	AGND	Analog ground. PGND and AGND pins must be connected together directly at the part.
10	AGND	Analog ground. PGND and AGND pins must be connected together directly at the part.
11	PGND	Power ground. PGND and AGND pins must be connected together directly at the part.
12	PGND	Power ground. PGND and AGND pins must be connected together directly at the part.
13	SW2	Adjustable buck power switch input. Switch connected between V_{IN} pins and SW2 pin.
14	V_{IN}	Analog power input. V_{IN} pins should be connected together directly at the part.
15	V_{IN}	Analog power input. V_{IN} pins should be connected together directly at the part.
16	CB2	Adjustable buck converter bootstrap capacitor connection.
17	$\overline{SHDN2}$	Shutdown pin for adjustable buck converter. Active low.
18	SS2	Adjustable buck soft start pin.
19	FSLCT	Switching frequency select input. Use a resistor to set the frequency anywhere between 300kHz and 600kHz.
20	SS1	Fixed buck soft start pin.
21	$\overline{SHDN1}$	Shutdown pin for fixed buck converter. Active low.
22	CB1	Fixed buck converter bootstrap capacitor connection.
23	V_{IN}	Analog power input. V_{IN} pins should be connected together directly at the part.
24	SW1	Fixed buck power switch input. Switch connected between V_{IN} pins and SW1 pin.

Block Diagram



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings[1][2]

V_{IN}		−0.3V to 22V
SW1 Voltage		−0.3V to 22V
SW2 Voltage		−0.3V to 22V
FB1, FB2 Voltages		−0.3V to 7V
CB1, CB2 Voltages		−0.3V to V_{IN}+7V (V_{IN}=V_{SW})
V_{C1} Voltage		1.75V ≤ V_{C1} ≤ 2.25V
V_{C2} Voltage		0.965V ≤ V_{C2} ≤ 1.565V
$\overline{SHDN1}$ Voltage		−0.3V to 7.5V
$\overline{SHDN2}$ Voltage		−0.3V to 7.5V
SS1 Voltage		−0.3V to 2.1V
SS2 Voltage		−0.3V to 2.1V
FSLCT Voltage		AGND to 5V
Maximum Junction Temperature		150°C
Power Dissipation[3]		Internally Limited
Lead Temperature		300°C
Vapor Phase (60 sec.)		215°C
Infrared (15 sec.)		220°C
ESD Susceptibility[4]	Human Body Model	2kV

(1) Absolute maximum ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions for which the device is intended to be functional, but device parameter specifications may not be ensured. For ensured specifications and test conditions, see the Electrical Characteristics.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J(MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. See the Electrical Characteristics table for the thermal resistance. The maximum allowable power dissipation at any ambient temperature is calculated using: P_D (MAX) = ($T_{J(MAX)}$ − T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown.
(4) The human body model is a 100 pF capacitor discharged through a 1.5kΩ resistor into each pin.

Operating Conditions

Operating Junction Temperature Range[1]	−40°C to +125°C
Storage Temperature	−65°C to +150°C
Supply Voltage	4V to 20V
SW1 Voltage	20V
SW2 Voltage	20V

(1) All limits specified at room temperature (standard typeface) and at temperature extremes (bold typeface). All room temperature limits are 100% tested or ensured through statistical analysis. All limits at temperature extremes are specified via correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).

Electrical Characteristics

Specifications in standard type face are for T_J = 25°C and those with **boldface type** apply over the full **Operating Temperature Range** (T_J = −40°C to +125°C). V_{IN} = 5V, I_L = 0A, and F_{SW} = 300kHz unless otherwise specified.

Symbol	Parameter	Conditions	Min[1]	Typ[2]	Max[1]	Units
I_Q	Total Quiescent Current (both switchers)	Not Switching		2.7	**6**	mA
		Switching, switch open		6	**12**	mA
		$V_{\overline{SHDN}}$ = 0V		9	**27**	µA
V_{FB1}	Fixed Buck Feedback Voltage			3.3		V
V_{FB2}	Adjustable Buck Feedback Voltage			1.267		V

(1) All limits specified at room temperature (standard typeface) and at temperature extremes (bold typeface). All room temperature limits are 100% tested or ensured through statistical analysis. All limits at temperature extremes are specified via correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).
(2) Typical numbers are at 25°C and represent the most likely norm.

Electrical Characteristics (continued)

Specifications in standard type face are for T_J = 25°C and those with **boldface type** apply over the full **Operating Temperature Range** (T_J = −40°C to +125°C). V_{IN} = 5V, I_L = 0A, and F_{SW} = 300kHz unless otherwise specified.

Symbol	Parameter	Conditions	Min(1)	Typ(2)	Max(1)	Units
I_{CL1}(3)	Fixed Buck Switch Current Limit	V_{IN} = 8V(4)		2.2		A
I_{CL2}(3)	Adjustable Buck Switch Current Limit	V_{IN} = 8V(4)		3.2		A
I_{B1}	Fixed Buck FB Pin Bias Current(5)	V_{IN} = 20V		65		µA
I_{B2}	Adjustable Buck FB Pin Bias Current(5)	V_{IN} = 20V		65		nA
V_{IN}	Input Voltage Range		**4**		**20**	V
g_{m1}	Fixed Buck Error Amp Transconductance	ΔI = 20µA		1340		µmho
g_{m2}	Adjustable Buck Error Amp Transconductance	ΔI = 20µA		1360		µmho
A_{V1}	Fixed Buck Error Amp Voltage Gain			134		V/V
A_{V2}	Adjustable Buck Error Amp Voltage Gain			136		V/V
D_{MAX}	Maximum Duty Cycle		**89**	93		%
F_{SW}	Switching Frequency	R_F = 46.4k	**200**	300	**400**	kHz
		R_F = 22.6k	**475**	600	**775**	kHz
$I_{\overline{SHDN1}}$	Fixed Buck Shutdown Pin Current	0V < $V_{\overline{SHDN1}}$ < 7.5V	**−5**		**5**	µA
$I_{\overline{SHDN2}}$	Adjustable Buck Shutdown Pin Current	0V < $V_{\overline{SHDN2}}$ < 7.5V	**−5**		**5**	µA
I_{L1}	Fixed Buck Switch Leakage Current	V_{IN} = 20V		0.01	**5**	µA
I_{L2}	Adjustable Buck Switch Leakage Current	V_{IN} = 20V		0.01	**5**	µA
R_{DSON1}	Fixed Buck Switch R_{DSON}(6)			160		mΩ
R_{DSON2}	Adjustable Buck Switch R_{DSON}(6)			160		mΩ
$Th_{\overline{SHDN1}}$	Fixed Buck $\overline{SHDN}$ Threshold	Output High	**1.8**	1.36		V
		Output Low		1.33	**0.7**	
$Th_{\overline{SHDN2}}$	Adjustable Buck $\overline{SHDN}$ Threshold	Output High	**1.8**	1.36		V
		Output Low		1.33	**0.7**	
I_{SS1}	Fixed Buck Soft Start Pin Current		**4**	9	**15**	µA
I_{SS2}	Adjustable Buck Soft Start Pin Current		**4**	9	**15**	µA
UVP	On Threshold		**4**	3.8		V
	Off Threshold			3.6	**3.3**	
θ_{JA}	Thermal Resistance(7)	TSSOP, package only		115		°C/W

(3) Duty cycle affects current limit due to ramp generator.
(4) Current limit at 0% duty cycle. See *TYPICAL PERFORMANCE* section for Switch Current Limit vs. V_{IN}
(5) Bias current flows into FB pin.
(6) Includes the bond wires, R_{DSON} from V_{IN} pin(s) to SW pin.
(7) Refer to Texas Instruments packaging website for more detailed thermal information and mounting techniques for the TSSOP package.

Typical Performance Characteristics

Shutdown I_Q vs. Input Voltage

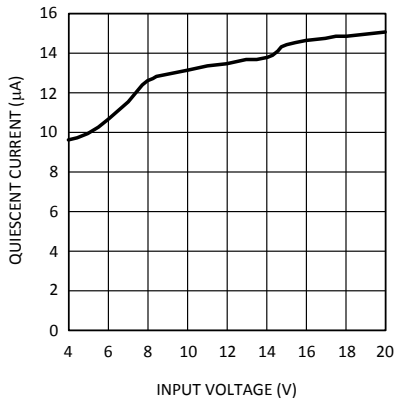


Figure 2.

Switching I_Q vs. Input Voltage (F_{SW} = 300kHz)

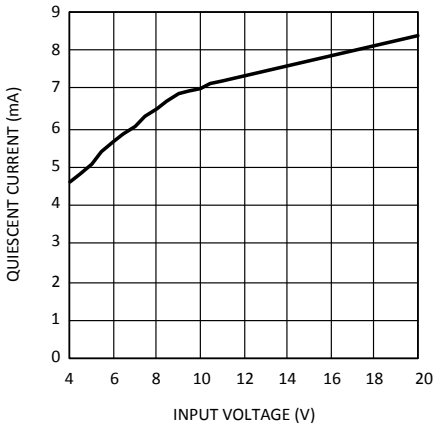


Figure 3.

Switching Frequency vs. Input Voltage (F_{SW} = 300kHz)

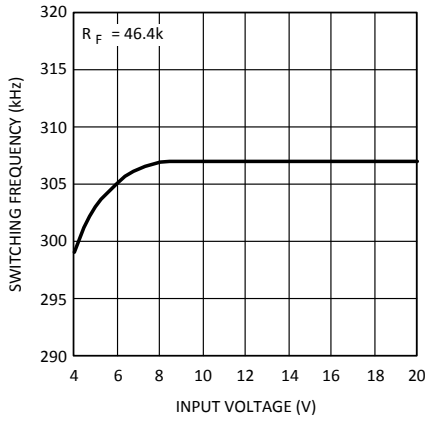


Figure 4.

Fixed Buck $R_{DS(ON)}$ vs. Input Voltage

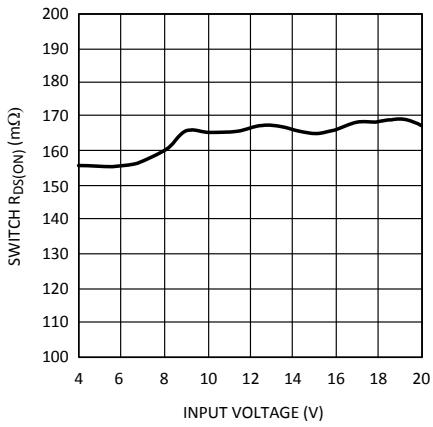


Figure 5.

Adjustable Buck $R_{DS(ON)}$ vs. Input Voltage

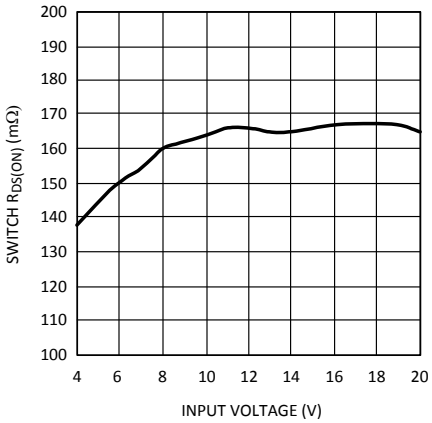


Figure 6.

Fixed Buck Efficiency vs. Load Current

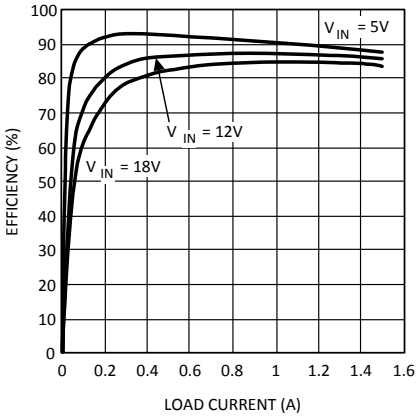


Figure 7.

Typical Performance Characteristics (continued)

Adjustable Buck Efficiency vs. Load Current (V_{OUT} = 15V)

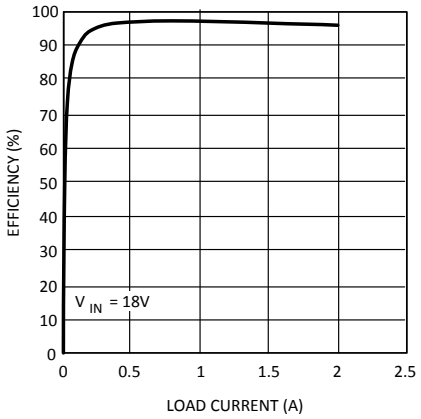


Figure 8.

Adjustable Buck Efficiency vs. Load Current (V_{OUT} = 5V)

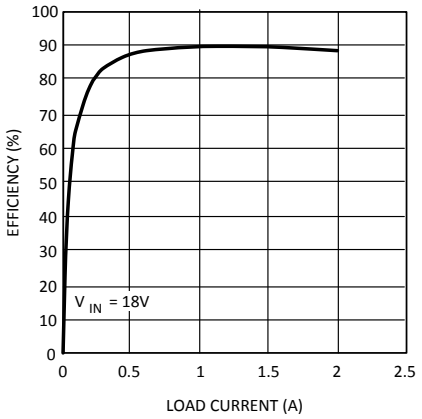


Figure 9.

Fixed Buck Switch Current Limt vs. Input Voltage

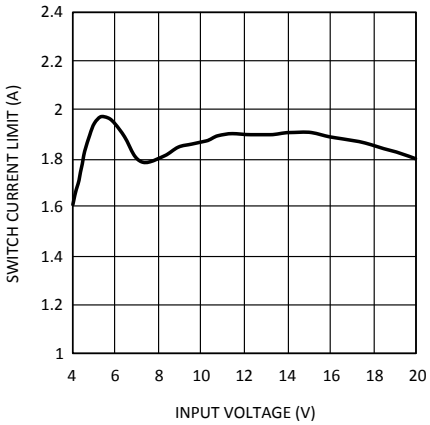


Figure 10.

Adjustable Buck Switch Current Limt vs. Input Voltage (V_{OUT} = 5V)

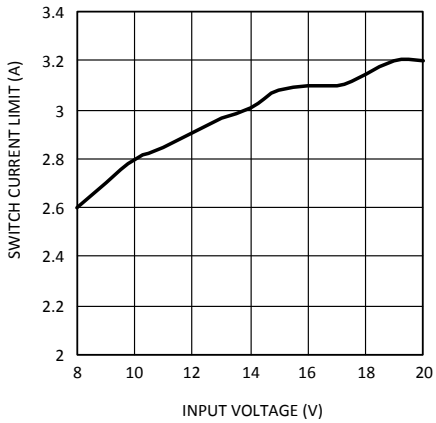


Figure 11.

BUCK OPERATION

PROTECTION (BOTH REGULATORS)

The LM2717 has dedicated protection circuitry running during normal operation to protect the IC. The Thermal Shutdown circuitry turns off the power devices when the die temperature reaches excessive levels. The UVP comparator protects the power devices during supply power startup and shutdown to prevent operation at voltages less than the minimum input voltage. The OVP comparator is used to prevent the output voltage from rising at no loads allowing full PWM operation over all load conditions. The LM2717 also features a shutdown mode for each converter decreasing the supply current to approximately 10µA (both in shutdown mode).

CONTINUOUS CONDUCTION MODE

The LM2717 contains current-mode, PWM buck regulators. A buck regulator steps the input voltage down to a lower output voltage. In continuous conduction mode (when the inductor current never reaches zero at steady state), the buck regulator operates in two cycles. The power switch is connected between V_{IN} and SW1 and SW2.

In the first cycle of operation the transistor is closed and the diode is reverse biased. Energy is collected in the inductor and the load current is supplied by C_{OUT} and the rising current through the inductor.

During the second cycle the transistor is open and the diode is forward biased due to the fact that the inductor current cannot instantaneously change direction. The energy stored in the inductor is transferred to the load and output capacitor.

The ratio of these two cycles determines the output voltage. The output voltage is defined approximately as:

$$D = \frac{V_{OUT}}{V_{IN}}, \; D' = (1-D) \tag{1}$$

where D is the duty cycle of the switch, D and D′ will be required for design calculations.

DESIGN PROCEDURE

This section presents guidelines for selecting external components.

SETTING THE OUTPUT VOLTAGE (ADJUSTABLE REGULATOR)

The output voltage is set using the feedback pin and a resistor divider connected to the output as shown in Figure 12. The feedback pin voltage is 1.26V, so the ratio of the feedback resistors sets the output voltage according to the following equation:

$$R_{FB1} = R_{FB2} \times \frac{V_{OUT} - 1.267}{1.267} \Omega \tag{2}$$

INPUT CAPACITOR

A low ESR aluminum, tantalum, or ceramic capacitor is needed betwen the input pin and power ground. This capacitor prevents large voltage transients from appearing at the input. The capacitor is selected based on the RMS current and voltage requirements. The RMS current is given by:

$$I_{RMS} = I_{OUT} \times \frac{\sqrt{V_{OUT}(V_{IN} - V_{OUT})}}{V_{IN}} \tag{3}$$

The RMS current reaches its maximum ($I_{OUT}/2$) when V_{IN} equals $2V_{OUT}$. This value should be calculated for both regulators and added to give a total RMS current rating. For an aluminum or ceramic capacitor, the voltage rating should be at least 25% higher than the maximum input voltage. If a tantalum capacitor is used, the voltage rating required is about twice the maximum input voltage. The tantalum capacitor should be surge current tested by the manufacturer to prevent being shorted by the inrush current. The minimum capacitor value should be 47µF for lower output load current applications and less dynamic (quickly changing) load conditions. For higher output current applications or dynamic load conditions a 68µF to 100µF low ESR capacitor is recommended. It is also recommended to put a small ceramic capacitor (0.1µF to 4.7µF) between the input pins and ground to reduce high frequency spikes.

INDUCTOR SELECTION

The most critical parameters for the inductor are the inductance, peak current and the DC resistance. The inductance is related to the peak-to-peak inductor ripple current, the input and the output voltages (for 300kHz operation):

$$L = \frac{(V_{IN} - V_{OUT}) V_{OUT}}{V_{IN} \times I_{RIPPLE} \times 300\ kHz} \quad (4)$$

A higher value of ripple current reduces inductance, but increases the conductance loss, core loss, and current stress for the inductor and switch devices. It also requires a bigger output capacitor for the same output voltage ripple requirement. A reasonable value is setting the ripple current to be 30% of the DC output current. Since the ripple current increases with the input voltage, the maximum input voltage is always used to determine the inductance. The DC resistance of the inductor is a key parameter for the efficiency. Lower DC resistance is available with a bigger winding area. A good tradeoff between the efficiency and the core size is letting the inductor copper loss equal 2% of the output power.

OUTPUT CAPACITOR

The selection of C_{OUT} is driven by the maximum allowable output voltage ripple. The output ripple in the constant frequency, PWM mode is approximated by:

$$V_{RIPPLE} = I_{RIPPLE} \left(ESR + \frac{1}{8F_S C_{OUT}} \right) \quad (5)$$

The ESR term usually plays the dominant role in determining the voltage ripple. Low ESR ceramic, aluminum electrolytic, or tantalum capacitors (such as Taiyo Yuden MLCC, Nichicon PL series, Sanyo OS-CON, Sprague 593D, 594D, AVX TPS, and CDE polymer aluminum) is recommended. An electrolytic capacitor is not recommended for temperatures below −25°C since its ESR rises dramatically at cold temperature. Ceramic or tantalum capacitors have much better ESR specifications at cold temperature and is preferred for low temperature applications.

BOOTSTRAP CAPACITOR

A 4.7nF ceramic capacitor or larger is recommended for the bootstrap capacitor. For applications where the input voltage is less than twice the output voltage a larger capacitor is recommended, generally 0.1µF to 1µF to ensure plenty of gate drive for the internal switches and a consistently low $R_{DS(ON)}$.

SOFT-START CAPACITOR (BOTH REGULATORS)

The LM2717 does not contain internal soft-start which allows for fast startup time but also causes high inrush current. Therefore for applications that need reduced inrush current the LM2717 has circuitry that is used to limit the inrush current on start-up of the DC/DC switching regulators. This inrush current limiting circuitry serves as a soft-start. The external SS pins are used to tailor the soft-start for a specific application. A current (I_{SS}) charges the external soft-start capacitor, C_{SS}. The soft-start time can be estimated as:

$$T_{SS} = C_{SS} * 0.6V / I_{SS} \quad (6)$$

When programming the softstart time simply use the equation given in the *Soft-Start Capacitor* section above.

SHUTDOWN OPERATION (BOTH REGULATORS)

The shutdown pins of the LM2717 are designed so that they may be controlled using 1.8V or higher logic signals. If the shutdown function is not to be used the pin may be left open. The maximum voltage to the shutdown pin should not exceed 7.5V. If the use of a higher voltage is desired due to system or other constraints it may be used, however a 100k or larger resistor is recommended between the applied voltage and the shutdown pin to protect the device.

SCHOTTKY DIODE

The breakdown voltage rating of D_1 and D_2 is preferred to be 25% higher than the maximum input voltage. The current rating for the diode should be equal to the maximum output current for best reliability in most applications. In cases where the input voltage is much greater than the output voltage the average diode current is lower. In this case it is possible to use a diode with a lower average current rating, approximately (1-D)*I_{OUT} however the peak current rating should be higher than the maximum load current.

LAYOUT CONSIDERATIONS

The LM2717 uses two separate ground connections, PGND for the drivers and boost NMOS power device and AGND for the sensitive analog control circuitry. The AGND and PGND pins should be tied directly together at the package. The feedback and compensation networks should be connected directly to a dedicated analog ground plane and this ground plane must connect to the AGND pin. If no analog ground plane is available then the ground connections of the feedback and compensation networks must tie directly to the AGND pin. Connecting these networks to the PGND can inject noise into the system and effect performance.

The input bypass capacitor C_{IN}, as shown in Figure 12, must be placed close to the IC. This will reduce copper trace resistance which effects input voltage ripple of the IC. For additional input voltage filtering, a 0.1µF to 4.7µF bypass capacitors can be placed in parallel with C_{IN}, close to the V_{IN} pins to shunt any high frequency noise to ground. The output capacitors, C_{OUT1} and C_{OUT2}, should also be placed close to the IC. Any copper trace connections for the C_{OUTX} capacitors can increase the series resistance, which directly effects output voltage ripple. The feedback network, resistors R_{FB1} and R_{FB2}, should be kept close to the FB pin, and away from the inductor to minimize copper trace connections that can inject noise into the system. Trace connections made to the inductors and schottky diodes should be minimized to reduce power dissipation and increase overall efficiency. For more detail on switching power supply layout considerations see Application Note AN-1149: *Layout Guidelines for Switching Power Supplies* (SNVA021).

Application Information

Table 1. Some Recommended Inductors (Others May Be Used)

Manufacturer	Inductor	Contact Information
Coilcraft	DO3316 and DO5022 series	www.coilcraft.com
Coiltronics	DRQ73 and CD1 series	www.cooperet.com
Pulse	P0751 and P0762 series	www.pulseeng.com
Sumida	CDRH8D28 and CDRH8D43 series	www.sumida.com

Table 2. Some Recommended Input And Output Capacitors (Others May Be Used)

Manufacturer	Capacitor	Contact Information
Vishay Sprague	293D, 592D, and 595D series tantalum	www.vishay.com
Taiyo Yuden	High capacitance MLCC ceramic	www.t-yuden.com
Cornell Dubilier	ESRD seriec Polymer Aluminum Electrolytic SPV and AFK series V-chip series	www.cde.com
Panasonic	High capacitance MLCC ceramic EEJ-L series tantalum	www.panasonic.com

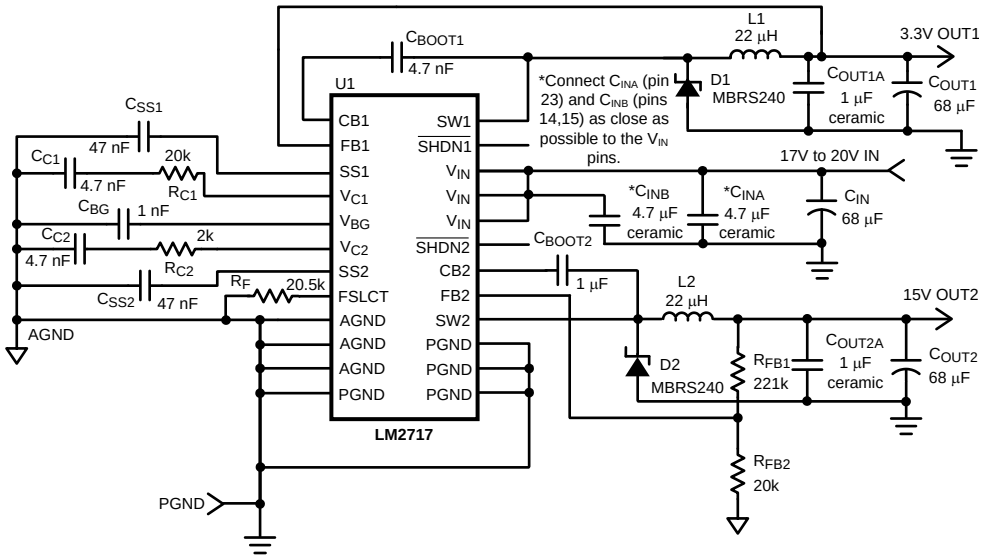


Figure 12. 15V, 3.3V Output Application

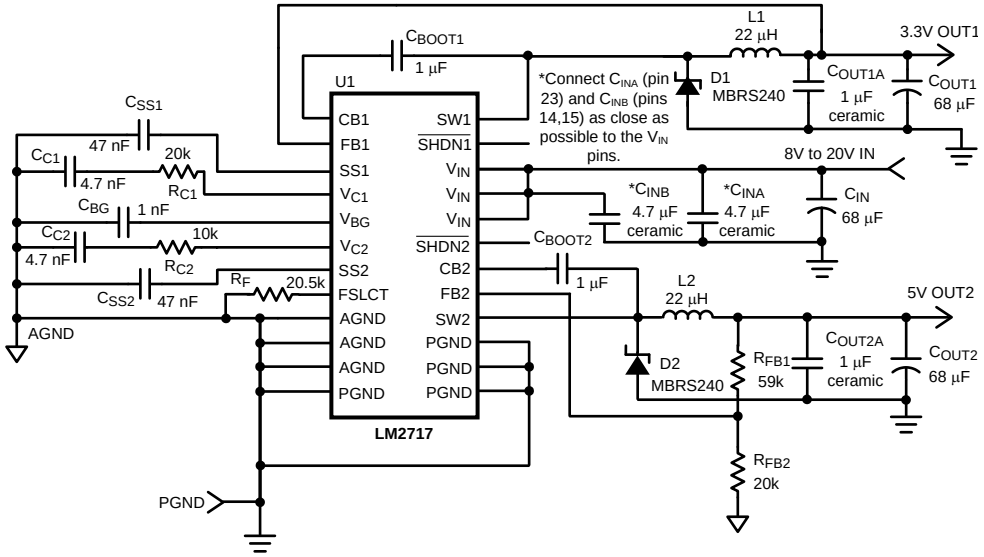


Figure 13. 5V, 3.3V Output Application

REVISION HISTORY

Changes from Revision C (March 2013) to Revision D	Page
• Changed layout of National Data Sheet to TI format	11

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM2717MT/NOPB	ACTIVE	TSSOP	PW	24	61	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LM2717MT	Samples
LM2717MTX/NOPB	ACTIVE	TSSOP	PW	24	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LM2717MT	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

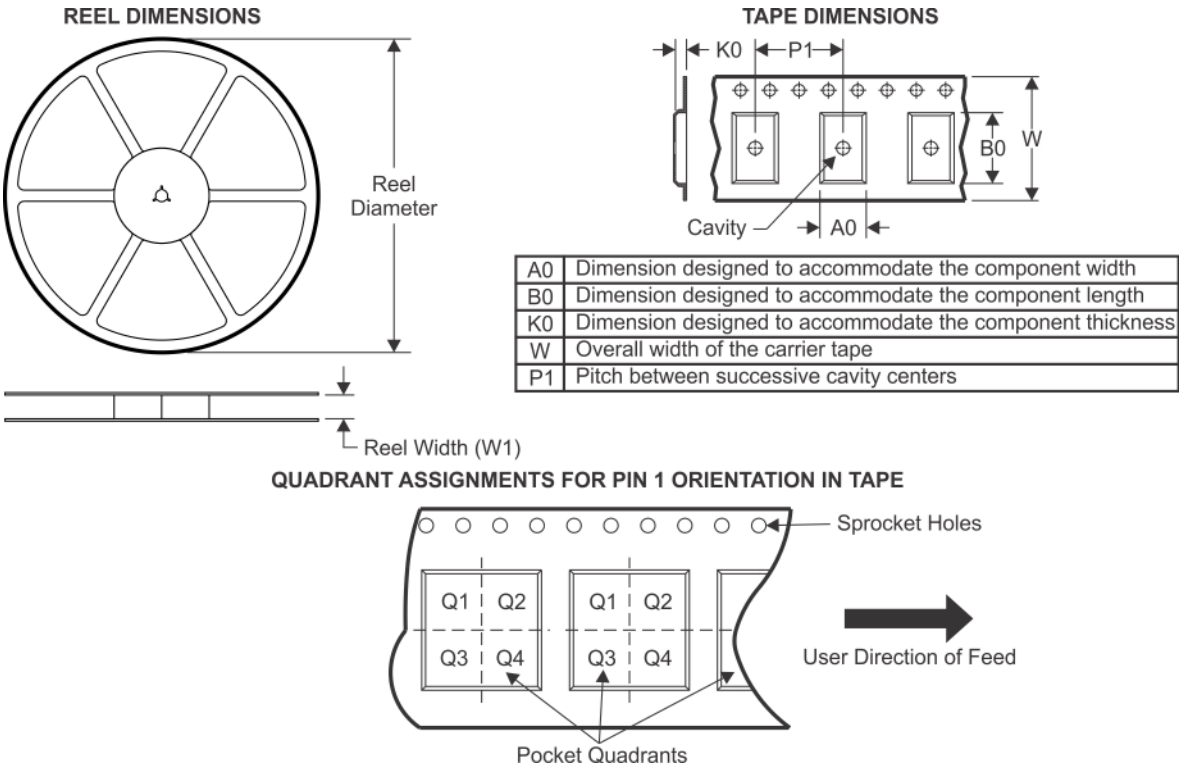
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

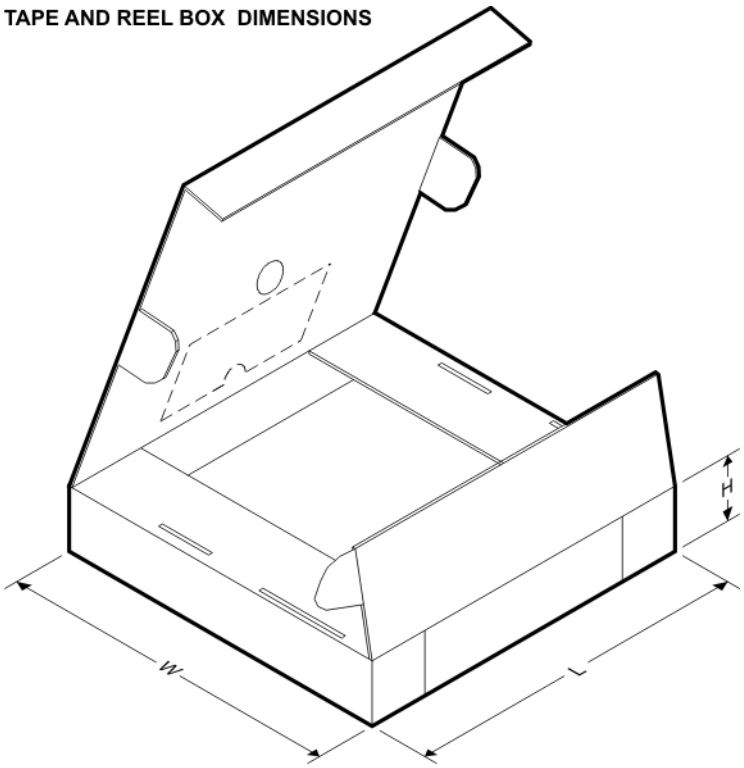


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM2717MTX/NOPB	TSSOP	PW	24	2500	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

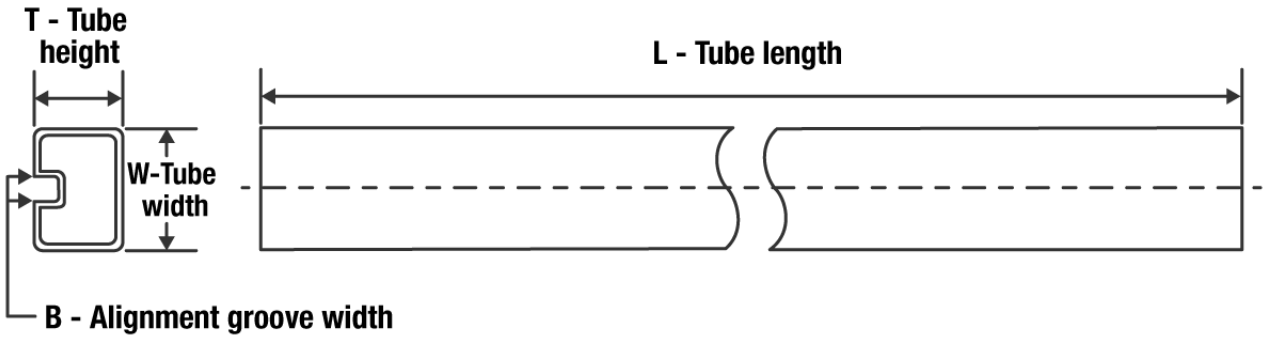
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM2717MTX/NOPB	TSSOP	PW	24	2500	367.0	367.0	35.0

TUBE



*All dimensions are nominal

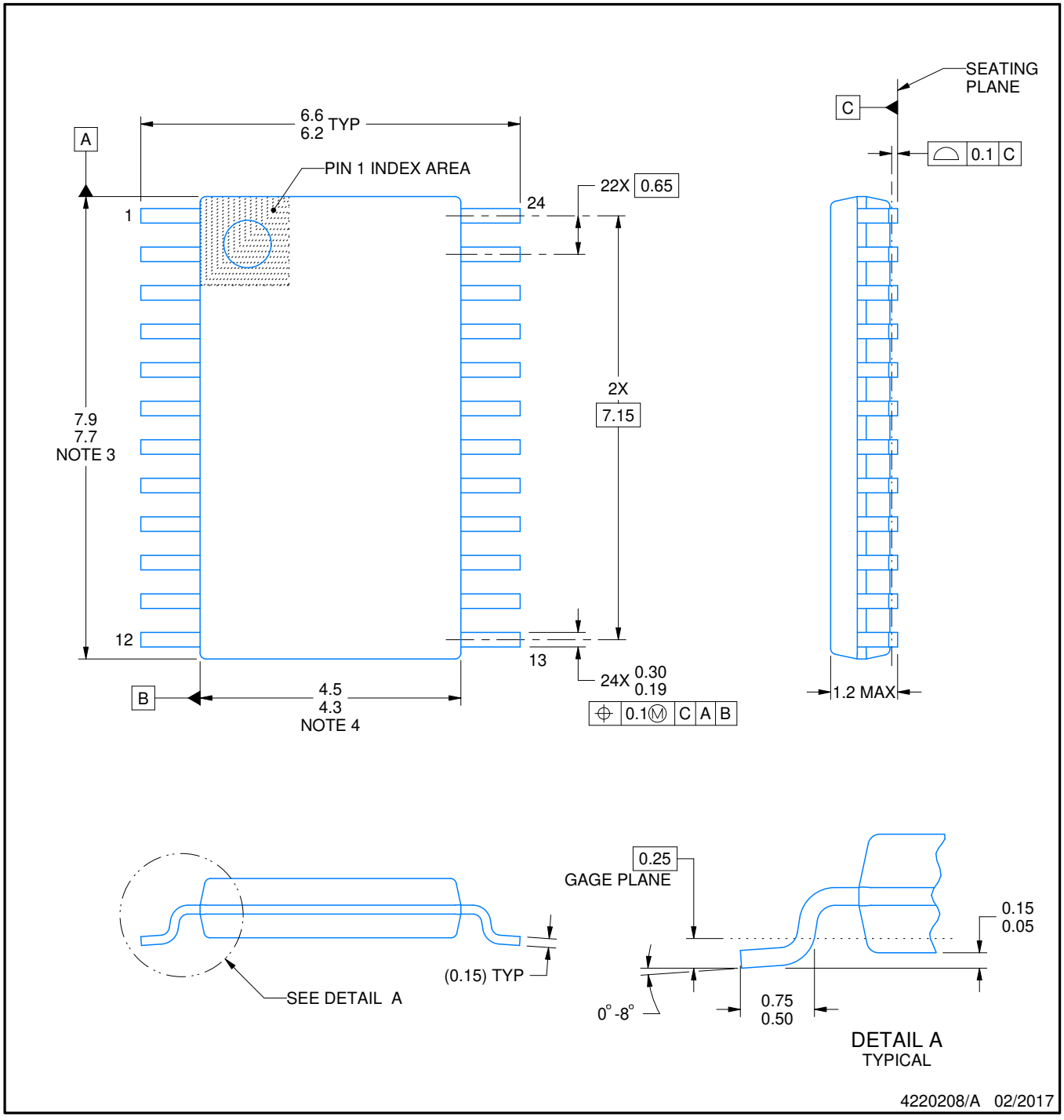
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LM2717MT/NOPB	PW	TSSOP	24	61	495	8	2514.6	4.06

PACKAGE OUTLINE

PW0024A

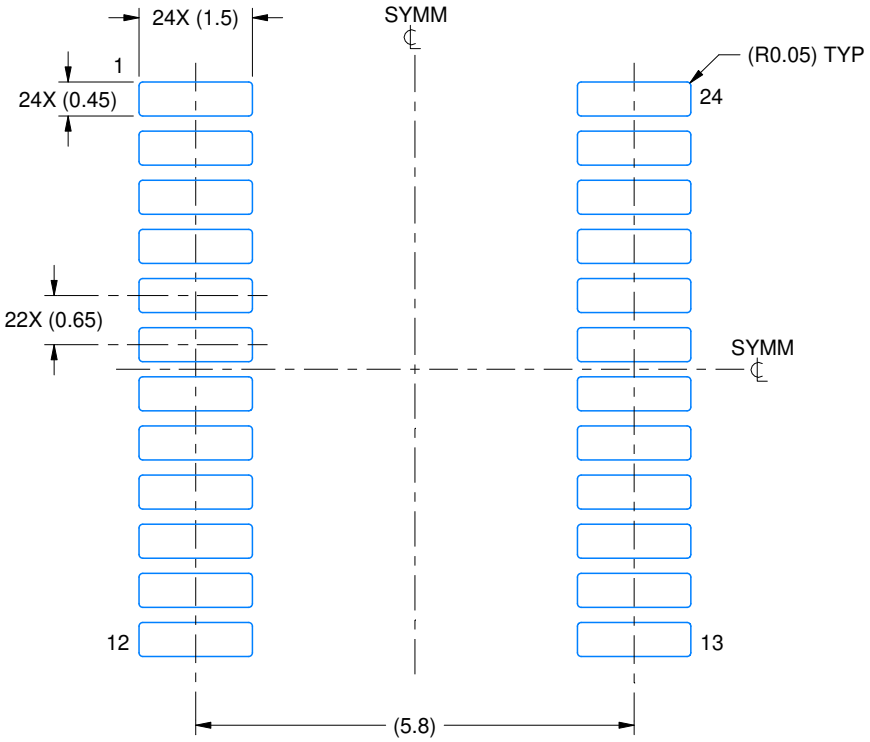
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

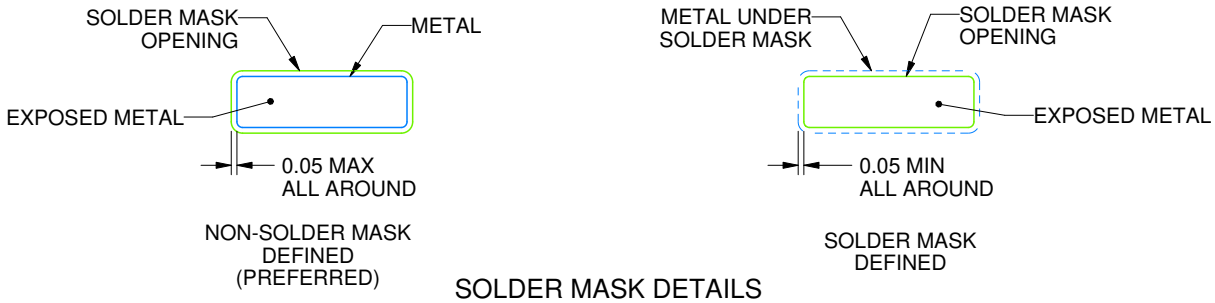


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

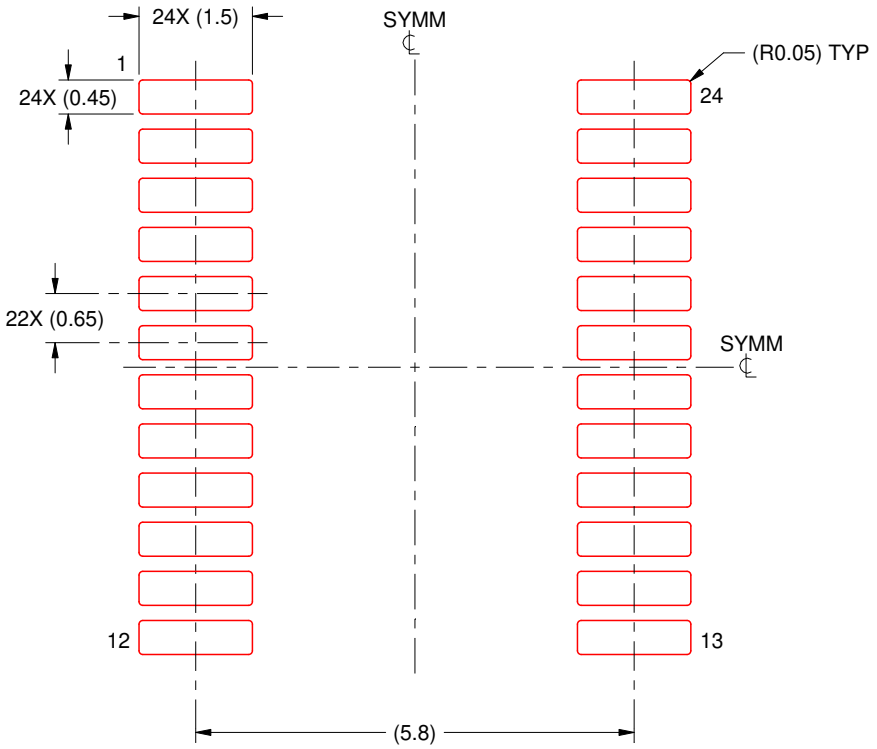


SOLDER MASK DETAILS

4220208/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220208/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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