19-3112; Rev 0; 11/92

MAXIM

8-Channel/Dual 4-Channel, Monolithic CMOS Multiplexers

1.0 SCOPE

1.1 This specification covers the detail requirements for two multiplexers with two configurations—8-channel single-ended and 4-channel differential. These circuits are processed in accordance with MIL-STD-883 and are fully compliant to paragraph 1.2.1.

It is highly recommended that this data sheet be used as a baseline for new military or aerospace source control drawings.

For typical applications and operating characteristics, consult Maxim's data books.

1.2 Part Numbers

Device	Part Number
-1	DG508A(X)/883B
-2	DG509A(X)/883B

1.3 Package

(X)	Package	Description
AK	J-16	16-Pin Ceramic Dual-In-Line Package (CERDIP)
AL	F-16	16-Pin Flat Package (FP)
AP	D-16	16-Pin Sidebraze Ceramic Package (Ceramic SB)
AZ	L-20	20-Pin Leadless Chip Carrier (LCC)

Note: See *Package Information* section for package drawings and dimensions.

1.4 Absolute Maximum Ratings

(T_A = +25°C, unless otherwise noted.)

V+ to V- 44V
V+ to GND 22V
V- to GND ..... -25V
Digital Inputs, V_S or V_D ..... (V- - 2V) to (V+ + 2V) or 20mA (whichever comes first)
Continuous Current (any terminal except S or D) 30mA
Continuous Current, S or D 20mA
Peak Current, S or D (pulsed at 1ms, 10% duty cycle max) 40mA
Power Dissipation (T_A = +70°C, Tj = +150°C)
16-Pin CERDIP (derate 10.00mW/°C above +70°C) 800mW
16-Pin FP (derate 6.06mW/°C above +70°C) 485mW
16-Pin Ceramic SB (derate 10.53mW/°C above +70°C) 842mW
20-Pin LCC (derate 9.09mW/°C above +70°C) 727mW
Operating Temperature Range ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10 sec) ..... +300°C

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1.5 Thermal Resistance

Θ_{JC} = 50°C/W for Q-16
Θ_{JC} = 55°C/W for E-20
Θ_{JC} = 65°C/W for F-16
Θ_{JC} = 45°C/W for D-16
Θ_{JA} = 100°C/W for Q-16
Θ_{JA} = 110°C/W for E-20
Θ_{JA} = 165°C/W for F-16
Θ_{JA} = 95°C/W for D-16

2.0 REQUIREMENTS

2.1 Electrical performance characteristics are specified in Table 1 and apply over the full ambient operating temperature range, unless otherwise specified.

TABLE 1. ELECTRICAL PERFORMANCE CHARACTERISTICS (Note 1)

CHARACTERISTICS	SYMBOL	CONDITIONS	DEVICE TYPES	GROUP A SUB-GROUPS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Analog-Signal Range	V_{ANALOG}	V_S = ±15V	All	1, 2, 3	-15		15	V
Drain-Source On Resistance	$r_{DS(ON)}$	V_O = ±10V, I_S = -200µA, sequence each switch on	All	1, 3			400	Ω
				2			500	
Drain-On Leakage Current	$I_{D(ON)}$	V_S = V_D = ±10V, sequence each switch on	-1	1	-10		10	µA
				2	-200		200	
			-2	1	-10		10	
				2	-100		100	
Drain-Off Leakage Current	$I_{D(OFF)}$	V_D = ±10V, V_{EN} = 0V, V_S = ∓10V	-1	1	-10		10	µA
				2	-200		200	
			-2	1	-10		10	
				2	-100		100	
Source-Off Leakage Current	$I_{S(OFF)}$	V_S = ±10V, V_D = ∓10V, V_{EN} = 0V	All	1	-1		1	µA
				2	-50		50	
Logic Input Current, Input Voltage High	I_{AH}	V_A = 2.4V	All	1	-10			µA
				2	-30			
		V_A = 15V		1			10	
				2			30	
Logic Input Current, Input Voltage Low	I_{AL}	V_{EN} = 0V or 2.4V, V_A = 0V	All	1	-10			µA
				2	-30			
Input Low Threshold	V_{AL}		All	1, 2, 3			0.8	V
Input High Threshold	V_{AH}		All	1, 2, 3	2.4			V
Positive Supply Current	I+	V_{EN} = 0V or 2.4V	All	1			2.4	mA

TABLE 1. ELECTRICAL PERFORMANCE CHARACTERISTICS (Note 1) (continued)

CHARACTERISTICS	SYMBOL	CONDITIONS	DEVICE TYPES	GROUP A SUB-GROUPS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Negative Supply Current	I-	V_{EN} = 0V or 2.4V	All	1	-1.5			mA
Transition Time	t_{TRANS}	Figure 1	All	9			1	µs
				10, 11			1.5	
Break-Before-Make Time	t_{OPEN}	Figure 2	All	9	5			ns
Enable Turn-On Time	$t_{ON(EN)}$	Figure 3	All	9			1.5	µs
				10, 11			2.0	
Enable Turn-Off Time	$t_{OFF(EN)}$	Figure 3	All	9			1.0	µs
				10, 11			2.0	
Charge Injection (Note 2)	Q		All	4		20		pC
Off Isolation (Note 2)	V_{ISO}	V_{EN} = 0V, R_L = 1kΩ, C_L = 15pF, V_S = 7V_{RMS}, f = 500kHz	All	4		50		dB
Logic Input Capacitance (Note 2)	C_{IN}	f = 1MHz	All	4		5		pF
Source-Off Capacitance (Note 2)	$C_{S(OFF)}$	V_{EN} = V_S = 0V, f = 140kHz	All	4		6		pF
Drain-Off Capacitance (Note 2)	$C_{D(OFF)}$	V_{EN} = V_D = 0V, f = 140kHz	-1	4		25		pF
			-2			12		

Note 1: V+ = 15V, V- = -15V, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V, unless otherwise noted.
Note 2: Typical limit for design aid only, not production tested.

3.0 QUALITY ASSURANCE

3.1 Sampling and inspection procedures shall be in accordance with MIL-M-38510 and, to the extent specified, with MIL-STD-883.

3.2 Screening shall be in accordance with Method 5004 of MIL-STD-883. Burn-in test (Method 1015):
(1) Test condition A, B, C, or D.
(2) T_A = +125°C, minimum.
(3) Interim and final electrical test requirements shall be as specified in Table 2.

3.3 Quality conformance inspection shall be in accordance with Method 5005 of MIL-STD-883 including Groups A, B, C, and D inspection.
Group A inspection:
(1) Tests as specified in Table 2.
(2) Selected subgroups in Table 1, Method 5005 of MIL-STD-883 shall be omitted.

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3.4 Groups C and D inspections:

a. End-point electrical parameters shall be specified in Table 1.

b. Steady-state life test (Method 1005 of MIL-STD-883):

(1) Test condition A, B, C, or D.

(2) TA = +125°C, minimum.

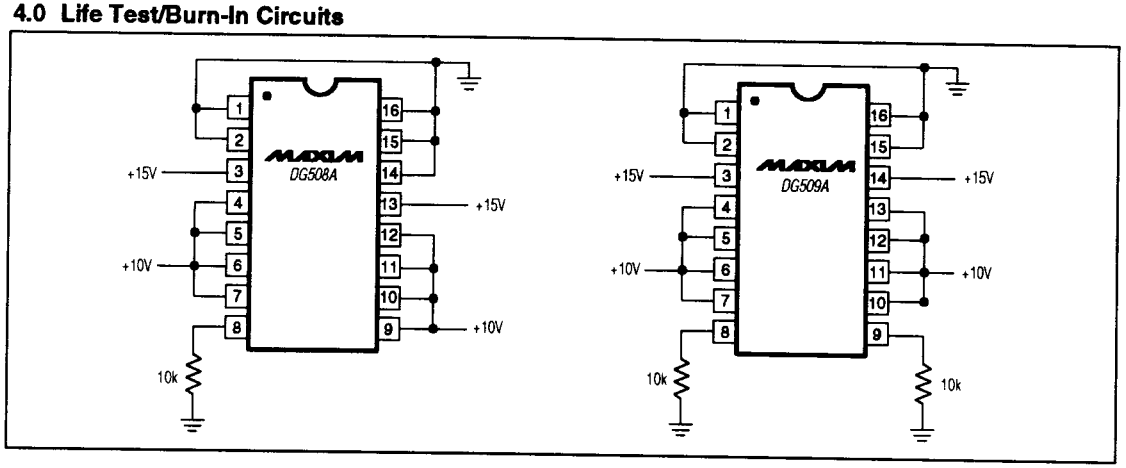
(3) Test duration, 1000 hours, except as permitted by Method 1005 of MIL-STD-883.

TABLE 2. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 Test Requirements	Subgroups (per Method 5005, Table 1)
Interim Electrical Parameters (Method 5004)	1
Final Electrical Parameters (Method 5004)	1,* 2, 3, 9
Group A Test Requirements (Method 5005)	1, 2, 3, 9, 10,** 11**
Groups C and D End-Point Electrical Parameters (Method 5005)	1

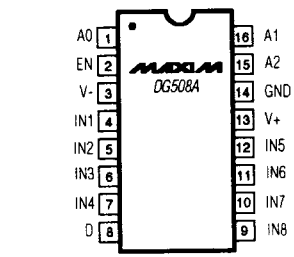
* PDA applies to Subgroup 1 only.
** Subgroups 10 and 11, if not tested, shall be guaranteed to the limits in Table 1.

4.0 Life Test/Burn-In Circuits

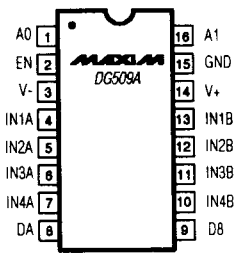


4.1 Pin Configurations

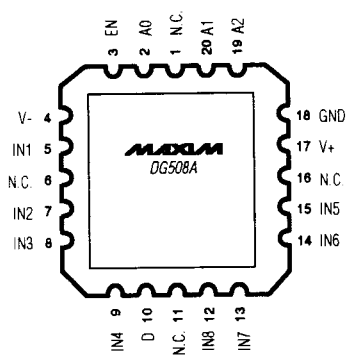
TOP VIEW



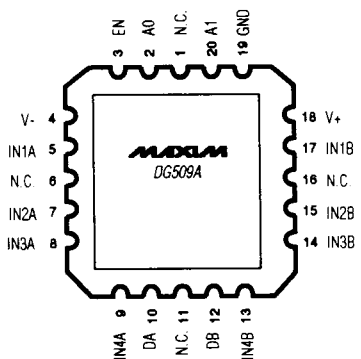
16-PIN CERDIP/FP



16-PIN CERDIP/FP



20-PIN LCC



20-PIN LCC

4.2 Truth Tables

DG508A				
A2	**A1**	**A0**	**EN**	**ON SWITCH**
X	X	X	0	NONE
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

DG509A			
A1	**A0**	**EN**	**ON SWITCH**
X	X	0	NONE
0	0	1	1
0	1	1	2
1	0	1	3
1	1	1	4

Note: LOGIC "0" = $V_{AL} \leq 0.8V$, LOGIC "1" = $V_{AH} \geq 2.4V$.

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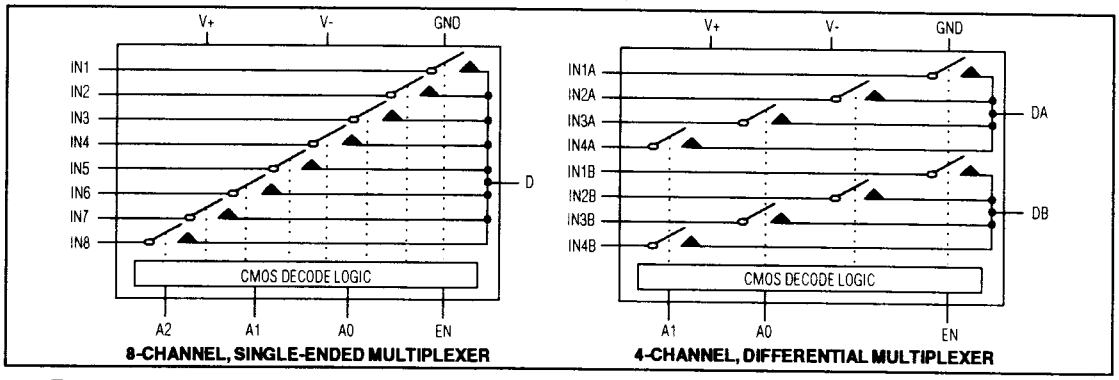
4.3 Functional Diagrams



4.4 Test Circuits

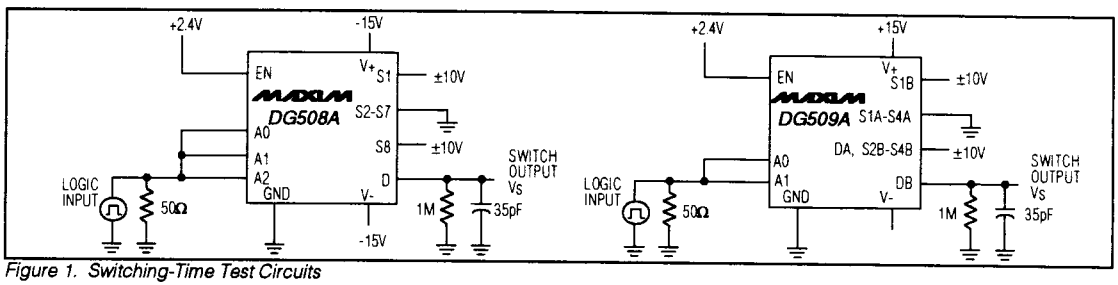


Figure 1. Switching-Time Test Circuits

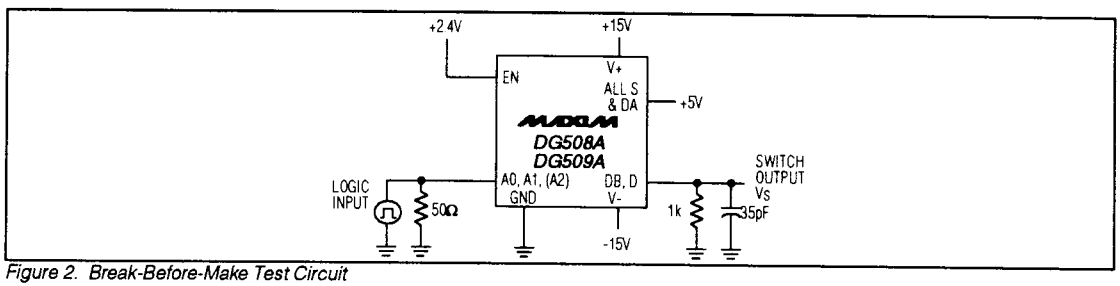


Figure 2. Break-Before-Make Test Circuit

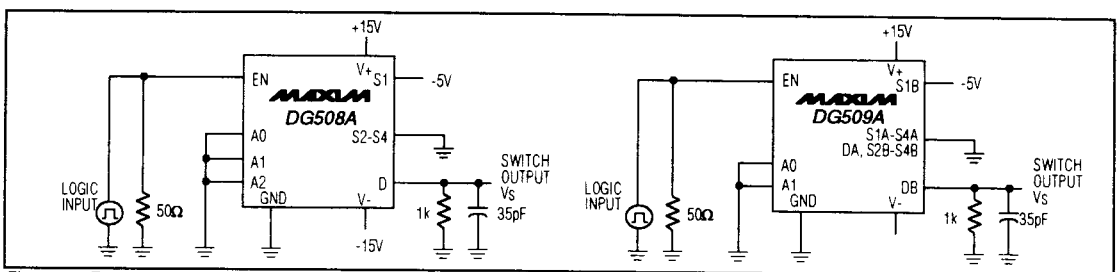


Figure 3. Enable-Time Test Circuits