TPS22971 3.6-V, 3-A, 6.7-mΩ On-Resistance Load Switch with Adjustable Fast Turn-ON and Power Good

1 Features

- Input voltage range (V_{IN}): 0.65 V to 3.6 V
- On-resistance
  - $R_{DS(on)}$ = 6.7 mΩ (typical) at V_{IN} ≥ 1.8 V
  - $R_{DS(on)}$ = 7.2 mΩ (typical) at V_{IN} = 1.05 V
  - $R_{DS(on)}$ = 8.9 mΩ (typical) at V_{IN} = 0.65 V
- Maximum continuous switch current (I_{MAX}): 3 A
- ON state (I_Q): 30 µA (typical) at 3.6 V_{IN}
- OFF state (I_{SD}): 1 µA (typical) at 3.6 V_{IN}
- Adjustable slew rate through CT pin
  - Fast turn-ON ≤ 65 µs at V_{IN} = 1 V
- Power good (PG) indicator after switch turn ON
- Low threshold enable (ON) of 0.9 V (V_{IH}) supports use of low voltage control logic
- Thermal shutdown (T_{SD})
- Quick output discharge (QOD): 150-Ω (typical)

2 Applications

- PC & notebooks
- Tablets
- Computer on modules
- Optical modules
- Data storage

3 Description

The TPS22971 is a space-saving single-channel load switch with controlled and adjustable turn-on slew rate and an integrated power good indicator. the device contains an n-channel mosfet that can operate over a low input voltage range of 0.65 v to 3.6 V and can support a maximum continuous current of 3 A. A low on-resistance of 6.7-mΩ minimizes the power loss and voltage drop across the load switch. The switch is controlled by an on and off input (ON), which is capable of interfacing directly with low-voltage control signals.

By default, the TPS22971 has a fast turn-on time to minimize system startup and wait time. The adjustable slew rate can also be reduced to limit inrush current. A power good (PG) signal internally monitors the gate threshold and indicates when the switch is fully on. When the switch is disabled, a 150-Ω on-chip resistor quickly discharges the output to ground and keeps it from floating.

The TPS22971 is available in an ultra-small, space saving 8-pin WCSP package and is characterized for operation over the free-air temperature range of –40°C to 105°C and integrates thermal shutdown to turn off in case of overheating.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS22971	DSBGA (8)	1.90 mm × 0.90 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application

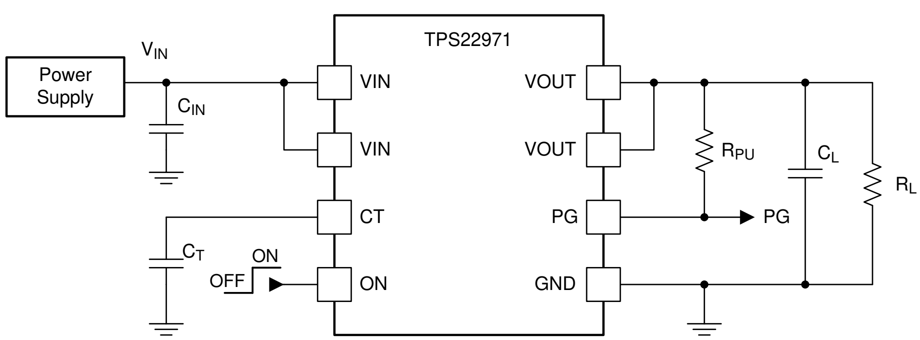


Table of Contents

4 Revision History

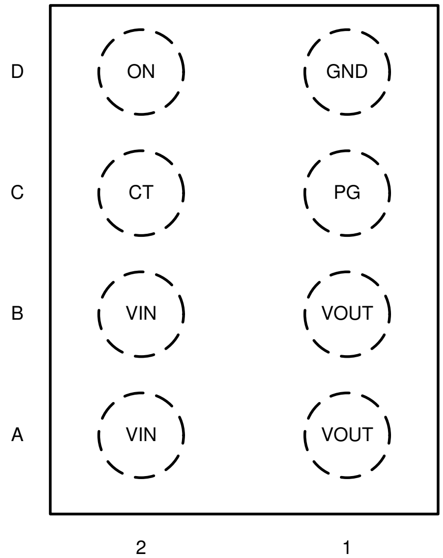
Changes from Revision B (December 2017) to Revision C	Page
• Changed test conditions from "V_{IN} = 1.0 V" to "V_{IN} = 1.05 V" and " 0°C ≤ T_A ≤ 85°C" to "–40°C ≤ T_A ≤ 85°C" for fast turn-on time specification in *Switching Characteristics* table	6
• Added load resistance and load capacitance test conditions for fast turn-on time specification in *Switching Characteristics* table	6

Changes from Original (April 2017) to Revision A	Page
• Changed device status from "Advance Information" to " Production Data"	1

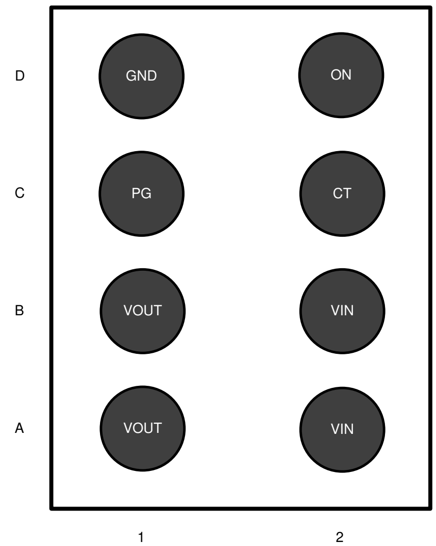
Changes from Revision A (July 2017) to Revision B	Page
• Deleted YZPT from Part Number in the *Device Information* table	1
• Changed 1.1 µA to 1 µA in the *Features* section	1
• Deleted Duplicate Package Drawing	1

5 Pin Configuration and Functions

YZP Package
8-Pin DSBGA
Laser Marking View



YZP Package
8-Pin DSBGA
Bump View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
CT	C2	O	VOUT slew rate control. Adding capacitance from this pin to ground lowers the output slew rate
GND	D1	GND	Ground
ON	D2	I	Switch enable control input. Do not leave floating
PG	C1	O	Power Good Indication. Open drain releases when the switch is fully on
VOUT	A1, B1	O	Switch output
VIN	A2, B2	I	Switch input

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{IN}	Input voltage	–0.3	4	V
V_{OUT}	Output voltage	–0.3	4	V
V_{ON}	ON voltage	–0.3	4	V
V_{PG}	PG voltage	–0.3	4	V
I_{MAX}	Maximum continuous switch current		3	A
I_{PLS}	Maximum pulsed switch current, pulse < 300-µs, 2% duty cycle		4	A
T_J	Maximum junction temperature	Internally Limited		
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IN}	Input voltage	0.65	3.6	V
V_{OUT}	Output voltage		V_{IN}	V
V_{IH}	High-level input voltage, ON	0.9	3.6	V
V_{IL}	Low-level input voltage, ON	0	0.45	V
T_J	Operating temperature	–40	125	°C
T_A	Operating free-air temperature	–40	105	°C
C_T	CT pin capacitor voltage rating	7		V

6.4 Thermal Information

THERMAL METRIC (1)		TPS22971 YZP (DSBGA) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	130	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	54	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	51	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	50	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

Unless otherwise noted, V_{IN} = 0.65 V to 3.6 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
I_Q	Quiescent current	V_{OUT} = Open, Switch enabled	V_{IN} > 1.2 V	–40°C to +85°C		30	65	µA
				–40°C to +105°C			75	
			V_{IN} ≤ 1.2 V	–40°C to +85°C		20	50	
				–40°C to +105°C			55	
I_{SD}	Shutdown current	V_{OUT} = GND, Switch disabled	V_{IN} > 1.8 V	–40°C to +85°C		1	7.5	µA
				–40°C to +105°C			18	
			V_{IN} ≤ 1.8 V	–40°C to +85°C		0.9	5.5	
				–40°C to +105°C			9.5	
R_{ON}	ON-resistance	I_{OUT} = –200 mA	V_{IN} ≥ 1.8 V	25°C		6.7	10	mΩ
				–40°C to +85°C			12	
				–40°C to +105°C			12	
			V_{IN} = 1.2 V	25°C		6.9	10	
				–40°C to +85°C			12	
				–40°C to +105°C			13	
			V_{IN} = 1.05 V	25°C		7.2	10.5	
				–40°C to +85°C			13	
				–40°C to +105°C			14	
			V_{IN} = 0.65 V	25°C		8.9	14	
				–40°C to +85°C			18	
				–40°C to +105°C			19	
R_{PD}	Output pull down resistance (1)	I_{OUT} = 3 mA, Switch disabled	V_{IN} = 3.6 V	–40°C to +105°C		150		Ω
			V_{IN} = 0.65 V	–40°C to +105°C		710		Ω
I_{ON}	ON input leakage current	V_{ON} =0 V to 3.6 V		–40°C to +105°C			0.1	µA
$I_{PG,LK}$	Leakage current into PG pin	V_{PG} = 0 V to 3.6 V	V_{ON} ≤ V_{IL}	–40°C to +105°C		0.1	8.5	µA
$V_{PG,OL}$	PG output low voltage	V_{PG} = 0 V to 3.6 V	V_{ON} ≥ V_{IH}, I_{PG} = 1 mA	–40°C to +105°C			0.2	V
T_{SD}	Thermal shutdown	T_J rising				170		°C
$T_{SD, HYS}$	Thermal shutdown hysteresis	T_J falling				30		°C

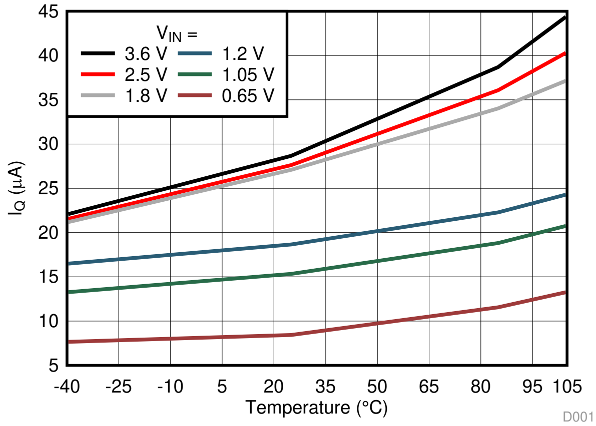
(1) See the *Quick Output Discharge (QOD)* section.

6.6 Switching Characteristics

All typical values are at 25°C unless otherwise noted

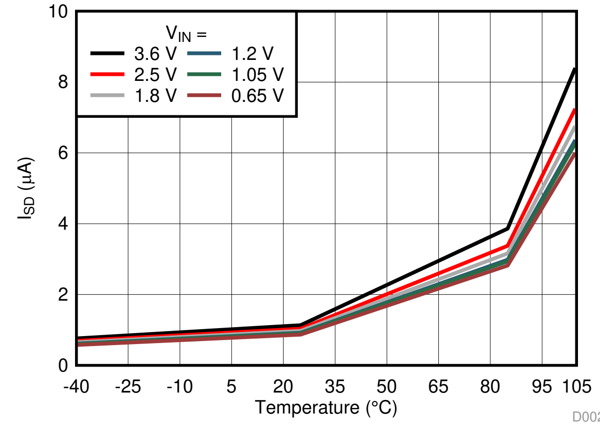
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN} = 3.6 V						
t_{ON}	Turn-On time	C_T = 0 pF		54		µs
		C_T = 1000 pF		198		
		C_T = 10000 pF		1520		
t_R	VOUT Rise time	C_T = 0 pF		35		
		C_T = 1000 pF		150		
		C_T = 10000 pF		1230		
$t_{PG,ON}$	PG Turn-On time	C_T = 0 pF		134		
		C_T = 1000 pF		314		
		C_T = 10000 pF		1990		
$t_{PG,OFF}$	PG Turn-Off time			1.9		
t_{OFF}	Turn-Off time			3.5		
t_F	VOUT Fall time	C_L = 0.1 µF, R_L = 10 Ω		2.1		
V_{IN} = 1.8 V						
t_{ON}	Turn-On time	C_T = 0 pF		41		µs
		C_T = 1000 pF		126		
		C_T = 10000 pF		857		
t_R	VOUT Rise time	C_T = 0 pF		21		
		C_T = 1000 pF		82		
		C_T = 10000 pF		628		
$t_{PG,ON}$	PG Turn-On time	C_T = 0 pF		105		
		C_T = 1000 pF		220		
		C_T = 10000pF		1230		
$t_{PG,OFF}$	PG Turn-Off time			0.8		
t_{OFF}	Turn-Off time			4.8		
t_F	VOUT Fall time	C_L = 0.1 µF, R_L = 10 Ω		2.1		
V_{IN} = 0.65 V						
t_{ON}	Turn-On time	C_T = 0 pF		54		µs
		C_T = 1000 pF		127		
		C_T = 10000 pF		720		
t_R	VOUT Rise time	C_T = 0 pF		21		
		C_T = 1000 pF		61		
		C_T = 10000 pF		386		
$t_{PG,ON}$	PG Turn-On time	C_T = 0 pF		165		
		C_T = 1000 pF		290		
		C_T = 10000 pF		1290		
$t_{PG,OFF}$	PG Turn-Off time			0.5		
t_{OFF}	Turn-Off time			55		
t_F	VOUT Fall time	C_L = 0.1 µF, R_L = 10 Ω		8		
V_{IN} = 1.05 V						
t_{ON}	Fast Turn-On time	C_T = 0 pF, C_L = 0.1 µF, R_L = 10 Ω , –40°C ≤ T_A ≤ 85°C		30	65	µs

6.7 Typical DC Characteristics



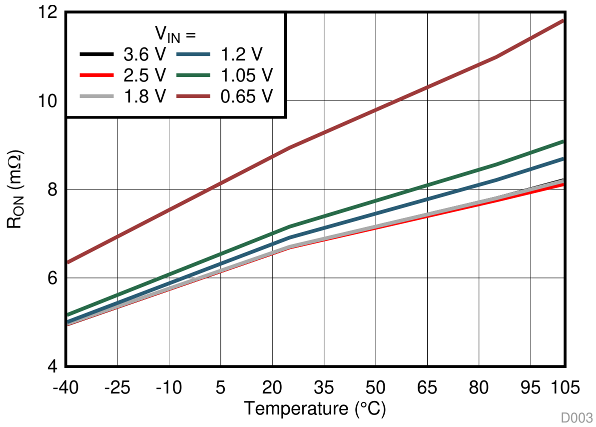
V_{ON} = 3.6 V I_{OUT} = 0

Figure 1. Quiescent Current vs Temperature



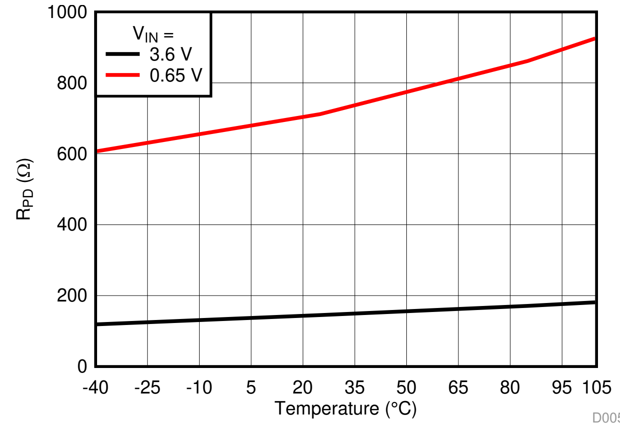
V_{ON} = 0 V V_{OUT} = 0

Figure 2. Input Shutdown Current vs Temperature



V_{ON} = 3.6 V I_{OUT} = -200 mA

Figure 3. On-Resistance vs Temperature



V_{ON} = 3.6 V   Initially V_{OUT} = V_{IN}

Figure 4. Output Pull-Down Resistance vs Temperature

6.8 Typical AC Characteristics

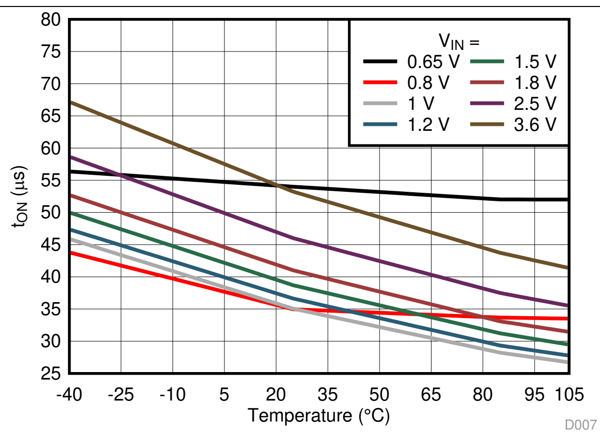
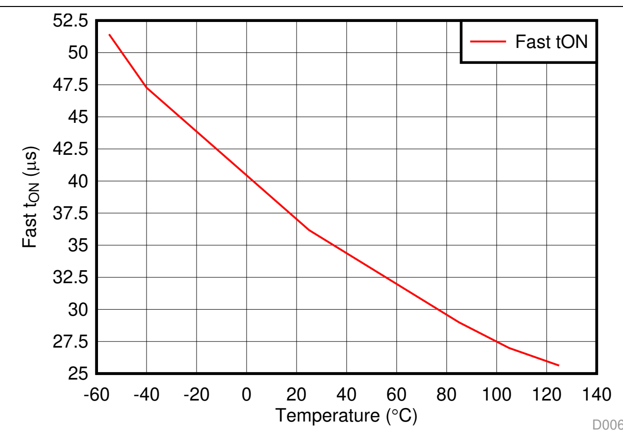


Figure 5. Turn-On Time vs Temperature



V_{IN} = 1V C_T = 0 pF C_L = 0.1 µF R_L = 10 Ω

Figure 6. Fast Turn-On Time vs Temperature

Typical AC Characteristics (continued)

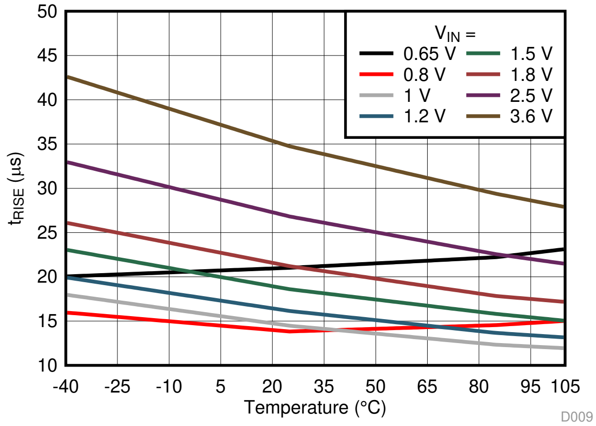


Figure 7. Rise Time vs Temperature

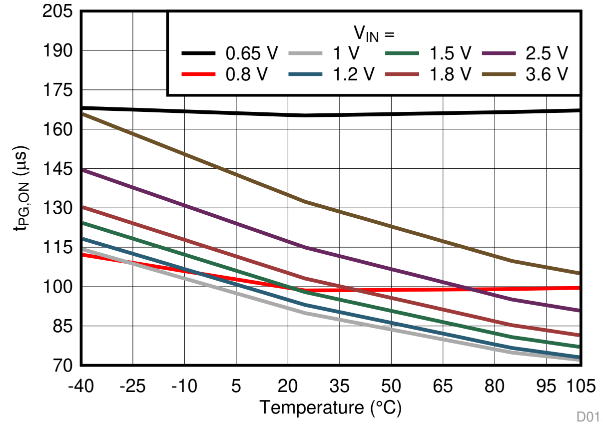


Figure 8. PG Turn-On Time vs Temperature

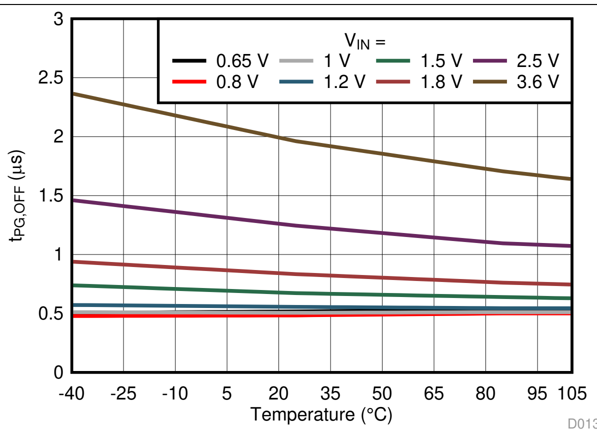


Figure 9. PG Turn-Off Time vs Temperature

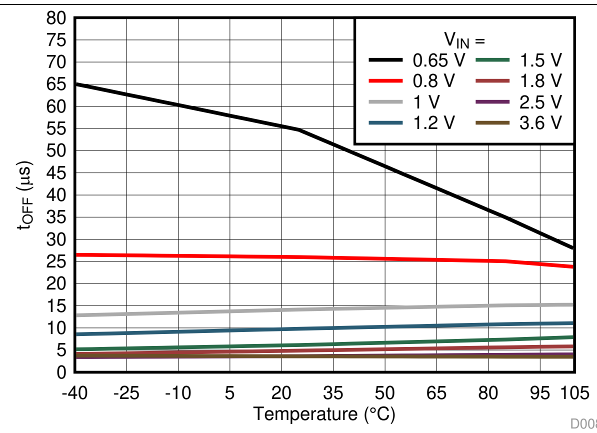
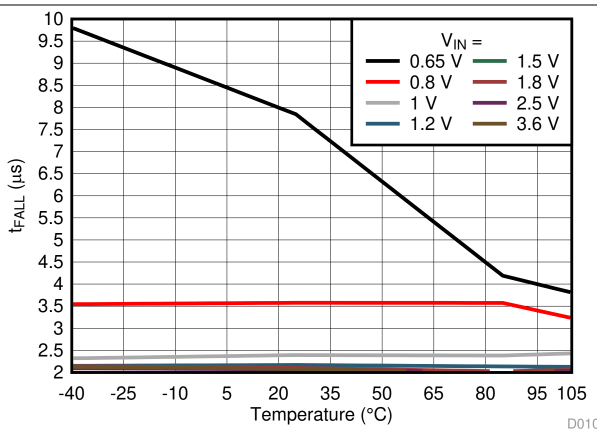
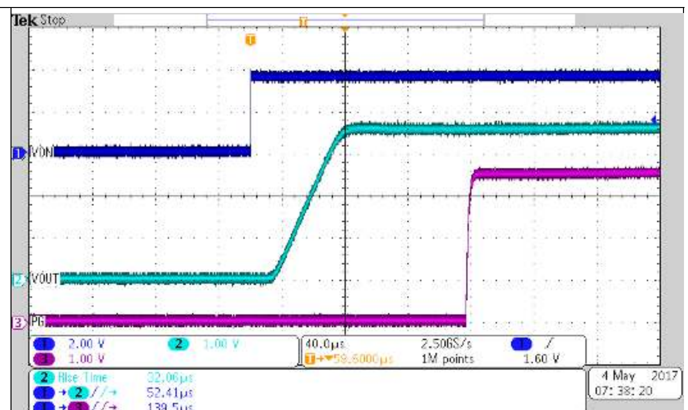


Figure 10. Turn-Off Time vs Temperature



R_L = 10 Ω C_L = 0.1 µF

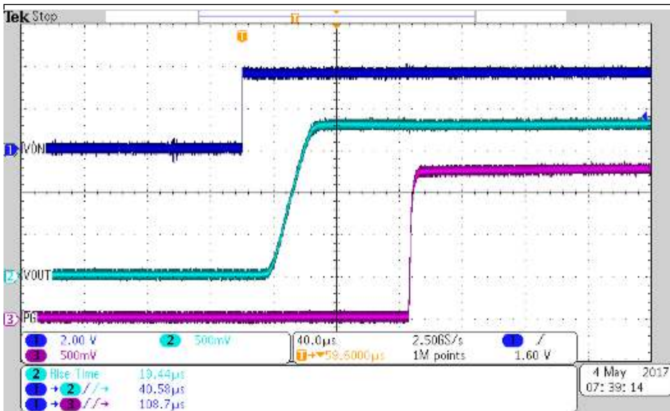
Figure 11. Fall Time vs Temperature



R_L = 10 Ω C_T = 0 pF
T_A = 25°C C_L = 0.1 µF

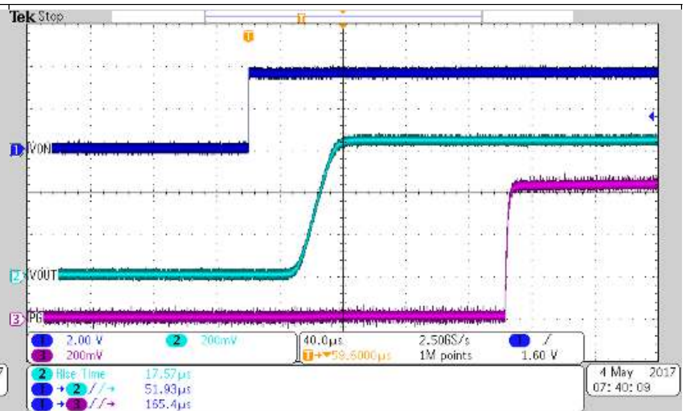
Figure 12. Turn-On Response at 3.6 V_{IN}

Typical AC Characteristics (continued)



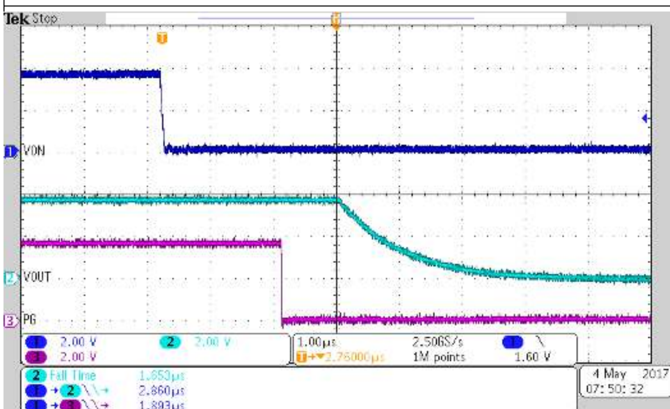
R_L = 10 Ω C_T = 0 pF
T_A = 25°C C_L = 0.1 µF

Figure 13. Turn-On Response at 1.8 V_{IN}



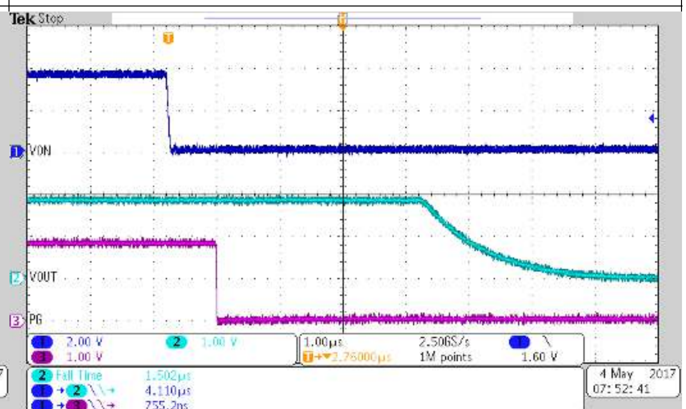
R_L = 10 Ω C_T = 0 pF
T_A = 25°C C_L = 0.1 µF

Figure 14. Turn-On Response at 0.65 V_{IN}



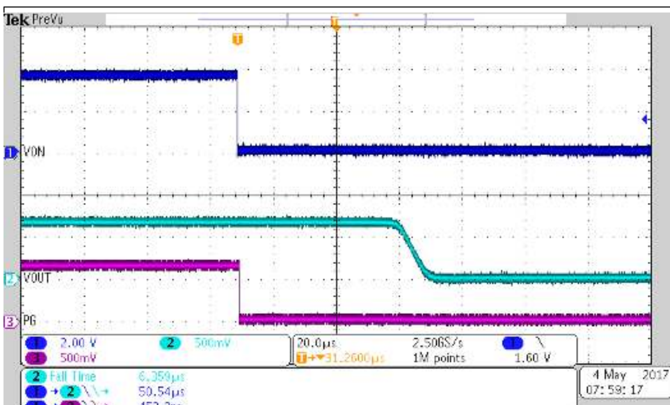
R_L = 10 Ω C_T = 0 pF
T_A = 25°C C_L = 0.1 µF

Figure 15. Turn-Off Response at 3.6 V_{IN}



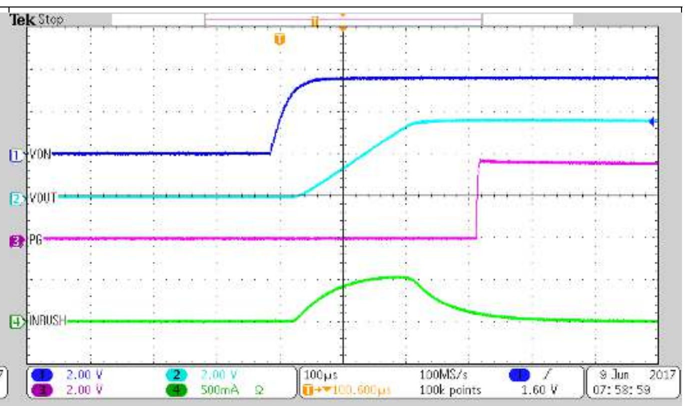
R_L = 10 Ω C_T = 0 pF
T_A = 25°C C_L = 0.1 µF

Figure 16. Turn-Off Response at 1.8 V_{IN}



R_L = 10 Ω C_{IN} = 0 pF
T_A = 25°C C_L = 0.1 µF

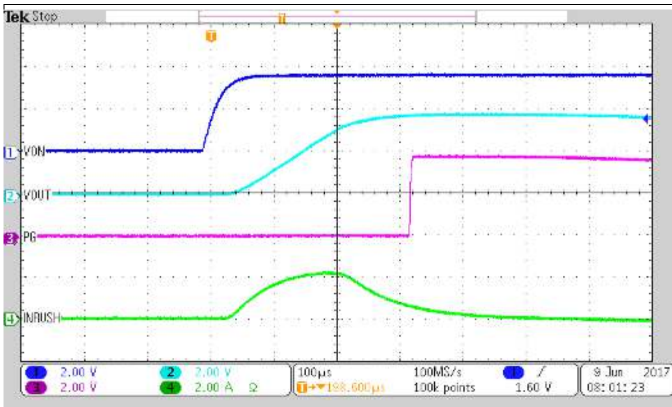
Figure 17. Turn-Off Response at 0.65 V_{IN}



C_T = 1000 pF C_L = 33 µF
R_L = OPEN T_A = 25°C

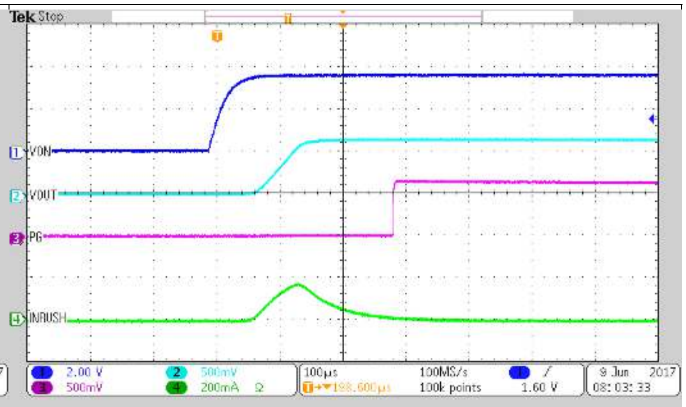
Figure 18. Low Inrush Current at 3.6 V_{IN}

Typical AC Characteristics (continued)



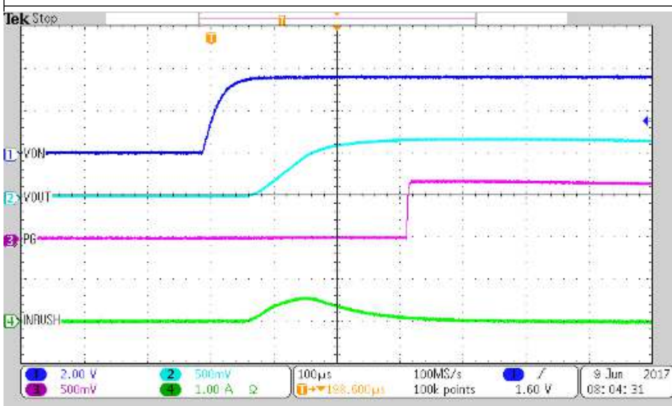
C_T = 1000 pF C_L = 133 µF
R_L = OPEN T_A = 25°C

Figure 19. High Inrush Current at 3.6 V_{IN}



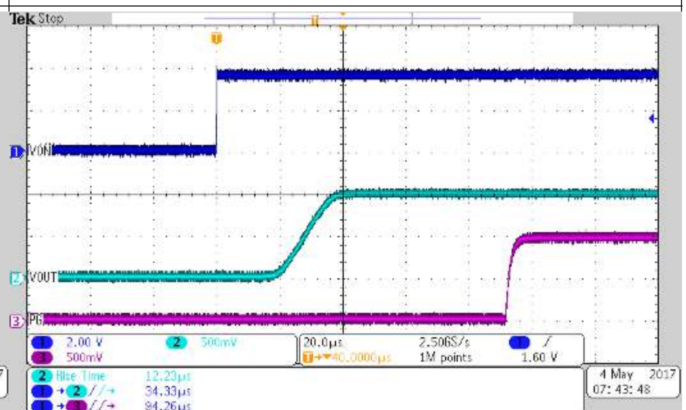
C_T = 1000 pF C_L = 33 µF
R_L = OPEN T_A = 25°C

Figure 20. Low Inrush Current at 0.65 V_{IN}



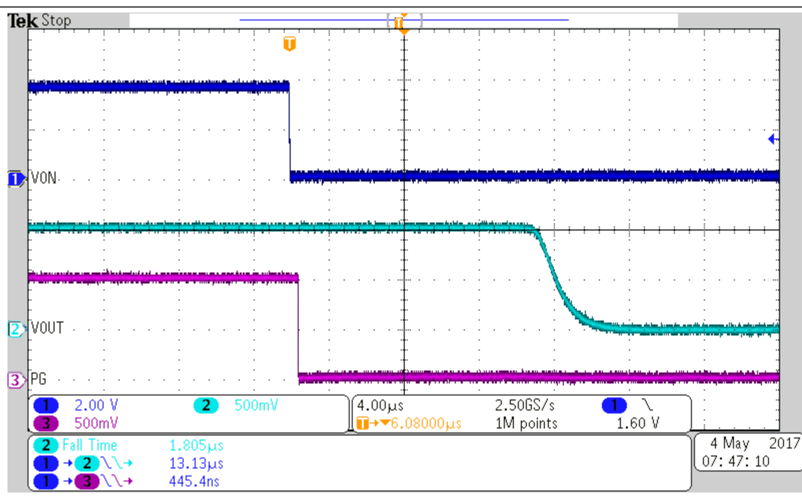
C_T = 1000 pF C_L = 133 µF
R_L = OPEN T_A = 25°C

Figure 21. High Inrush Current at 0.65 V_{IN}



C_T = 0 pF C_L = 0.1 µF
R_L = 10 Ω T_A = 25°C

Figure 22. Fast Turn-On Response



C_{IN} = 0 pF C_L = 0.1 µF
R_L = 10 Ω T_A = 25°C

Figure 23. Fast Turn-Off Response

7 Parameter Measurement Information

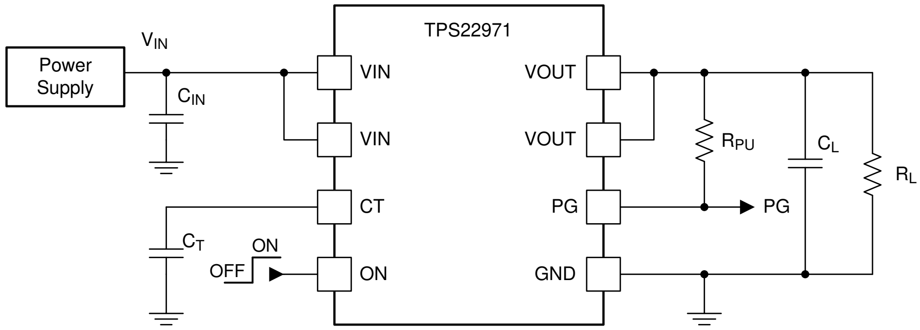


Figure 24. TPS22971 Test Circuit

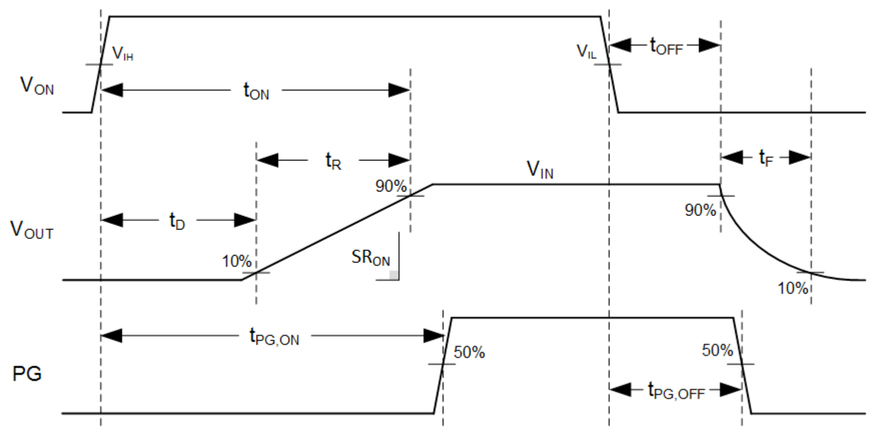


Figure 25. AC Timing Waveforms

8 Detailed Description

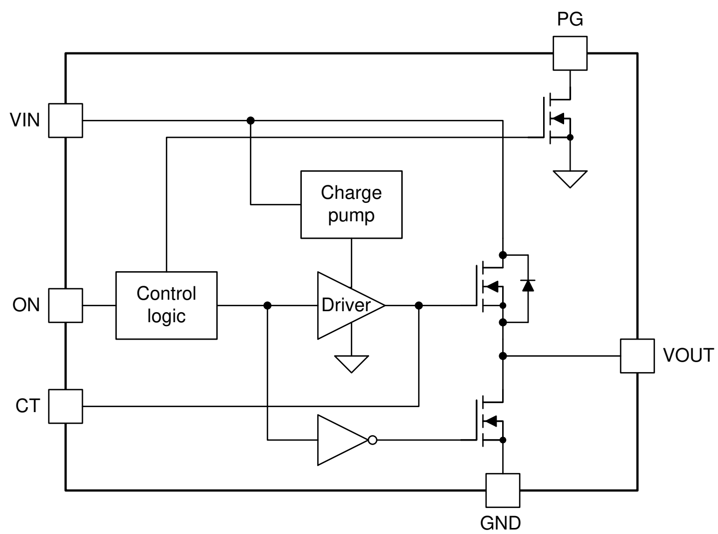
8.1 Overview

The TPS22971 is a single channel, 3-A load switch in a small, space-saving WCSP-8 package. This device implements a low resistance N-channel MOSFET with a controlled rise time for applications that need to limit the inrush current.

The controlled rise time for the device greatly reduces inrush current caused by large bulk load capacitances, thereby reducing or eliminating power supply droop. The adjustable slew rate through CT provides the design flexibility to trade off the inrush current and power up timing requirements. Integrated PG indicator notifies the system about the status of the load switch to facilitate seamless power sequencing.

This device is also designed to have very low leakage current during off state, which prevents downstream circuits from pulling high standby current from the supply. Integrated control logic, driver, power supply, and output discharge FET eliminates the need for additional external components, which reduces solution size and bill of materials (BOM) count.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 On and Off Control

The ON pin controls the state of the switch. Asserting ON high enables the switch. ON has a low threshold, making it capable of interfacing with low-voltage signals. The ON pin is compatible with standard GPIO logic. It can be used with any microcontroller with 1.2-V, 1.8-V, 2.5-V or 3.3-V GPIOs. This pin does not have an internal bias and must not be left floating for proper functionality.

8.3.2 Controlled Turn-On

The TPS22971 has controlled Turn-On for inrush current control. A capacitor to GND on the CT pin adjusts the slew rate. For a given input voltage and desired slew rate, Equation 1 can be used to find the required CT value. For calculated CT values less than 220 pF, use 0 pF instead when solving for t_{ON} and $t_{PG,ON}$.

$$CT\left(VIN, SR\right) = \frac{\left(\frac{VIN}{SR} - \left(3.1 \times VIN\right) - 14.2\right) \times 800}{\left(\left(32.5 \times VIN\right) + 12.5\right)}$$

where

- CT is the capacitor on the CT pin (in pF)

Feature Description (continued)

- VIN is the input voltage (in V)
- SR is the desired slew rate (in V/µs) (1)

The CT value determined in Equation 1 can be used to find the total Turn-On time, t_{ON}, in Equation 2 or Equation 3 depending on V_{IN}.

$$tON\left(VIN \geq 0.95\ V, CT\right) = \left(\left(15 + \left(33 \times VIN\right)\right) \times \frac{CT}{1000}\right) + \left(\left(3.9 \times VIN\right) + 35\right) \tag{2}$$

$$tON\left(VIN < 0.95\ V, CT\right) = \left(\left(45 + \left(33 \times VIN\right)\right) \times \frac{CT}{1000}\right) + \left(\left(3.9 \times VIN\right) + 55\right)$$

where

- tON is the Turn-On time (in µs)
- CT is the capacitor on the CT pin (in pF)
- VIN is the input voltage (in V) (3)

8.3.3 Power Good (PG)

The TPS22971 has a power good (PG) output signal to indicate the gate of the pass FET is driven high and the switch is fully on (full load ready). The signal is an active high and open drain output which can be connected to a voltage source through an external pull up resistor, R_{PU}. This voltage source can be V_{OUT} from the TPS22971 or another external voltage. Equation 4 and Equation 5 show the approximate equation for the relationship between CT setting, V_{IN} and PG Turn-On time ($t_{PG,ON}$):

$$tPG,ON\left(VIN \geq 0.95\ V, CT\right) = \left(\left(40 + \left(36 \times VIN\right)\right) \times \frac{CT}{1000}\right) + \left(\left(10.7 \times VIN\right) + 85\right) \tag{4}$$

$$tPG,ON\left(VIN < 0.95\ V, CT\right) = \left(\left(80 + \left(36 \times VIN\right)\right) \times \frac{CT}{1000}\right) + \left(\left(10.7 \times VIN\right) + 155\right)$$

where

- $t_{PG,ON}$ is the PG Turn-On time (in µs)
- V_{IN} is the input voltage (in V)
- C_T is the capacitance value on the CT pin (in pF) (5)

8.3.4 Quick Output Discharge (QOD)

The TPS22971 includes a QOD feature. When the switch is disabled, a discharge resistor is connected between VOUT and GND. This resistor has a typical value of 150 Ω and prevents the output from floating while the switch is disabled. The QOD pull-down resistance can vary with input voltage and temperature, see Figure 4.

8.4 Device Functional Modes

Table 1 lists the functional modes for the TPS22971.

Table 1. Function Table

TPS22971			
ON-Pin	**V_{IN} to V_{OUT}**	**V_{OUT} to GND**	**PG to GND**
Below V_{IL}	OFF	ON	ON
Above V_{IH}	ON	OFF	OFF

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Thermal Consideration

It is recommended to limit the junction temperature (T_J) to below 125°C. To calculate the maximum allowable dissipation, $P_{D(max)}$ for a given output current and ambient temperature, use Equation 6 as a guideline:

$$P_{D(max)} = \frac{T_{J(max)} - T_A}{\theta_{JA}}$$

where

- $P_{D(max)}$ is maximum allowable power dissipation
- $T_{J(max)}$ is maximum allowable junction temperature
- T_A is ambient temperature of the device
- Θ_{JA} is junction to air thermal impedance. See the *Thermal Information* section. This parameter is highly dependent upon board layout (6)

9.1.2 PG Pull Up Resistor

The PG output is an open drain signal which connects to a voltage source through a pull up resistor R_{PU}. The PG signal can be used to drive the enable pins of downstream devices, EN. PG is active high, and its voltage is given by Equation 7.

$$V_{PG} = V_{OUT} - \left(I_{PG,LK} + I_{EN,LK}\right) \times R_{PU}$$

where

- V_{OUT} is the voltage where PG is tied to
- $I_{PG,LK}$ is the leakage current into PG pin
- $I_{EN,LK}$ is the leakage current into the EN pin driven by PG
- R_{PU} is the pull up resistance (7)

V_{PG} needs to be higher than $V_{IH,MIN}$ of the EN pin to be treated as logic high. The maximum R_{PU} is determined by Equation 8.

$$R_{PU,MAX} = \frac{V_{OUT} - V_{IH,MIN}}{I_{PG,LK} + I_{EN,LK}} \quad (8)$$

When PG is disabled, with 1 mA current into PG pin (IPG = 1 mA), $V_{PG.OL}$ is less than 0.2 V and treated as logic low as long as $V_{IL,MAX}$ of the EN pin is greater than 0.2 V. The minimum R_{PU} is determined by Equation 9.

$$R_{PU,MIN} = \frac{V_{OUT}}{I_{PG} + I_{EN,LK}} \quad (9)$$

R_{PU} can be chosen within the range defined by $R_{PU,MIN}$ and $R_{PU,MAX}$. R_{PU} = 10 kΩ is used for characterization.

9.1.3 Power Sequencing

The TPS22971 has an integrated power good indicator which can be used for power sequencing. As shown in Figure 26, the switch to the second load is controlled by the PG signal from the first switch. This ensures that the power to load 2 is only enabled after the same power to load 1 is enabled after the first switch has turned on.

Application Information (continued)

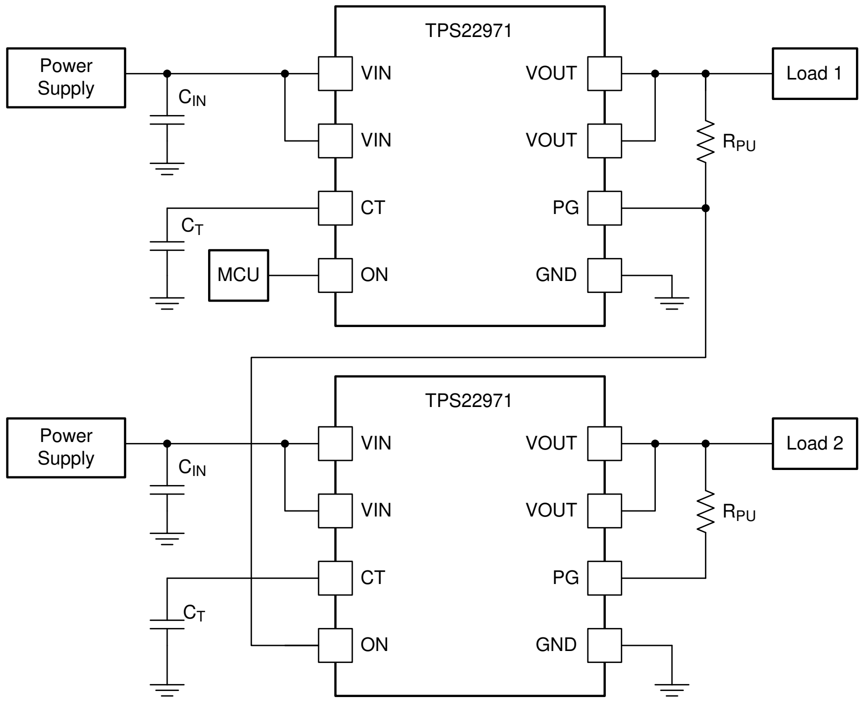


Figure 26. Power Sequencing

9.2 Typical Application

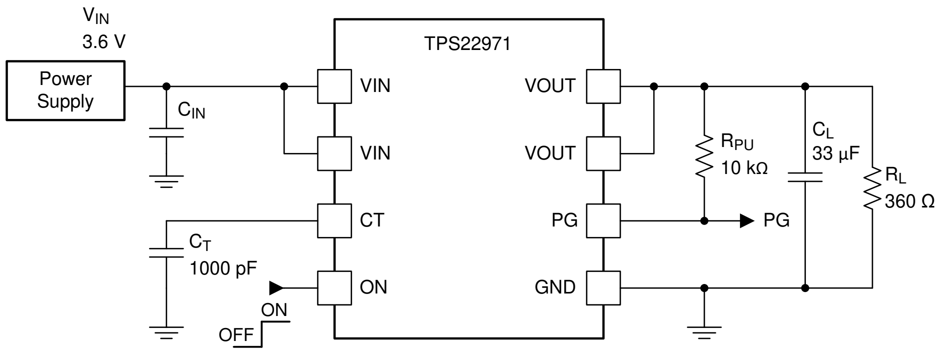


Figure 27. Typical Application

9.2.1 Design Requirements

For this design example, below, use the input parameters shown in Table 2.

Table 2. Design Parameters

DESIGN PARAMETER	VALUE
V_{IN}	3.6 V
I_{LOAD}	10 mA
Load capacitance (C_L)	33 µF
Maximum voltage drop	1%
Maximum inrush current	630 mA

9.2.2 Detailed Design Procedure

9.2.2.1 Maximum Voltage Drop and On-Resistance

At 3.6-V input voltage, with a maximum voltage drop tolerance of 1%, the TPS22971 has a typical R_{ON} of 6.7 mΩ. The rail is supplying 10 mA of current; the voltage drop for a rail is calculated based on Equation 10.

$$V_{DROP} = R_{ON} \times I_{LOAD} \quad (10)$$

$$V_{DROP} = 0.067\ mV \quad (11)$$

The maximum voltage drop is 1% which is 36 mV. The voltage drop caused by the load current across the on resistance is 0.067 mV.

9.2.2.2 Managing Inrush Current

When the switch is enabled, the output capacitors must be charged up from 0 V to V_{IN}. This charge arrives in the form of inrush current. Given a load capacitance (C_L) of 33 µF, an input voltage (V_{IN}) of 3.6V and a maximum inrush (I_{INRUSH}) of 630 mA, use Equation 12 and Equation 13 to solve for Slew Rate (SR).

$$SR = \frac{I_{INRUSH}}{C_L} \quad (12)$$

$$SR = 0.0191\ V / \mu s \quad (13)$$

Now that the desired slew rate has been calculated, use SR and V_{IN} in in Equation 14 to calculate a CT capacitance value.

$$CT\left(VIN, SR\right) = 1007\ pF \quad (14)$$

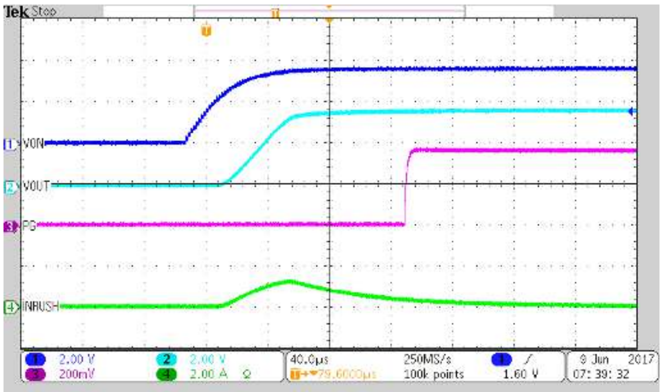
A capacitance value of 1007pF is a non-standard value therefore a 1000 pF CT capacitance is used moving forward.

The calculated CT value can be used with Equation 2 and Equation 4 to determine t_{ON} and $t_{PG,ON}$, respectively as shown in Equation 15 and Equation 16.

$$t_{ON}\left(VIN, CT\right) = 182.8\ \mu s \quad (15)$$

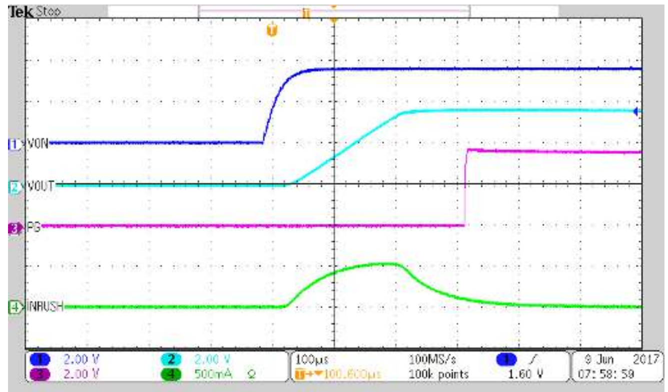
$$t_{PG,ON}\left(VIN, CT\right) = 293.1\ \mu s \quad (16)$$

9.2.3 Application Curves



V_{IN} = 3.6 V V_{ON} = 3.6 V C_{IN} = 1 µF
R_L = OPEN T_A = 25°C C_L = 33 µF

Figure 28. TPS22971 Inrush Current With C_T = 0 pF



V_{IN} = 3.6 V V_{ON} = 3.6 V C_{IN} = 1 µF
R_L = OPEN T_A = 25°C C_L = 33 µF

Figure 29. TPS22971 Inrush Current With C_T = 1000 pF

10 Power Supply Recommendations

The device is designed to operate from a VIN range of 0.65 V to 3.6 V. The V_{IN} power supply must be well regulated and placed as close to the device terminal as possible. The power supply must be able to withstand all transient load current steps. In most situations, using an input capacitance of 1 µF is sufficient to prevent the supply voltage from dipping when the switch is turned on. In cases where the power supply is slow to respond to a large transient current or large load current step, additional bulk capacitance may be required on the input.

The requirements for larger input capacitance can be mitigated by adding additional capacitance to the CT pin. This causes the load switch to turn on more slowly. Not only does this reduce transient inrush current, but it also gives the power supply more time to respond to the load current step.

11 Layout

11.1 Layout Guidelines

All traces must be as short as possible for best performance. Using wide traces for V_{IN}, V_{OUT}, and GND helps minimize the parasitic electrical effects along with minimizing the thermal impedance. The CT trace must be as short as possible to reduce parasitic capacitance.

11.2 Layout Example

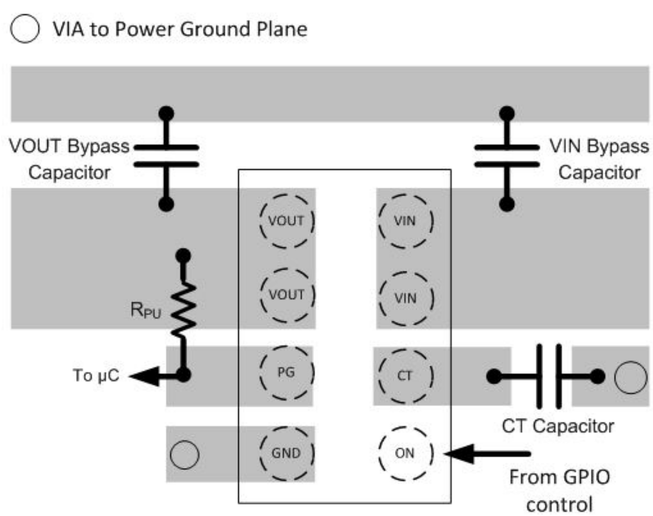


Figure 30. Package Layout Examples

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

TPS22971 Load Switch Evaluation Module User's Guide

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

SLYZ022 — *TI Glossary*.
This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS22971YZPR	ACTIVE	DSBGA	YZP	8	3000	RoHS & Green	SAC396 | SNAGCU	Level-1-260C-UNLIM	-40 to 85	1CKI	Samples
TPS22971YZPT	ACTIVE	DSBGA	YZP	8	250	RoHS & Green	SAC396 | SNAGCU	Level-1-260C-UNLIM	-40 to 85	1CKI	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

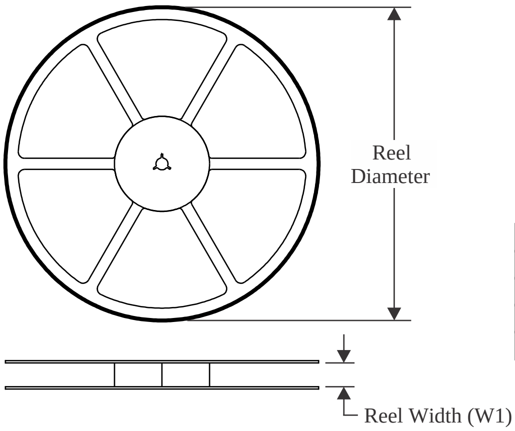
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

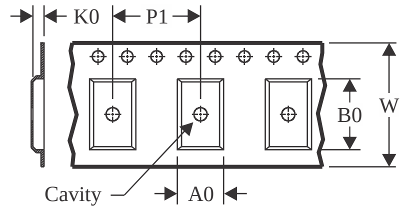
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

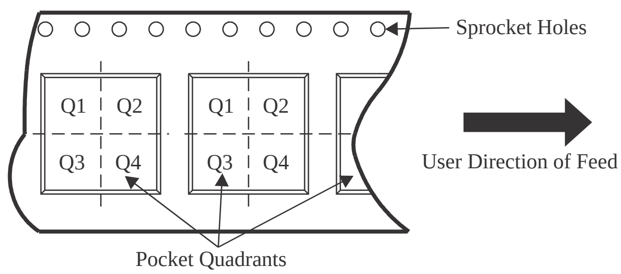


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

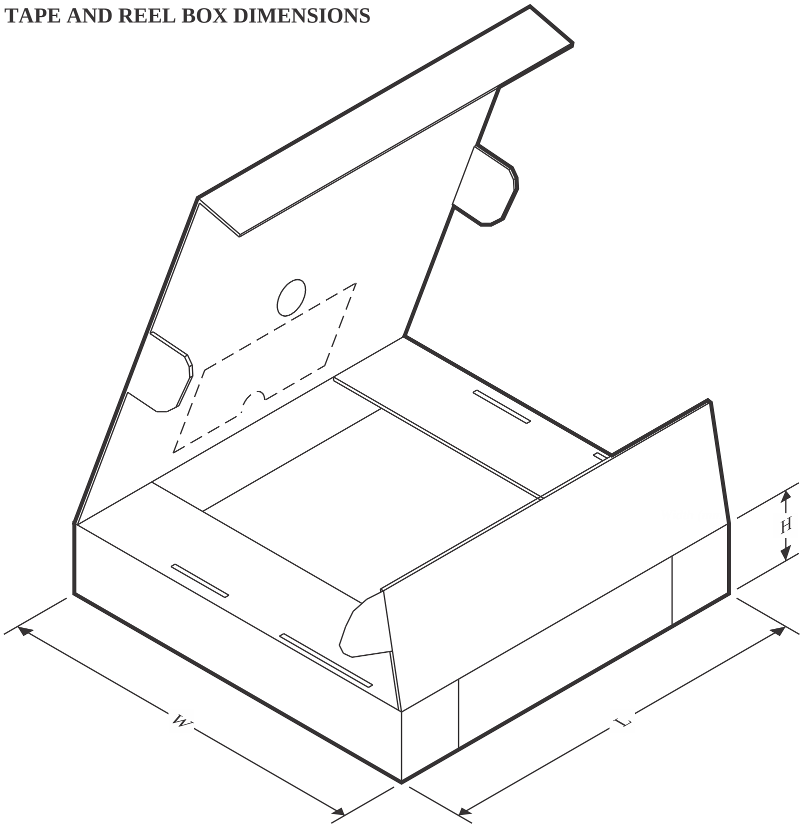
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

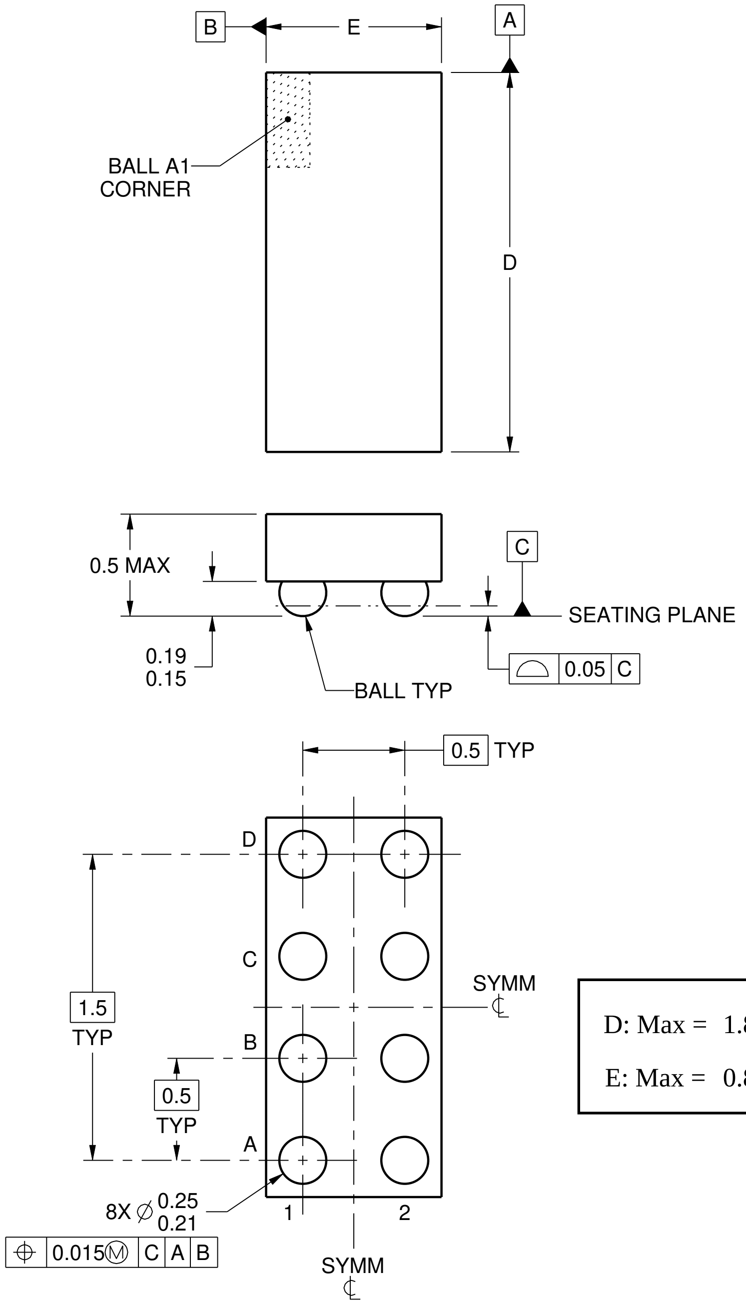
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS22971YZPR	DSBGA	YZP	8	3000	180.0	8.4	1.0	2.06	0.63	2.0	8.0	Q1
TPS22971YZPR	DSBGA	YZP	8	3000	180.0	8.4	1.02	2.02	0.63	2.0	8.0	Q1
TPS22971YZPT	DSBGA	YZP	8	250	180.0	8.4	1.0	2.06	0.63	2.0	8.0	Q1
TPS22971YZPT	DSBGA	YZP	8	250	180.0	8.4	1.02	2.02	0.63	2.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS22971YZPR	DSBGA	YZP	8	3000	182.0	182.0	20.0
TPS22971YZPR	DSBGA	YZP	8	3000	182.0	182.0	20.0
TPS22971YZPT	DSBGA	YZP	8	250	182.0	182.0	20.0
TPS22971YZPT	DSBGA	YZP	8	250	182.0	182.0	20.0



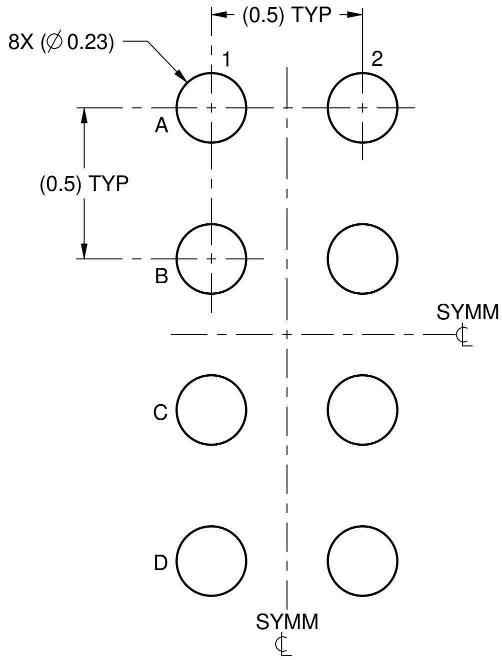
D: Max = 1.89 mm, Min = 1.83 mm

E: Max = 0.89 mm, Min = 0.83 mm

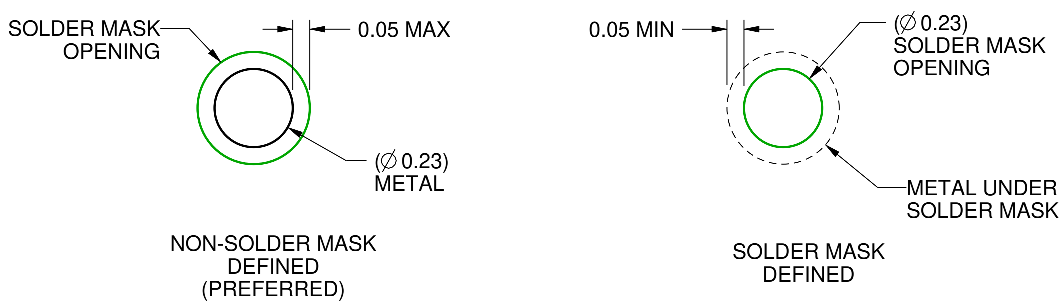
4223082/A 07/2016

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:40X

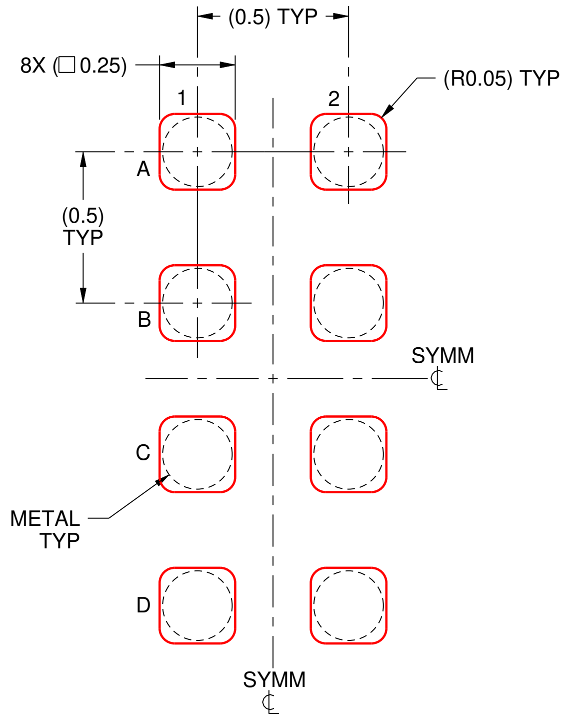


SOLDER MASK DETAILS
NOT TO SCALE

4223082/A 07/2016

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4223082/A 07/2016

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265