



# OCTAL D FLIP-FLOP WITH ENABLE; HEX D FLIP-FLOP WITH ENABLE; 4-BIT D FLIP-FLOP WITH ENABLE

The SN54/74LS377 is an 8-bit register built using advanced Low Power Schottky technology. This register consists of eight D-type flip-flops with a buffered common clock and a buffered common clock enable.

The SN54/74LS378 is a 6-Bit Register with a buffered common enable. This device is similar to the SN54/74LS174, but with common Enable rather than common Master Reset.

The SN54/74LS379 is a 4-Bit Register with buffered common Enable. This device is similar to the SN54/74LS175 but features the common Enable rather than common Master Reset.

- 8-Bit High Speed Parallel Registers
- Positive Edge-Triggered D-Type Flip Flops
- Fully Buffered Common Clock and Enable Inputs
- True and Complement Outputs
- Input Clamp Diodes Limit High Speed Termination Effects

## PIN NAMES

$\bar{E}$	Enable (Active LOW) Input
$D_0-D_3$	Data Inputs
CP	Clock (Active HIGH Going Edge) Input
$Q_0-Q_3$	True Outputs (Note b)
$\bar{Q}_0-\bar{Q}_3$	Complemented Outputs (Note b)

## NOTES:

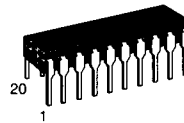
- a) 1 TTL Unit Load (U.L.) = 40  $\mu$ A HIGH/1.6 mA LOW.  
b) The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

LOADING (Note a)	
HIGH	LOW
0.5 U.L.	0.25 U.L.
0.5 U.L.	0.25 U.L.
0.5 U.L.	0.25 U.L.
10 U.L.	5 (2.5) U.L.
10 U.L.	5 (2.5) U.L.

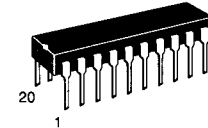
**SN54/74LS377  
SN54/74LS378  
SN54/74LS379**

**OCTAL D FLIP-FLOP WITH  
ENABLE; HEX D FLIP-FLOP  
WITH ENABLE; 4-BIT D FLIP-FLOP  
WITH ENABLE**

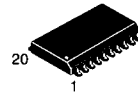
**LOW POWER SCHOTTKY**



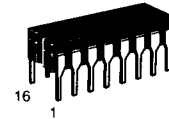
**J SUFFIX  
CERAMIC  
CASE 732-03**



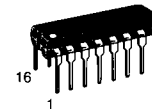
**N SUFFIX  
PLASTIC  
CASE 738-03**



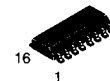
**DW SUFFIX  
SOIC  
CASE 751D-03**



**J SUFFIX  
CERAMIC  
CASE 620-09**



**N SUFFIX  
PLASTIC  
CASE 648-08**



**D SUFFIX  
SOIC  
CASE 751B-03**

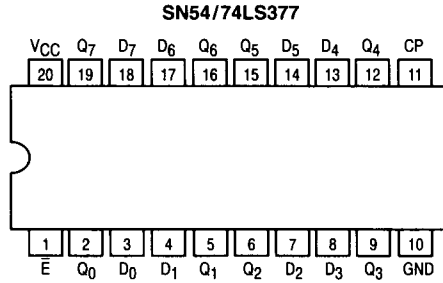
## ORDERING INFORMATION

SN54LSXXXJ	Ceramic
SN74LSXXXN	Plastic
SN74LSXXXDW	SOIC
SN74LSXXXD	SOIC

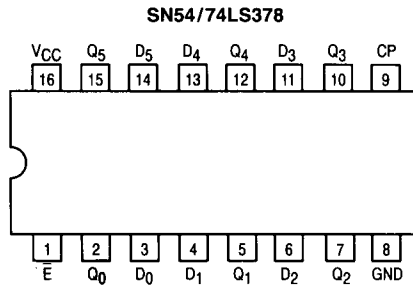
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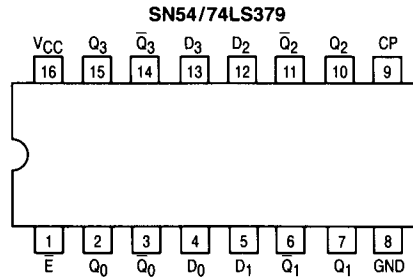
## CONNECTION DIAGRAM DIPS (TOP VIEW)



NOTE:  
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.



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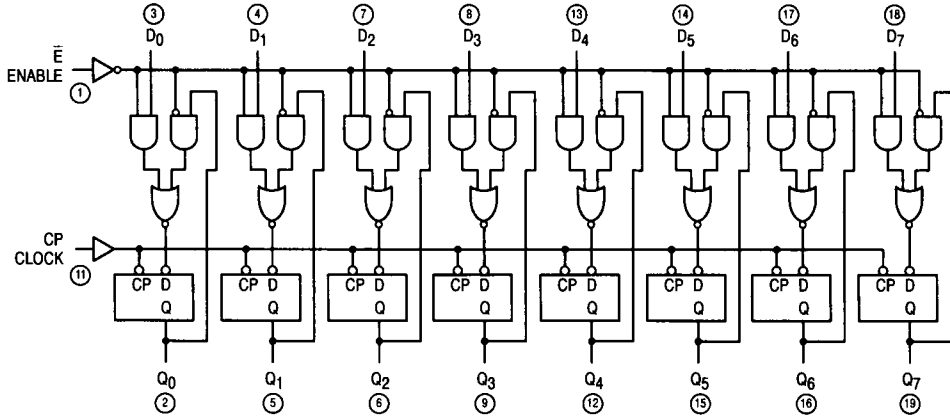


NOTE:  
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

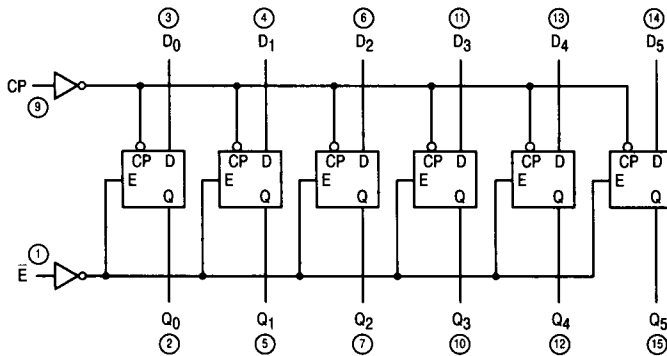
# SN54/74LS377 • SN54/74LS378 • SN54/74LS379

## LOGIC DIAGRAMS

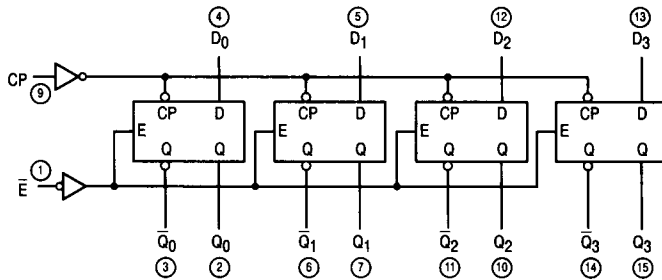
SN54/74LS377



SN54/74LS378



SN54/74LS379



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## GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V <sub>CC</sub>	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T <sub>A</sub>	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
I <sub>OH</sub>	Output Current — High	54, 74			-0.4	mA
I <sub>OL</sub>	Output Current — Low	54 74			4.0 8.0	mA

## DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V <sub>IL</sub>	Input LOW Voltage	54		0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74		0.8			
V <sub>IK</sub>	Input Clamp Diode Voltage		-0.65	-1.5	V	V <sub>CC</sub> = MIN, I <sub>IN</sub> = -18 mA	
V <sub>OH</sub>	Output HIGH Voltage	54	2.5	3.5	V	V <sub>CC</sub> = MIN, I <sub>OH</sub> = MAX, V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> per Truth Table	
		74	2.7	3.5	V		
V <sub>OL</sub>	Output LOW Voltage	54, 74		0.25	0.4	V	I <sub>OL</sub> = 4.0 mA I <sub>OL</sub> = 8.0 mA V <sub>CC</sub> = V <sub>CC</sub> MIN, V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> per Truth Table
		74		0.35	0.5	V	
I <sub>IH</sub>	Input HIGH Current			20	μA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 2.7 V	
				0.1	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 7.0 V	
I <sub>IL</sub>	Input LOW Current			-0.4	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 0.4 V	
I <sub>OS</sub>	Short Circuit Current (Note 1)		-20		-100	mA V <sub>CC</sub> = MAX	
I <sub>CC</sub>	Power Supply Current	LS377			28	mA V <sub>CC</sub> = MAX, NOTE 1	
		LS378			22		
		LS379			15		

NOTE: With all inputs open and GND applied to all data and enable inputs, I<sub>CC</sub> is measured after a momentary GND, then 4.5 V is applied to clock.

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

## AC CHARACTERISTICS (T<sub>A</sub> = 25°C, V<sub>CC</sub> = 5.0 V)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
f <sub>MAX</sub>	Maximum Clock Frequency	30	40		MHz	V <sub>CC</sub> = 5.0 V C <sub>L</sub> = 15 pF
t <sub>PLH</sub>	Propagation Delay, Clock to Output		17	27	ns	
t <sub>PHL</sub>			18	27		

## AC SETUP REQUIREMENTS (T<sub>A</sub> = 25°C, V<sub>CC</sub> = 5.0 V)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
t <sub>W</sub>	Any Pulse Width	20			ns	V <sub>CC</sub> = 5.0 V	
t <sub>S</sub>	Data Setup Time	20			ns		
t <sub>S</sub>	Enable Setup Time	Inactive — State	10				ns
		Active — State	25				ns
t <sub>H</sub>	Any Hold Time	5.0			ns		

## DEFINITION OF TERMS




SETUP TIME (t<sub>S</sub>) — is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW-to-HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t<sub>H</sub>) — is defined as the minimum time following

the clock transition from LOW-to-HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW-to-HIGH and still be recognized.

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## TRUTH TABLE

$\bar{E}$	CP	$D_n$	$Q_n$	$\bar{Q}_n$
H		X	No Change	No Change
L		H	H	L
L		L	L	H

L = LOW Voltage Level  
 H = HIGH Voltage Level  
 X = Immaterial

## AC WAVEFORMS

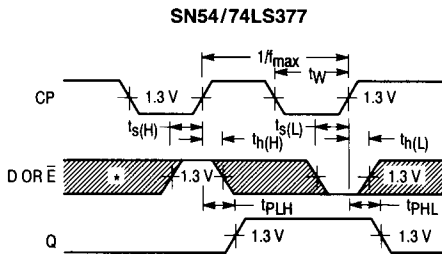


Figure 1. Clock to Output Delays Clock Pulse Width, Frequency, Setup and Hold Times Data or Enable to Clock

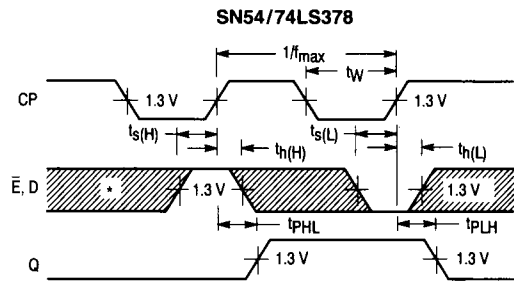
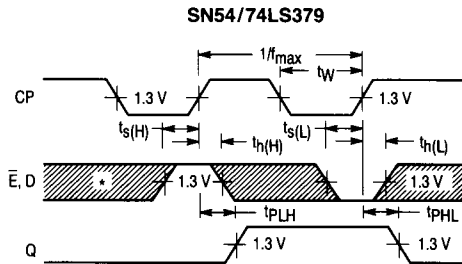


Figure 2. Clock to Output Delays Clock Pulse Width, Frequency, Setup and Hold Times Data or Enable to Clock



\*The shaded areas indicate when the input is permitted to change for predictable output performance.

Figure 3. Clock to Output Delays Clock Pulse Width, Frequency, Setup and Hold Times Data, Enable to Clock