BLF8G09LS-400PW; BLF8G09LS-400PGW Power LDMOS transistor

AMPLEON

Rev. 5 — 1 September 2015

Product data sheet

Product profile

1.1 General description

400 W LDMOS power transistor for base station applications at frequencies from 716 MHz to 960 MHz.

Table 1. Typical performance

Typical RF performance at T_{case} = 25 °C in a common source class-AB production test circuit, tested on straight lead device.

Test signal	f	I _{Dq}	V _{DS}	P _{L(AV)}	Gp	η_D	ACPR _{5M}
	(MHz)	(mA)	(V)	(W)	(dB)	(%)	(dBc)
2-carrier W-CDMA	716 to 728	3400	28	95	20.6	30	-35 <u>[1]</u>

[1] 3GPP test model 1; 64 DPCH; PAR = 8.4 dB at 0.01 % probability on CCDF; 10 MHz carrier spacing.

1.2 Features and benefits

- Excellent ruggedness
- Device can operate with the supply current delivered through the video leads
- High efficiency
- Low thermal resistance providing excellent thermal stability
- Designed for broadband operation
- Lower output capacitance for improved performance in Doherty applications
- Decoupling leads to enable improved video bandwidth (45 MHz typical)
- Designed for low memory effects providing excellent pre-distortability
- Internally matched for ease of use
- Integrated ESD protection
- Design optimized for gull-wing
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

1.3 Applications

RF power amplifiers for base stations and multi carrier applications in the 716 MHz to 960 MHz frequency range

2. Pinning information

Table 2. Pinning

		01 1161 1 411	
Pin	Description	Simplified outline	Graphic symbol
BLF8G09L	S-400PW (SOT1242B)		
1	drain1	6 1 2 7	4
2	drain2		6
3	gate1		8 -
4	gate2		3——5
5	source [1]	0 0 1	4———3
6	decoupling1 [2]	5	9•
7	decoupling2 [2]		7
8	n.c.		aaa-007816
9	n.c.		
BLF8G09L	S-400PGW (SOT1242C)		
1	drain1	0 4 0 7	
2	drain2	6 1 2 7	6
3	gate1		8 -
4	gate2	8 3 4 9	3——5
5	source [1]	5	4——5
6	decoupling1		9 •
7	decoupling2		7
8	n.c.		aaa-007816
9	n.c.		

^[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Packag	Package		
	Name	Description	Version	
BLF8G09LS-400PW	-	earless flanged ceramic package; 8 leads	SOT1242B	
BLF8G09LS-400PGW	-	earless flanged ceramic package; 8 leads	SOT1242C	

^[2] Device can operate with the supply current delivered through the combined decoupling leads.

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	65	V
V_{GS}	gate-source voltage		-0.5	+13	V
T _{stg}	storage temperature		-65	+150	°C
Tj	junction temperature	[1]	-	225	°C

^[1] Continuous use at maximum temperature will affect the reliability, for details refer to the on-line MTF calculator

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Тур	Unit
R _{th(j-c)}	thermal resistance from junction to case	T _{case} = 80 °C; P _L = 95 W	0.26	K/W

6. Characteristics

Table 6. DC characteristics

 T_i = 25 °C; per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V _{(BR)DSS}	drain-source breakdown voltage	$V_{GS} = 0 \text{ V}; I_D = 3 \text{ mA}$	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V _{DS} = 10 V; I _D = 300 mA	1.5	1.8	2.3	V
V_{GSq}	gate-source quiescent voltage	V _{DS} = 28 V; I _D = 1700 mA	1.7	2	2.5	V
I _{DSS}	drain leakage current	V _{GS} = 0 V; V _{DS} = 28 V	-	-	2.8	μА
I _{DSX}	drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75 \text{ V};$ $V_{DS} = 10 \text{ V}$		55	-	A
I _{GSS}	gate leakage current	V _{GS} = 11 V; V _{DS} = 0 V	-	-	280	nA
9 _{fs}	forward transconductance	V _{DS} = 10 V; I _D = 15 A	-	26	-	S
R _{DS(on)}	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75 V;$ $I_D = 12.25 A$	-	0.06	-	Ω

Table 7. RF characteristics

Test signal: 2-carrier W-CDMA; PAR = 8.4 dB at 0.01 % probability on the CCDF; 3GPP test model 1; 1-64 DPCH; f_1 = 718.5 MHz; f_2 = 723.5 MHz; f_3 = 720.5 MHz; f_4 = 725.5 MHz; RF performance at V_{DS} = 28 V; I_{Dq} = 3400 mA; T_{case} = 25 °C; unless otherwise specified; in a class-AB production test circuit, tested on straight lead device.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Gp	power gain	P _{L(AV)} = 95 W	18.8	20.6	-	dB
RLin	input return loss	P _{L(AV)} = 95 W	-	-19	-11	dB
η_{D}	drain efficiency	P _{L(AV)} = 95 W	26	30	-	%
ACPR _{5M}	adjacent channel power ratio (5 MHz)	P _{L(AV)} = 95 W	-	-35	-32	dBc

7. Test information

7.1 Ruggedness in class-AB operation

The BLF8G09LS-400PW and BLF8G09LS-400PGW are capable of withstanding a load mismatch corresponding to VSWR = 7 : 1 through all phases under the following conditions: V_{DS} = 28 V; I_{Dq} = 3400 mA; 2-carrier W-CDMA signal; P_L = 200 W; f = 716 MHz; 5 MHz carrier spacing; 46 % clipping.

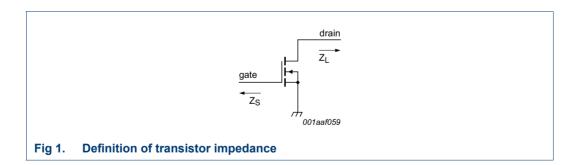
7.2 Impedance information

Table 8. Typical impedance

Measured load-pull data for the top-half of the push-pull package; I_{Dq} = 1800 mA; V_{DS} = 28 V; T_{case} = 25 °C, water cooled.

f	Z _S [1]	Z _L [1]
(MHz)	(Ω)	(Ω)
BLF8G09LS-400PW (straight le	ead)	
720	1.26 – j2.89	1.8 – j1.94
757	1.44 – j3.82	2 – j1.6
769	1.55 – j3.64	1.9 – j1.75
805	1.7 – j4.5	1.5 – j1.3
BLF8G09LS-400PGW (gull-win	g)	
720	1.37 – j3	1.7 – j2.1
757	1.4 – j3.6	1.6 – j2.3
769	1.3 – j3.9	1.7 – j2.2
805	1.6 – j4.3	1.48 – j1.97

[1] Z_S and Z_L defined in Figure 1.



7.3 VBW in class-AB operation

The BLF8G09LS-400PW and BLF8G09LS-400PGW show 45 MHz (typical) video bandwidth in class-AB test circuit in 722 MHz band at V_{DS} = 28 V and I_{Dq} = 3400 mA.

7.4 Test circuit

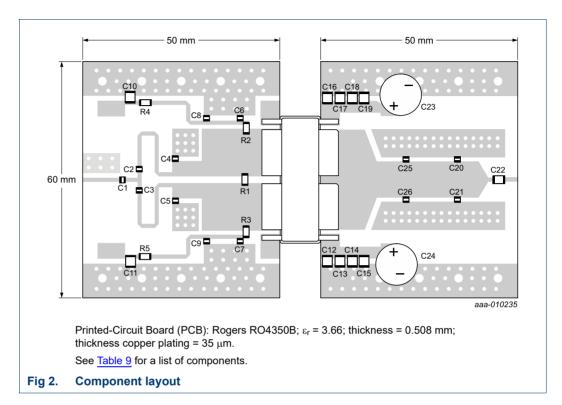


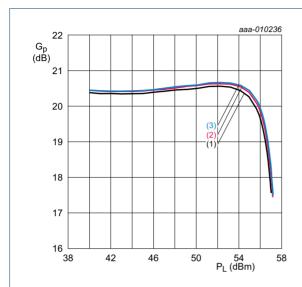
Table 9. List of components

For test circuit see Figure 2.

Component	Description	Value	Remarks
C1, C2, C3, C8, C9	multilayer ceramic chip capacitor	100 pF	ATC 100A
C4, C5	multilayer ceramic chip capacitor	9.1 pF	ATC 100A
C6, C7	multilayer ceramic chip capacitor	10 pF	ATC 100A
C10, C11, C13, C17	multilayer ceramic chip capacitor	1 μF, 50 V	Murata
C12, C16	multilayer ceramic chip capacitor	100 nF, 50 V	Murata
C14, C15, C18, C19	multilayer ceramic chip capacitor	10 μF, 50 V	Murata
C20, C21	multilayer ceramic chip capacitor	5.1 pF	ATC 100A
C22	multilayer ceramic chip capacitor	82 pF	ATC 100B
C23, C24	electrolytic capacitor	470 μF, 63 V	
C25, C26	multilayer ceramic chip capacitor	3 pF	ATC 100A
R1	resistor	10 Ω	
R2, R3, R4, R5	resistor	5.1 Ω	

7.5 Graphical data

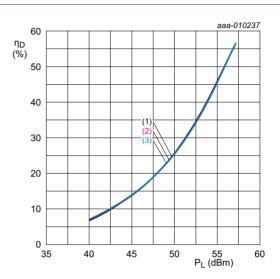
7.5.1 Pulsed CW



 V_{DS} = 28 V; I_{Dq} = 3400 mA; t_p = 100 $\mu s; \, \delta$ = 10 %.

- (1) f = 716 MHz
- (2) f = 722 MHz
- (3) f = 728 MHz

Fig 3. Power gain as a function of output power; typical values

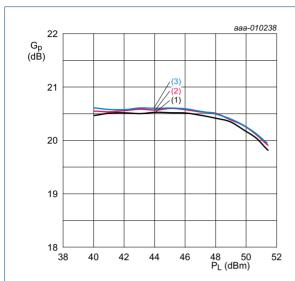


 V_{DS} = 28 V; I_{Dq} = 3400 mA; t_p = 100 $\mu s; \, \delta$ = 10 %.

- (1) f = 716 MHz
- (2) f = 722 MHz
- (3) f = 728 MHz

Fig 4. Drain efficiency as a function of output power; typical values

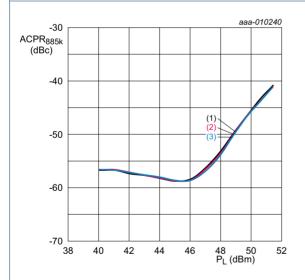
7.5.2 IS-95



 $V_{DS} = 28 \text{ V}; I_{Dq} = 3400 \text{ mA}.$

- (1) f = 716 MHz
- (2) f = 722 MHz
- (3) f = 728 MHz

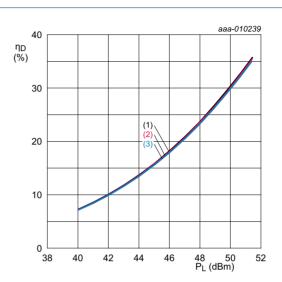
Fig 5. Power gain as a function of output power; typical values



 $V_{DS} = 28 \text{ V}; I_{Dq} = 3400 \text{ mA}.$

- (1) f = 716 MHz
- (2) f = 722 MHz
- (3) f = 728 MHz

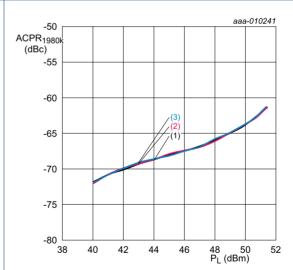
Fig 7. Adjacent channel power ratio (885 kHz) as a function of output power; typical values



 $V_{DS} = 28 \text{ V}; I_{Dq} = 3400 \text{ mA}.$

- (1) f = 716 MHz
- (2) f = 722 MHz
- (3) f = 728 MHz

Fig 6. Drain efficiency as a function of output power; typical values

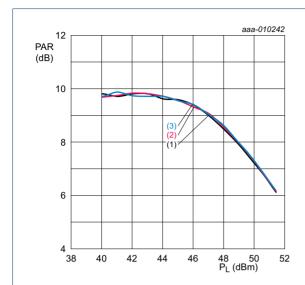


 $V_{DS} = 28 \text{ V}; I_{Dq} = 3400 \text{ mA}.$

- (1) f = 716 MHz
- (2) f = 722 MHz
- (3) f = 728 MHz

Fig 8. Adjacent channel power ratio (1980 kHz) as a function of output power; typical values

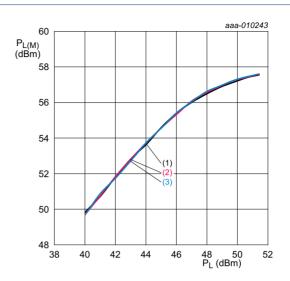
Power LDMOS transistor



 $V_{DS} = 28 \text{ V}; I_{Dq} = 3400 \text{ mA}.$

- (1) f = 716 MHz
- (2) f = 722 MHz
- (3) f = 728 MHz

Fig 9. Peak-to-average ratio as a function of output power; typical values

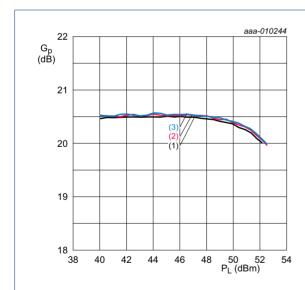


 $V_{DS} = 28 \text{ V}; I_{Dq} = 3400 \text{ mA}.$

- (1) f = 716 MHz
- (2) f = 722 MHz
- (3) f = 728 MHz

Fig 10. Peak output power as a function of output; typical values

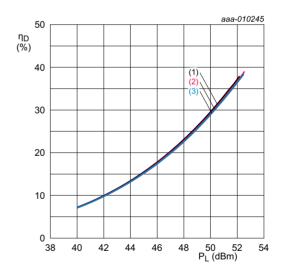
7.5.3 1-Carrier W-CDMA



 V_{DS} = 28 V; I_{Dq} = 3400 mA.

- (1) f = 716 MHz
- (2) f = 722 MHz
- (3) f = 728 MHz

Fig 11. Power gain as a function of output power; typical values

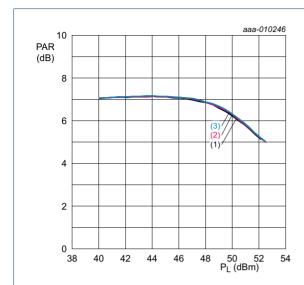


 $V_{DS} = 28 \text{ V}; I_{Dq} = 3400 \text{ mA}.$

- (1) f = 716 MHz
- (2) f = 722 MHz
- (3) f = 728 MHz

Fig 12. Drain efficiency as a function of output power; typical values

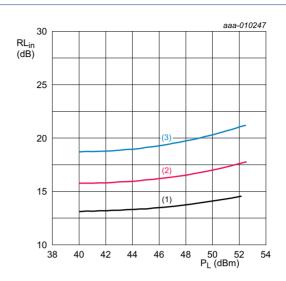
Power LDMOS transistor



 $V_{DS} = 28 \text{ V}; I_{Dq} = 3400 \text{ mA}.$

- (1) f = 716 MHz
- (2) f = 722 MHz
- (3) f = 728 MHz

Fig 13. Peak-to-average ratio as a function of output power; typical values

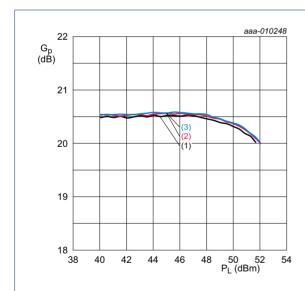


 $V_{DS} = 28 \text{ V}; I_{Dq} = 3400 \text{ mA}.$

- (1) f = 716 MHz
- (2) f = 722 MHz
- (3) f = 728 MHz

Fig 14. Input return loss as a function of output power; typical values

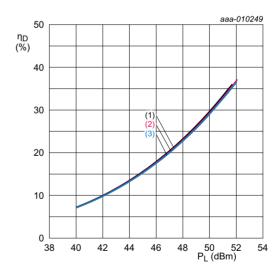
7.5.4 2-Carrier W-CDMA



 V_{DS} = 28 V; I_{Dq} = 3400 mA.

- (1) f = 716 MHz
- (2) f = 722 MHz
- (3) f = 728 MHz

Fig 15. Power gain as a function of output power; typical values

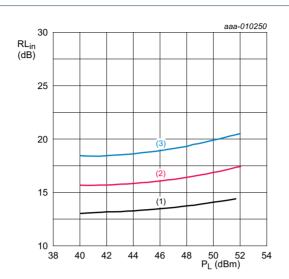


 V_{DS} = 28 V; I_{Dq} = 3400 mA.

- (1) f = 716 MHz
- (2) f = 722 MHz
- (3) f = 728 MHz

Fig 16. Drain efficiency as a function of output power; typical values

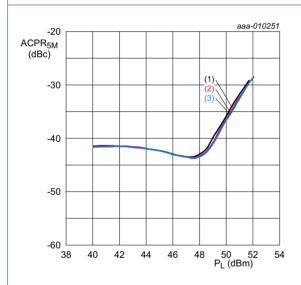
Power LDMOS transistor



 $V_{DS} = 28 \text{ V}; I_{Dq} = 3400 \text{ mA}.$

- (1) f = 716 MHz
- (2) f = 722 MHz
- (3) f = 728 MHz

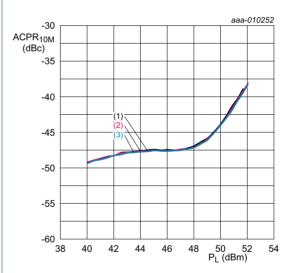
Fig 17. Input return loss as a function of output power; typical values



 $V_{DS} = 28 \text{ V}; I_{Dq} = 3400 \text{ mA}.$

- (1) f = 716 MHz
- (2) f = 722 MHz
- (3) f = 728 MHz

Fig 18. Adjacent channel power ratio (5 MHz) as a function of output power; typical values

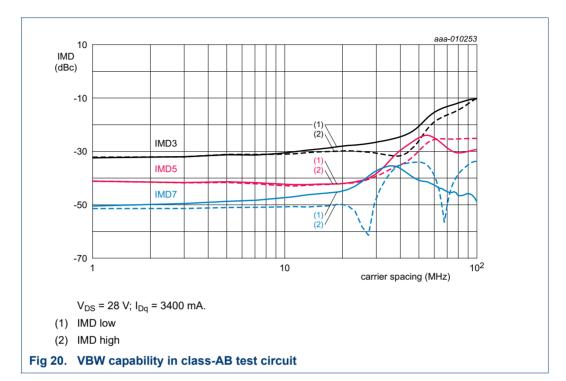


 V_{DS} = 28 V; I_{Dq} = 3400 mA.

- (1) f = 716 MHz
- (2) f = 722 MHz
- (3) f = 728 MHz

Fig 19. Adjacent channel power ratio (10 MHz) as a function of output power; typical values

7.5.5 2-Tone VBW



8. Package outline

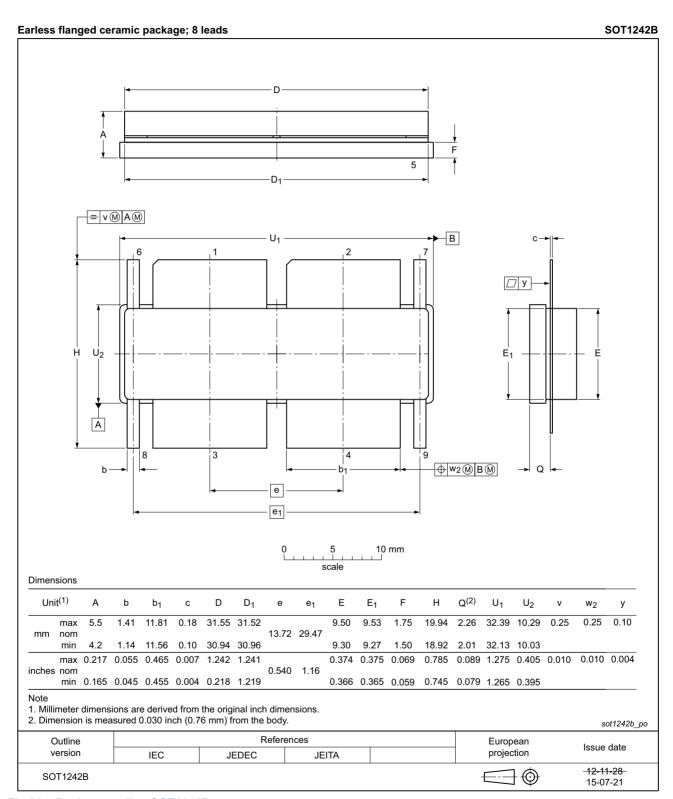


Fig 21. Package outline SOT1242B

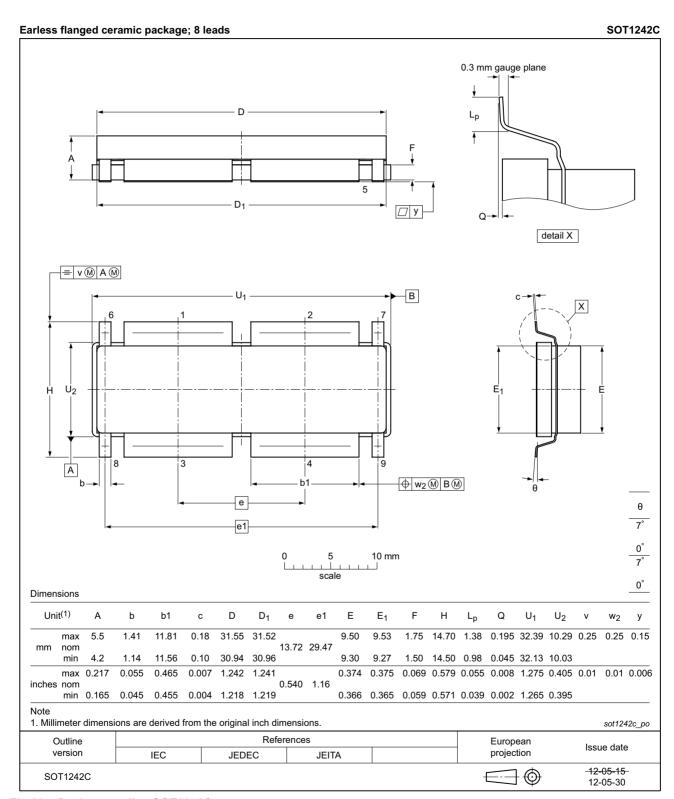


Fig 22. Package outline SOT1242C

9. Handling information

CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

10. Abbreviations

Table 10. Abbreviations

Acronym	Description	
3GPP	3rd Generation Partnership Project	
CCDF	Complementary Cumulative Distribution Function	
CW	Continuous Wave	
DPCH	Dedicated Physical CHannel	
ESD	ElectroStatic Discharge	
IS-95	Interim Standard 95	
LDMOS	Laterally Diffused Metal Oxide Semiconductor	
MTF	Median Time to Failure	
PAR	Peak-to-Average Ratio	
VBW	Video Bandwidth	
VSWR	Voltage Standing Wave Ratio	
W-CDMA	Wideband Code Division Multiple Access	

11. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLF8G09LS-400PW_ 8G09LS-400PGW#5	20150901	Product data sheet	-	BLF8G09LS-400PW_ 8G09LS-400PGW v.4
Modifications:	 The format of this document has been redesigned to comply with the new identity guidelines Ampleon. Legal texts have been adapted to the new company name where appropriate. 			
	• Legal texts have	e been adapted to the new compa	any name wnere approp	oriate.
BLF8G09LS-400PW_ 8G09LS-400PGW v.4	20150728	Product data sheet	-	BLF8G09LS-400PW_ 8G09LS-400PGW v.3
BLF8G09LS-400PW_ 8G09LS-400PGW v.3	20140324	Product data sheet	-	BLF8G09LS-400PW_ 8G09LS-400PGW v.2
BLF8G09LS-400PW_ 8G09LS-400PGW v.2	20131220	Preliminary data sheet	-	BLF8G09LS-400PW_ 8G09LS-400PGW v.1
BLF8G09LS-400PW_ 8G09LS-400PGW v.1	20130927	Objective data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition	
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.	
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.	
Product [short] data sheet	Production	This document contains the product specification.	

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions"
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Power LDMOS transistor

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For sales office addresses, please visit: http://www.ampleon.com/sales

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BLF8G09LS-400P(G)W

Power LDMOS transistor

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