TPS6224X-Q1 Automotive 2.25MHz 300mA Step-Down Converter in TSOT23 Package

1 Features

- AEC-Q100 Qualified with following results:
  - Device Temperature Grade 1: -40°C to 125°C Operating Junction Temeperature Range
- Output Current Up to 300 mA
- V_{IN} Range From 2 V to 6 V
- 2.25-MHz Fixed-Frequency Operation in PWM Mode
- Power-Save Mode at Light Load Currents
- Output Voltage Accuracy in PWM Mode ±1.5%
- Fixed Output Voltages
  - 1.80V TPS62243-Q1
  - 1.25V TPS62244-Q1
- 15-µA Typical Quiescent Current
- 100% Duty Cycle for Lowest Dropout
- Available in a TSOT 23 (5) 2.90-mm × 1.60-mm Package

2 Applications

- Remote Keyless Entry (RKE)
- Passive Entry Passive Start (PEPS)
- Advanced Driver Assistance Systems (ADAS)
  - Front Camera, Surround View, and Park Assist

3 Description

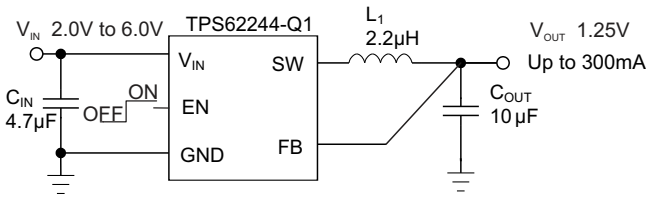
The TPS6224x-Q1 devices are high-efficiency synchronous DC/DC step-down converters providing a fixed output voltage and up to 300 mA of output current. They offer low power consumption for battery-powered/always-on automotive applications like Remote Keyless Entry (RKE) or Passive Entry Passive Start (PEPS) key fobs and base stations. With an input voltage range of 2 V to 6 V, the devices support applications powered by Li-MnO2 coin cell batteries, Li-Ion batteries, two- (2S) and three-cell (3S) alkaline, 3.3-V and 5-V input voltage rails. The TPS6224x-Q1 operate at a 2.25-MHz fixed switching frequency at high load current and enters the power-save mode operation at light load currents to maintain high efficiency and low power consumption over the entire load current range. The power-save mode is optimized for low output-voltage ripple. In the shutdown mode, the current consumption is reduced to less than 1 µA. The TPS6224x-Q1 allow the use of small inductors and capacitors to achieve a small solution size, and is available in a 5-pin TSOT23 package.

Device Information(1)

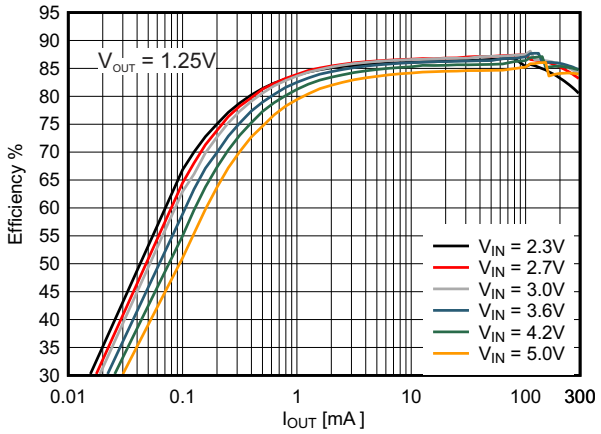
PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS6224X-Q1	TSOT (5)	2.90 mm × 1.60 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Schematic



Efficiency vs Output Current



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4 Revision History

DATE	REVISION	NOTES
March 2018	*	Initial release.

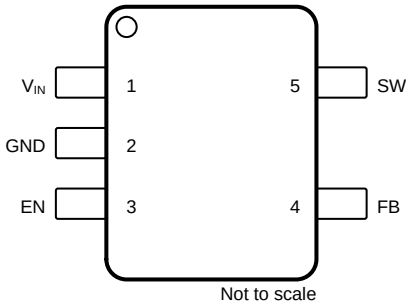
5 Device Comparison Table

PART NUMBER(1)	FIXED OUTPUT VOLTAGES [V]	OPERATING MODE
TPS62243-Q1	1.80 V	PFM/PWM with automatic transition
TPS62244-Q1	1.25 V	PFM/PWM with automatic transition

(1) For all available packages, see the orderable addendum at the end of the data sheet.

6 Pin Configuration and Functions

DDC Package
5-Pin SOT
Top View



Not to scale

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
EN	3	I	This is the enable pin of the device. Pulling this pin to low forces the device into shutdown mode. Pulling this pin to high enables the device. This pin must be terminated.
FB	4	I	Feedback Pin for the internal regulation loop. Connect the external resistor divider to this pin. In case of fixed output voltage option, connect this pin directly to the output capacitor.
GND	2	PWR	GND supply pin.
SW	5	O	This is the switch pin and is connected to the internal MOSFET switches. Connect the inductor to this terminal.
V_{IN}	1	PWR	V_{IN} power supply pin.

7 Specifications

7.1 Absolute Maximum Ratings(1)

		MIN	MAX	UNIT
V_I	Input voltage(2)	–0.3	7	V
	Voltage at EN	–0.3	V_{IN} + 0.3, ≤7	V
	Voltage on SW	–0.3	7	V
	Peak output current	Internally limited		A
T_J	Maximum operating junction temperature	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 (1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_I	Supply voltage, VIN	2	6	V
I_{OUT}	Output current, 2.3V < VIN < 6V		300	mA
	Output current, 2V ≤ VIN ≤ 2.3V		150	mA
L	Inductance	1.5	4.7	µH
C_{OUT}	Output capacitance	4.7	10	µF
T_J	Operating junction temperature	–40	125	°C

7.4 Thermal Information

THERMAL METRIC (1)		TPS6224X-Q1 DDC (TSOT 23) 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	193.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	40.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	35	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	34.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

T_J = -40°C to 125°C, typical values are at T_J = 25°C, unless otherwise noted. Specifications apply for condition V_{IN} = 3.6 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
I_Q	Operating quiescent current	I_{OUT} = 0 mA. Pulse frequency modulation (PFM) mode enabled, device not switching		15		µA
		I_{OUT} = 0 mA. PFM mode enabled, device switching, V_{OUT} = 1.25 V		18.5		
I_{SD}	Shutdown current	EN = GND, T_J = 25°C		0.1	1	µA
		EN = GND			10	
UVLO	Undervoltage lockout threshold	Falling		1.85		V
		Rising		1.95		
ENABLE, MODE						
V_{IH}	High-level input voltage, EN	2 V ≤ V_{IN} ≤ 6 V	1		V_{IN}	V
V_{IL}	Low-level input voltage, EN	2 V ≤ V_{IN} ≤ 6 V,	0		0.35	V
I_{IN}	Input bias current, EN	EN, MODE = GND or V_{IN}		0.01	1	µA
POWER SWITCH						
$R_{DS(on)}$	High-side MOSFET ON-resistance	V_{IN} = V_{GS} = 3.6 V, T_J = 25°C		240	480	mΩ
	Low-side MOSFET ON-resistance			180	380	
I_{LIMF}	Forward current limit MOSFET high-side and low-side	V_{IN} = V_{GS} = 3.6 V,	0.54		0.95	A
TSD	Thermal shutdown	Increasing junction temperature		140		°C
	Thermal shutdown hysteresis	Decreasing junction temperature		20		°C
OSCILLATOR						
f_{SW}	Oscillator frequency	2 V ≤ V_{IN} ≤ 6 V, PWM Mode	2	2.25	2.5	MHz
OUTPUT						
V_{OUT}	Output voltage	TPS62244 Q1 (fixed V_{OUT})		1.25		V
		TPS62243 Q1 (fixed V_{OUT})		1.80		V
V_{REF}	Internal reference voltage			600		mV
V_{FB}	Feedback voltage	PWM operation, 2 V ≤ V_{IN} ≤ 6 V, in fixed output voltage versions V_{FB} = V_{OUT}, See (1) ,T_J = 25°C	–1.5%	0%	1.5%	
		PWM operation, 2 V ≤ V_{IN} ≤ 6 V, in fixed output voltage versions V_{FB} = V_{OUT}, See (1)	–1.5%		2.5%	
	Feedback voltage PFM mode	Device in PFM mode		0%		
	Load regulation	PWM mode		–0.5		%/A
$t_{Start\ up}$	Start-up time	Time from active EN to reach 95% of V_{OUT} nominal		500		µs
t_{Ramp}	V_{OUT} ramp UP time	Time to ramp from 5% to 95% of V_{OUT}		250		µs
I_{lkg}	Leakage current into SW pin	V_{IN} = 3.6 V, V_{IN} = V_{OUT} = V_{SW}, EN = GND, T_J = 25°C (2)		0.1	1	µA
		V_{IN} = 3.6 V, V_{IN} = V_{OUT} = V_{SW}, EN = GND, (2)			10	

(1) For V_{IN} = V_O+ 0.6
(2) The internal resistor divider network is disconnected from FB pin.

7.6 Typical Characteristics

Table 1. Table of Graphs

		FIGURE
Shutdown Current into VIN	vs Input Voltage	Figure 1
Quiescent Current	vs Input Voltage	Figure 2
Static Drain-Source On-State Resistance	vs Input Voltage	Figure 3
		Figure 4

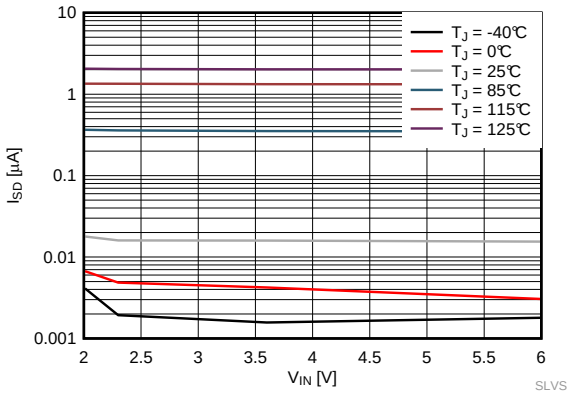


Figure 1. Shutdown Current vs Input Voltage

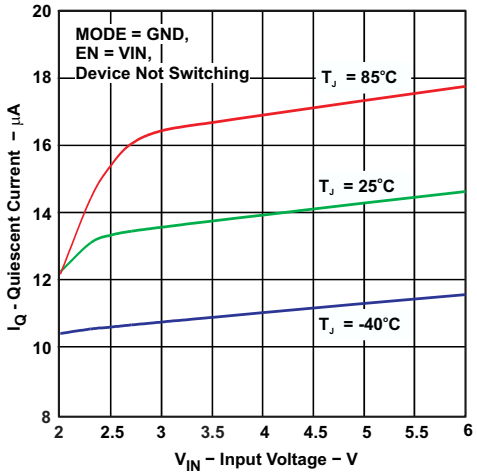


Figure 2. Quiescent Current vs Input Voltage

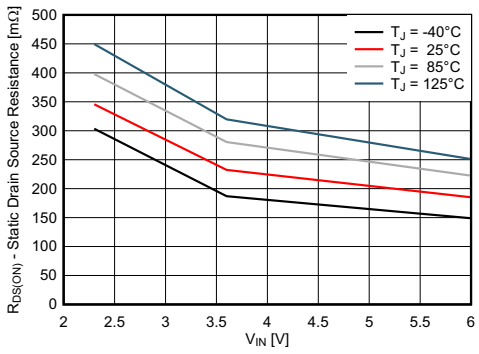


Figure 3. High Side Switch Static Drain-Source On-State Resistance vs Input Voltage

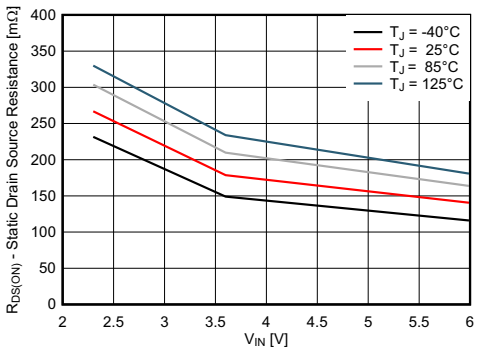


Figure 4. Low Side Switch Static Drain-Source On-State Resistance vs Input Voltage

8 Detailed Description

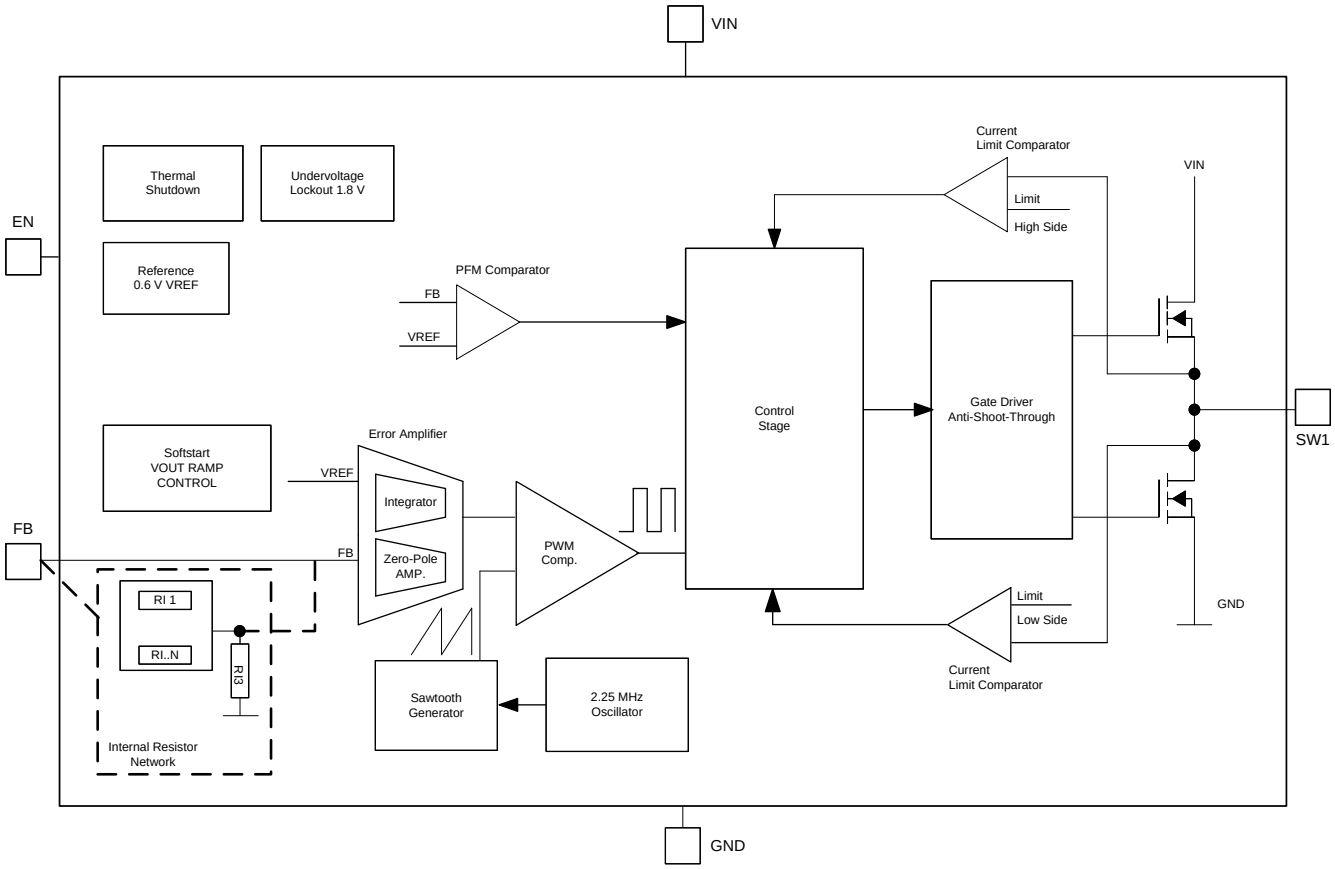
8.1 Overview

The TPS6224X-Q1 step-down converter typically operates with 2.25-MHz fixed-frequency pulse width modulation (PWM) at moderate to heavy load currents. At light load currents, the converter can automatically enter power save mode and then operates in PFM mode.

During PWM operation, the converter uses a unique fast-response voltage-mode control scheme with input voltage feed-forward to achieve good line and load regulation, allowing the use of small ceramic input and output capacitors. At the beginning of each clock cycle initiated by the clock signal, the high-side MOSFET switch is turned on. The current then flows from the input capacitor through the high-side MOSFET switch through the inductor to the output capacitor and load. During this phase, the current ramps up until the PWM comparator trips and the control logic turns off the switch. The current limit comparator also turns off the switch if the current limit of the high-side MOSFET switch is exceeded. After a dead time preventing shoot-through current, the low-side MOSFET rectifier is turned on and the inductor current ramps down. The current then flows from the inductor to the output capacitor and to the load. It returns back to the inductor through the low-side MOSFET rectifier.

The next cycle is initiated by the clock signal again turning off the low-side MOSFET rectifier and turning on the high-side MOSFET switch.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Undervoltage Lockout

The undervoltage lockout circuit prevents the device from malfunctioning at low input voltages and from excessive discharge of the battery and disables the output stage of the converter. The undervoltage lockout threshold is typically 1.85 V with falling V_{IN}.

8.3.2 Enable

The device is enabled by setting the EN pin to high. During the start-up time ($t_{Start\ up}$), the internal circuits are settled and the soft-start circuit is activated. The EN input can be used to control power sequencing in a system with various DC-DC converters. The EN pin can be connected to the output of another converter, to drive the EN pin high and sequence supply rails. With EN pin = GND, the device enters shutdown mode in which all circuits are disabled. In fixed-output voltage versions, the internal resistor divider network is then disconnected from FB pin.

8.3.3 Thermal Shutdown

As soon as the junction temperature, T_J, exceeds 140°C (typical) the device goes into thermal shutdown. In this mode, the high-side and low-side MOSFETs are turned off. The device continues its operation when the junction temperature falls below the thermal shutdown hysteresis.

8.4 Device Functional Modes

8.4.1 Soft Start

The TPS6224X-Q1 device has an internal soft-start circuit that controls the ramp up of the output voltage. The output voltage ramps up from 5% to 95% of its nominal value within typical 250 µs. This limits the inrush current in the converter during ramp up and prevents possible input voltage drops when using a battery or high impedance power source. The soft-start circuit is enabled within the start-up time, $t_{Start\ up}$.

8.4.2 Power Save Mode

The power save mode is enabled. If the load current decreases, the converter enters power save mode operation automatically. During power save mode, the converter skips switching and operates with reduced frequency in PFM mode with a minimum-quiescent current to maintain high efficiency.

The transition from PWM mode to PFM mode occurs once the inductor current in the low-side MOSFET switch becomes zero, which indicates discontinuous conduction mode.

During the power save mode, a PFM comparator monitors the output voltage. As the output voltage falls below the PFM comparator threshold of V_{OUT} nominal, the device starts a PFM current pulse. The high-side MOSFET switch turns on, and the inductor current ramps up. After the on-time expires, the switch turns off and the low-side MOSFET switch turns on until the inductor current becomes zero.

The converter effectively delivers a current to the output capacitor and the load. If the load is below the delivered current, the output voltage rises. If the output voltage is equal to or greater than the PFM comparator threshold, the device stops switching and enters a sleep mode with typical 15-µA current consumption.

If the output voltage is still below the PFM comparator threshold, a sequence of further PFM current pulses are generated until the PFM comparator threshold is reached. The converter starts switching again once the output voltage drops below the PFM comparator threshold.

With a fast single-threshold comparator, the output-voltage ripple during PFM mode operation can be kept to a minimum. The PFM pulse is time controlled, allowing the user to modify the charge transferred to the output capacitor by the value of the inductor. The resulting PFM output voltage ripple and PFM frequency both depend on the size of the output capacitor and the inductor value. Increasing output capacitor values and inductor values minimize the output ripple. The PFM frequency decreases with smaller inductor values and increases with larger values.

If the output current cannot be supported in PFM mode, the device exits PFM mode and enters PWM mode.

Device Functional Modes (continued)

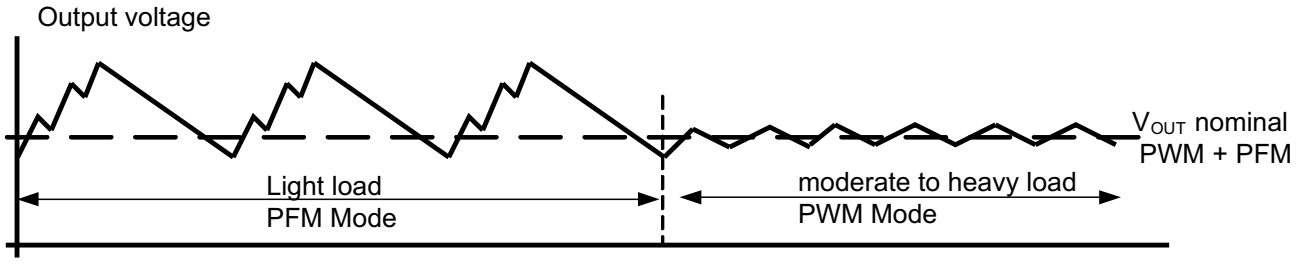


Figure 5. Power Save Mode

8.4.2.1 100% Duty Cycle Low Dropout Operation

The device starts to enter 100% duty-cycle mode once the input voltage comes close to the nominal output voltage. To maintain the output voltage, the high-side MOSFET switch is turned on 100% for one or more cycles.

With further decreasing V_{IN} the high-side MOSFET switch is turned on completely. In this case, the converter offers a low input-to-output voltage difference. This is particularly useful in battery-powered applications to achieve longest operation time by taking full advantage of the entire battery voltage range.

The minimum input voltage to maintain regulation depends on the load current and output voltage, and can be calculated as:

$$V_{IN}min = V_O max + I_O max\ (R_{DS(on)} max + R_L) \quad (1)$$

where

- $I_O$max = maximum output current plus inductor ripple current
- $R_{DS(on)}$max = maximum P-channel switch $R_{DS(on)}$
- R_L = DC resistance of the inductor
- $V_O$max = nominal output voltage plus maximum output voltage tolerance

8.4.3 Short-Circuit Protection

The high-side and low-side MOSFET switches are short-circuit protected with maximum switch current equal to I_{LIMF}. The current in the switches is monitored by current limit comparators. Once the current in the high-side MOSFET switch exceeds the threshold of its current limit comparator, it turns off and the low-side MOSFET switch is activated to ramp down the current in the inductor and high-side MOSFET switch. The high-side MOSFET switch can only turn on again once the current in the low-side MOSFET switch has decreased below the threshold of its current limit comparator.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The following section discusses the design of the external components to complete the power supply design by using typical applications as a reference.

9.2 Typical Application

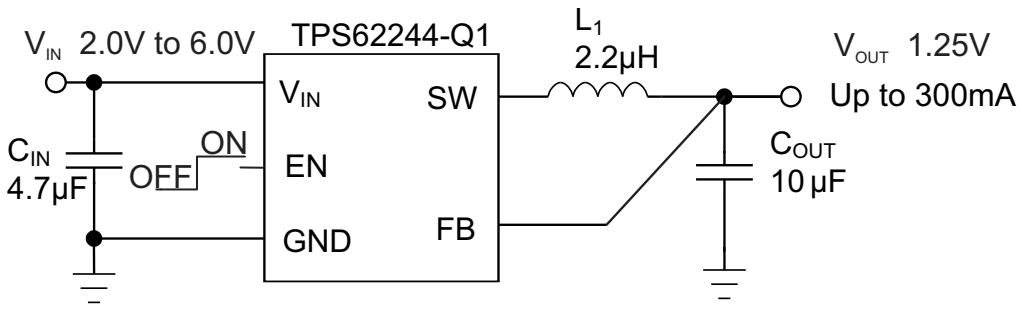


Figure 6. TPS62244Q1, Fixed 1.25 V V_{OUT}

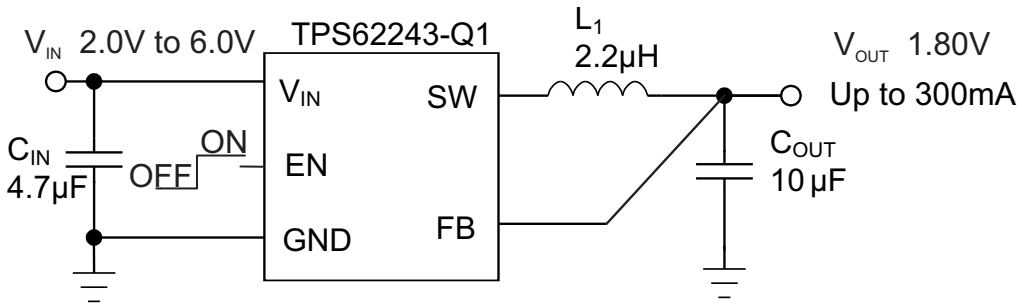


Figure 7. TPS62243Q1, Fixed 1.80 V V_{OUT}

9.2.1 Design Requirements

The device operates over an input voltage range from 2 V to 6 V. The output voltage setting is fixed.

9.2.2 Detailed Design Procedure

Table 2 shows the list of components for the *Application Curves*. Users must verify and validate these components for suitability with their application before using the components.

Table 2. List of Components

VALUE	COMPONENT REFERENCE	PART NUMBER	MANUFACTURER(1)
4.7 µF, 6.3 V. X5R Ceramic	C_{IN}	GRM188R60J475K	Murata
10 µF, 6.3 V. X5R Ceramic	C_{OUT}	GRM188R60J106M	Murata
2.2 µH, 110 mΩ	L_1	LPS3015	Coilcraft

(1) See *Third-party Products Disclaimer*

9.2.2.1 Output Filter Design (Inductor and Output Capacitor)

The TPS6224X-Q1 device is designed to operate with inductors in the range of 1.5 µH to 4.7 µH and with output capacitors in the range of 4.7 µF to 22 µF. The device is optimized for operation with a 2.2-µH inductor and 10-µF output capacitor.

Larger or smaller inductor values can be used to optimize the performance of the device for specific operation conditions. For stable operation, the L and C values of the output filter may not fall below 1-µH effective Inductance and 3.5-µF effective capacitance.

9.2.2.1.1 Inductor Selection

The inductor value has a direct effect on the ripple current. The selected inductor must be rated for its DC resistance and saturation current (Table 3). The inductor ripple current (ΔI_L) decreases with higher inductance and increases with higher V_I or V_O.

The inductor selection also has an impact on the output voltage ripple in the PFM mode. Higher inductor values lead to lower-output voltage ripple and higher PFM frequency, and lower inductor values lead to a higher-output voltage ripple with lower PFM frequency.

Equation 2 calculates the maximum inductor current in PWM mode under static load conditions. The saturation current of the inductor should be rated higher than the maximum inductor current as calculated with Equation 3. This is the recommendation because during heavy-load transients the inductor current rises above the calculated value.

$$\Delta I_L = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f} \tag{2}$$

$$I_{Lmax} = I_{OUTmax} + \frac{\Delta I_L}{2} \tag{3}$$

where

- f = Switching frequency (2.25-MHz typical)
- L = Inductor value
- ΔI_L = Peak-to-Peak inductor ripple current
- I_{Lmax} = Maximum inductor current

A more conservative approach is to select the inductor current rating just for the maximum switch current limit I_{LIMF} of the converter.

Accepting larger values of ripple current allows the use of low inductance values, but results in higher output voltage ripple, greater core losses, and lower output current capability.

The total losses of the coil strongly impact the efficiency of the DC-DC conversion and consist of both the losses in the DC resistance ($R_{(DC)}$) and the following frequency-dependent components:

- The losses in the core material (magnetic hysteresis loss, especially at high switching frequencies)
- Additional losses in the conductor from the skin effect (current displacement at high frequencies)
- Magnetic field losses of the neighboring windings (proximity effect)
- Radiation losses

Table 3. List of Inductors

INDUCTANCE (µH)	DIMENSIONS (mm)	PART NUMBER	MANUFACTURER(1)
2	2.5 × 2 × 1	MIPS2520D2R2	FDK
2	2.5 × 2 × 1.2	MIPSA2520D2R2	FDK
2.2	2.5 × 2 × 1	KSLI-252010AG2R2	Hitachi Metals
2.2	2.5 × 2 × 1.2	LQM2HPN2R2MJ0L	Murata
2.2	3 × 3 × 1.4	LPS3015	Coilcraft

(1) See *Third-party Products Disclaimer*

9.2.2.1.2 Output Capacitor Selection

The advanced fast-response voltage-mode control scheme of the TPS6224X-Q1 device allows the use of tiny ceramic capacitors. Ceramic capacitors with low-ESR values have the lowest-output voltage ripple and are recommended. The output capacitor requires either an X7R or X5R dielectric. Y5V and Z5U dielectric capacitors, aside from their wide variation in capacitance over temperature, become resistive at high frequencies.

At nominal load current, the device operates in PWM mode and the RMS ripple current is calculated as in Equation 4:

$$I_{RMSC_{OUT}} = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f} \times \frac{1}{2 \times \sqrt{3}} \quad (4)$$

At nominal load current, the device operates in PWM mode and the overall output voltage ripple is the sum of the voltage spike caused by the output capacitor ESR plus the voltage ripple caused by charging and discharging the output capacitor as in Equation 5:

$$\Delta V_{OUT} = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f} \times \left(\frac{1}{8 \times C_{OUT} \times f} + ESR \right) \quad (5)$$

At light load currents, the converter operates in power save mode and the output voltage ripple depends on the output capacitor and inductor value. Larger output capacitor and inductor values minimize the voltage ripple in PFM mode and tighten DC output accuracy in PFM mode.

9.2.2.1.3 Input Capacitor Selection

The buck converter has a natural pulsating input current; therefore, a low-ESR input capacitor is required for best input voltage filtering and minimizing the interference with other circuits caused by high-input voltage spikes. For most applications, a 4.7-µF to 10-µF ceramic capacitor is recommended (Table 4). Because ceramic capacitors lose up to 80% of their initial capacitance at 5 V, TI recommends using a 10-µF input capacitor for input voltages greater than 4.5 V. The input capacitor can be increased without any limit for better input voltage filtering.

Take care when using only small ceramic input capacitors. When a ceramic capacitor is used at the input, and the power is being supplied through long wires, such as from a wall adapter, a load step at the output, or V_{IN} step on the input, can induce ringing at the VIN pin. The ringing can couple to the output and be mistaken as loop instability, or could even damage the part by exceeding the maximum ratings.

Table 4. List of Capacitors

CAPACITANCE (µF)	DIMENSIONS (mm)	PART NUMBER	MANUFACTURER(1)
4.7	0603: 1.6 × 0.8 × 0.8	GRM188R60J475K	Murata
10	0603: 1.6 × 0.8 × 0.8	GRM188R60J106M69D	Murata

(1) See *Third-party Products Disclaimer*

9.2.3 Application Curves

The conditions for below application curves are VIN = 3.0V, VOUT= 1.25V and the components listed in Table 2, unless otherwise noted.

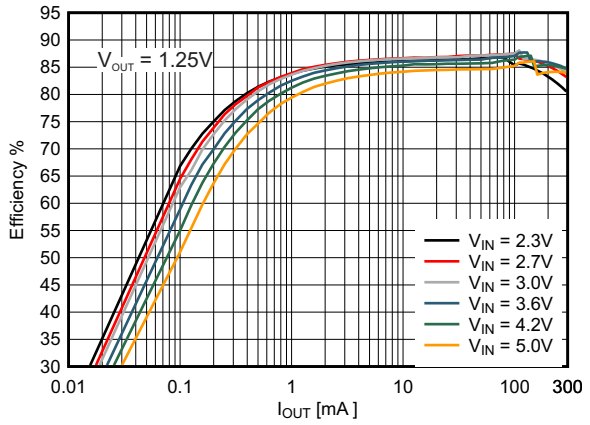


Figure 8. Efficiency vs Output Current, V_{OUT} = 1.25V

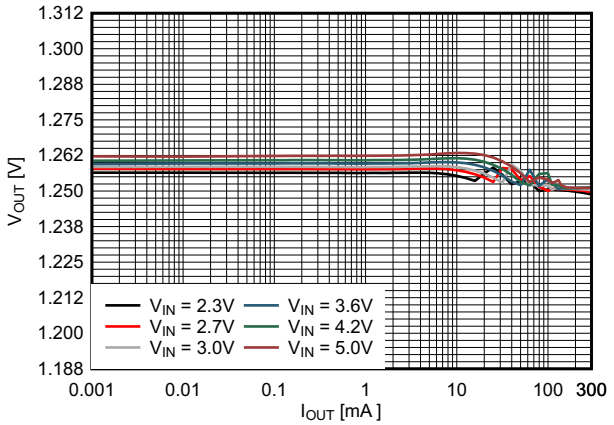


Figure 9. Output Voltage vs Output Current 1.25V V_{OUT}

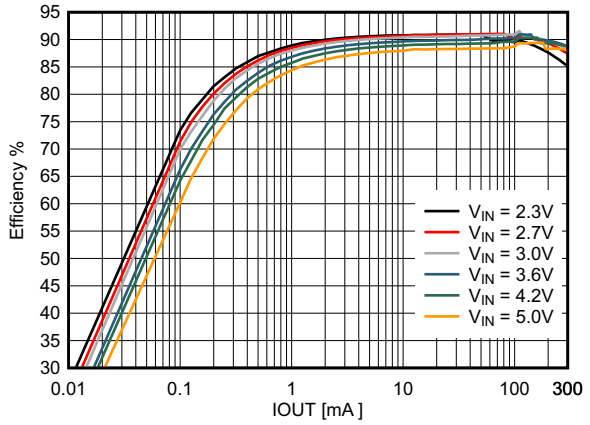


Figure 10. Efficiency vs Output Current, V_{OUT} = 1.8V

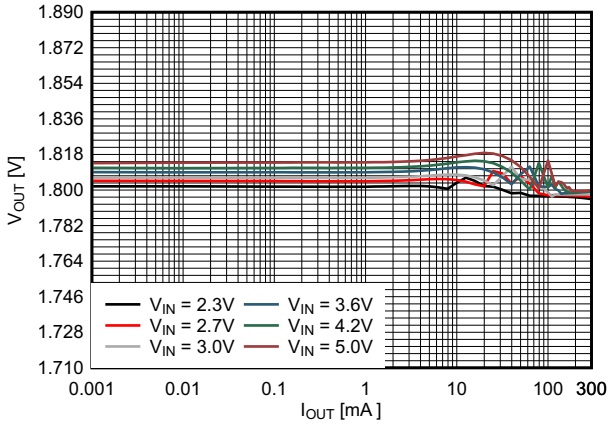
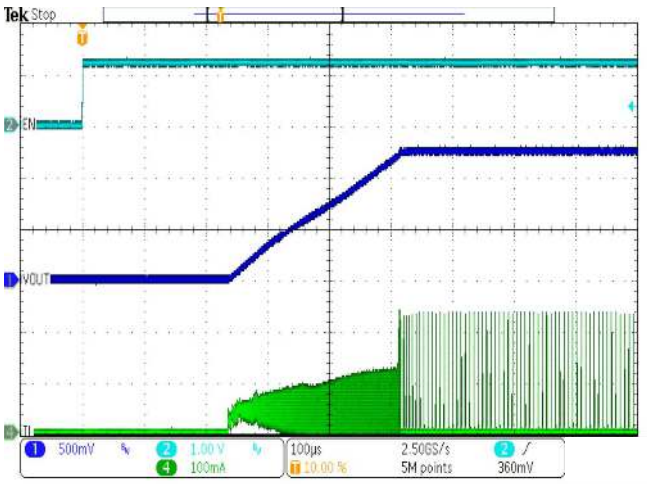
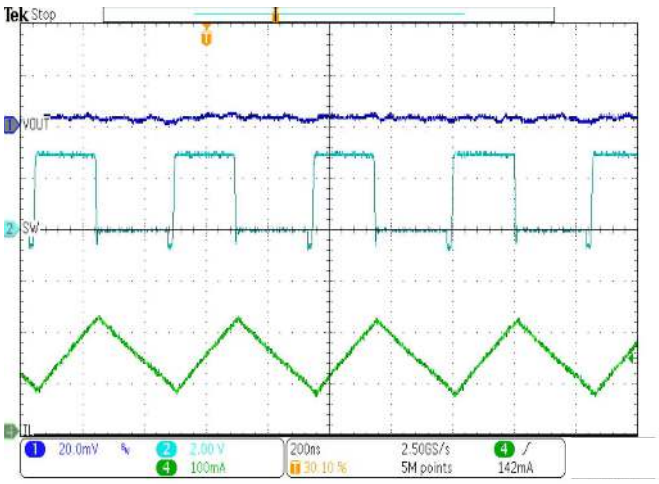


Figure 11. Output Voltage vs Output Current, V_{OUT} = 1.8V



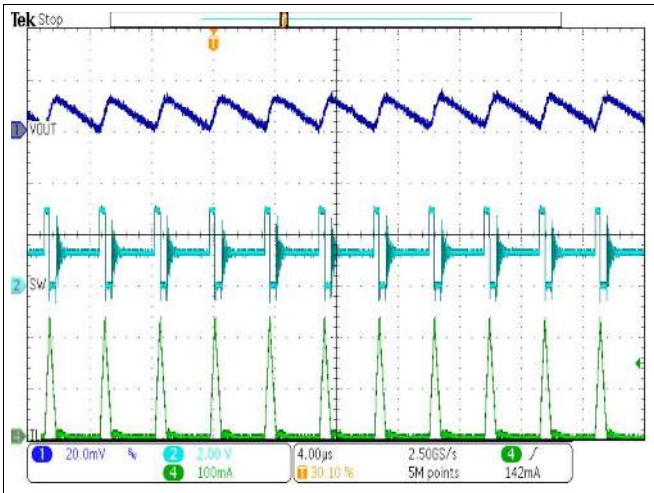
V_{IN} = 3V R_{Load} = 100Ω V_{OUT} = 1.25V

Figure 12. Start-Up Timing



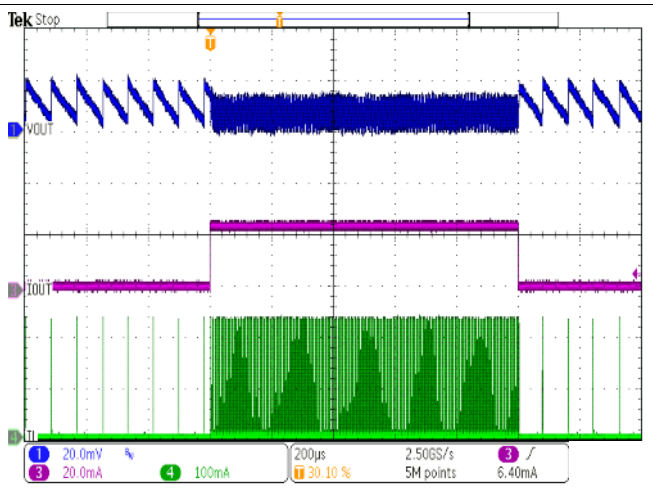
V_{IN} = 3V I_{OUT} = 150mA V_{OUT} = 1.25V

Figure 13. Typical PWM Mode Operation



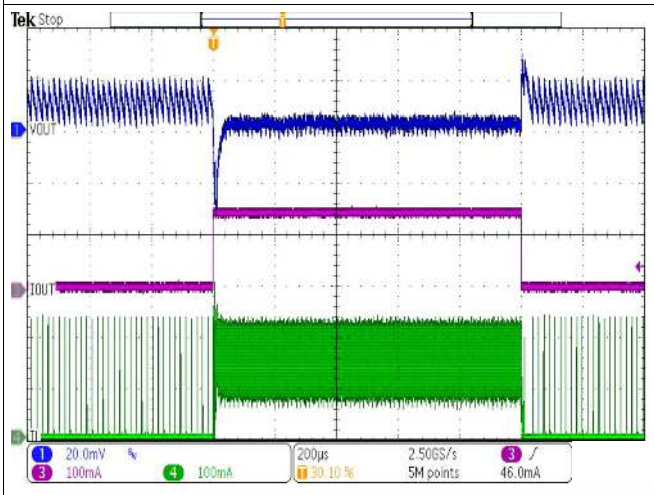
V_{IN} = 3V I_{OUT} = 25mA V_{OUT} = 1.25V

Figure 14. Typical PFM Mode Operation



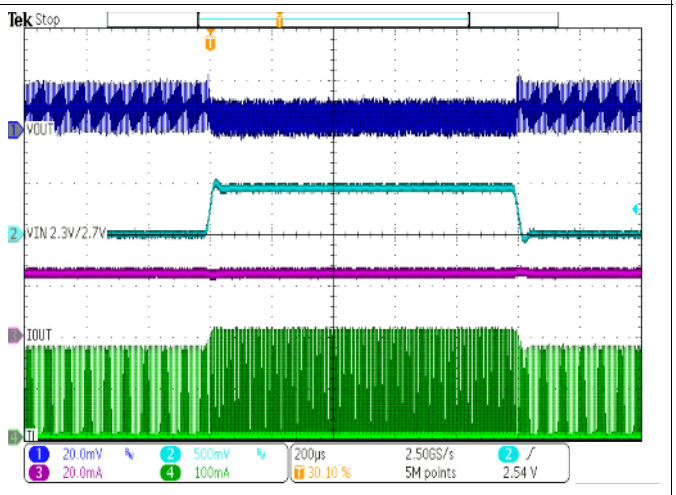
V_{IN} = 3V I_{OUT} = 1mA to 25mA to 1mA V_{OUT} = 1.25V
Rise / Fall Time 1µs

Figure 15. Load Transient PFM Mode



V_{IN} = 3V I_{OUT} = 5mA to 150mA to 5mA V_{OUT} = 1.25V
Rise / Fall Time 1µs

Figure 16. Load Transient PFM / PWM Mode



V_{IN} = 2.3V to 2.7V to 2.3V I_{OUT} = 25mA V_{OUT} = 1.25V
Rise / Fall Time 10µs

Figure 17. Line Transient PFM Mode

10 Power Supply Recommendations

The TPS6224X-Q1 device has no special requirements for its input power supply. The input power supply output current must be rated according to the supply voltage, output voltage, and output current of the TPS6224X-Q1.

11 Layout

11.1 Layout Guidelines

As for all switching power supplies, the layout is an important step in the design. Proper function of the device demands careful attention to PCB layout. To get the specified performance, the board layout must be carefully done. If not carefully done, the regulator could show poor line or load regulation, and additional stability issues as well as EMI problems. Figure 18 shows an example of layout design with the TLV62242-Q1 device.

- Providing a low-inductance, low-impedance ground path is critical. Therefore, use wide and short traces for the main current paths. The input capacitor as well as the inductor and output capacitor must be placed as close as possible to the IC pins.
- The FB line must be connected directly to the output capacitor and the FB line must be routed away from noisy components and traces (for example, the SW line).
- Because of the small package of this converter and the overall small solution size, the thermal performance of the PCB layout is important. For good thermal performance, PCB design of at least four layers is recommended.

11.2 Layout Example

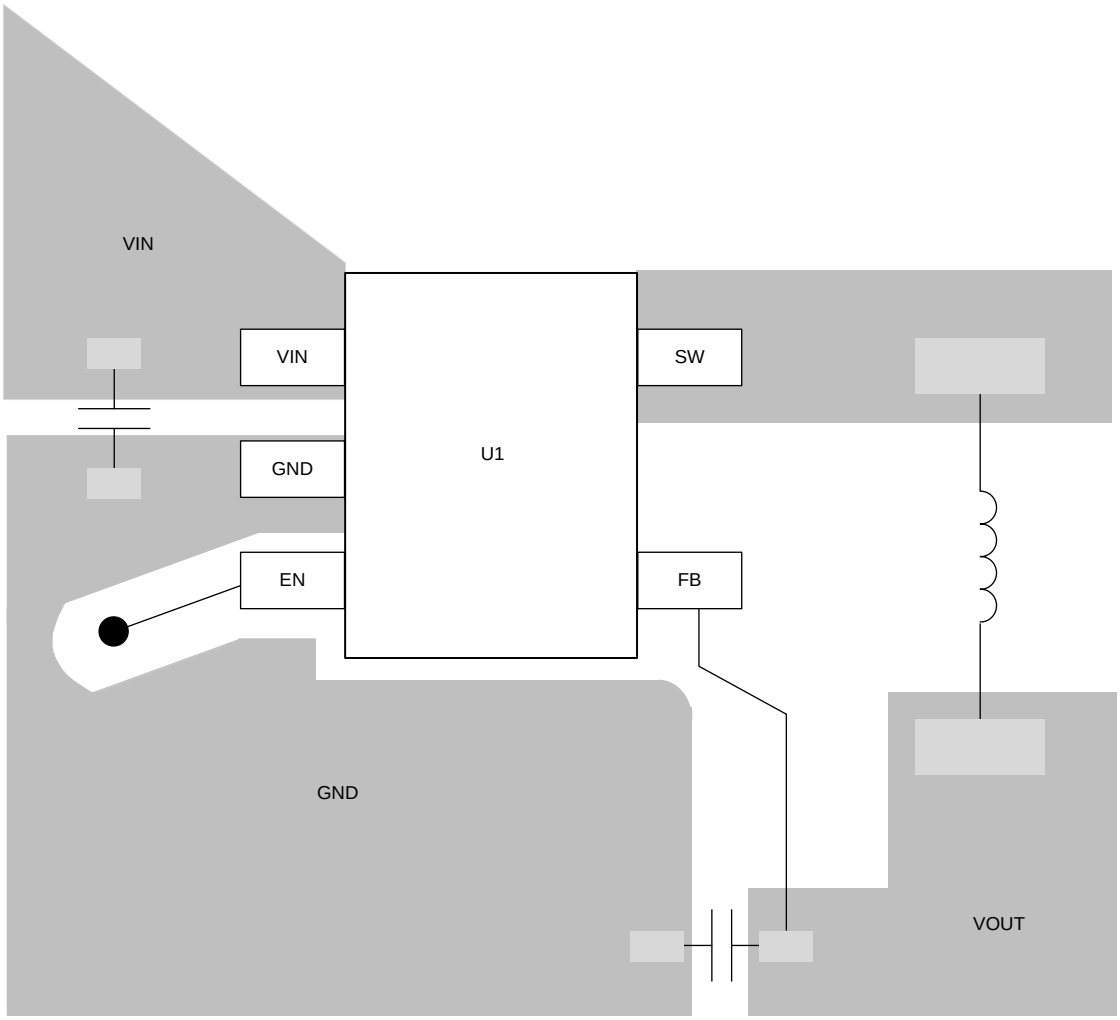


Figure 18. Suggested Layout for Fixed Output Voltage

12 Device and Documentation Support

12.1 Third-Party Products Disclaimer

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12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.

12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

13.1 Package Option Addendum

13.1.1 Packaging Information

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (3)	MSL Peak Temp (4)	Op Temp (°C)	Device Marking (5)(6)
TPS62243QDDCRQ1	PREVIEW	SOT-23-THIN	DDC	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	–40 to 115	1I3Z
TPS62244QDDCRQ1	PREVIEW	SOT-23-THIN	DDC	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	–40 to 115	1I2Z

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

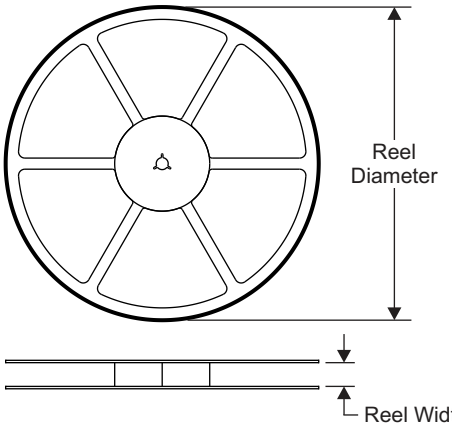
(4) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(5) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device

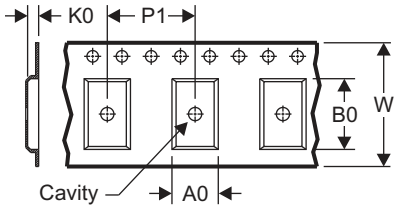
(6) Multiple Device markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

13.1.2 Tape and Reel Information

REEL DIMENSIONS

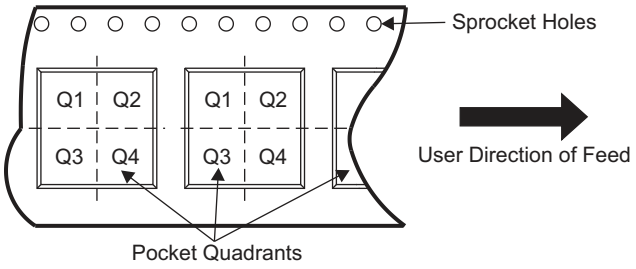


TAPE DIMENSIONS



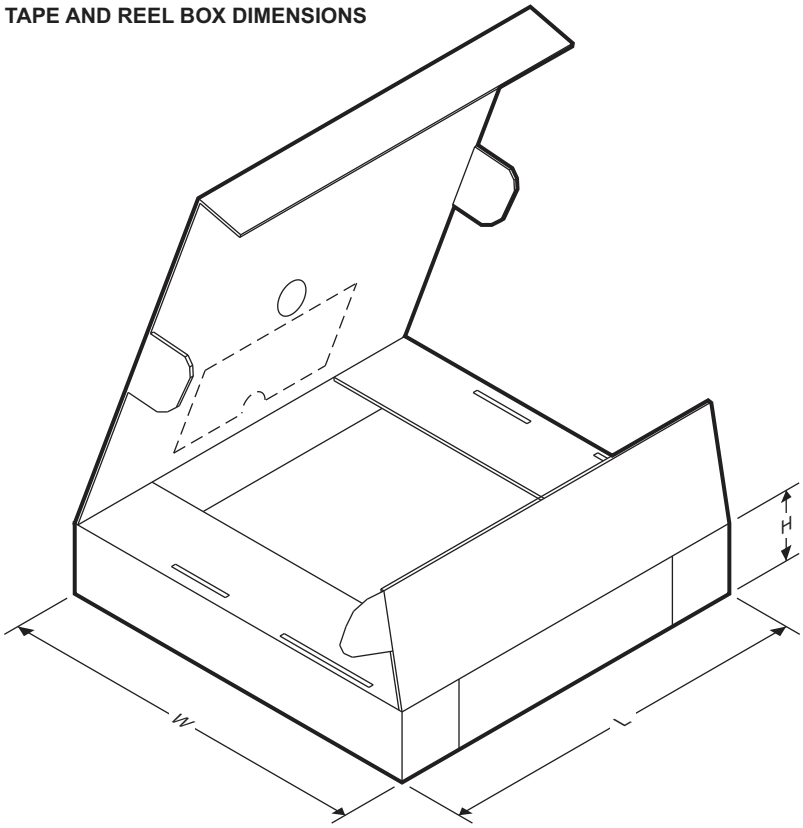
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS62243QDDCRQ1	SOT-23-THIN	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS62244QDDCRQ1	SOT-23-THIN	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS62243QDDCRQ1	SOT-23-THIN	DDC	5	3000	203.0	2.3.0	35.0
TPS62244QDDCRQ1	SOT-23-THIN	DDC	5	3000	203.0	2.3.0	35.0

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS62243QDDCRQ1	ACTIVE	SOT-23-THIN	DDC	5	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1I3Z	Samples
TPS62244QDDCRQ1	ACTIVE	SOT-23-THIN	DDC	5	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1I2Z	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

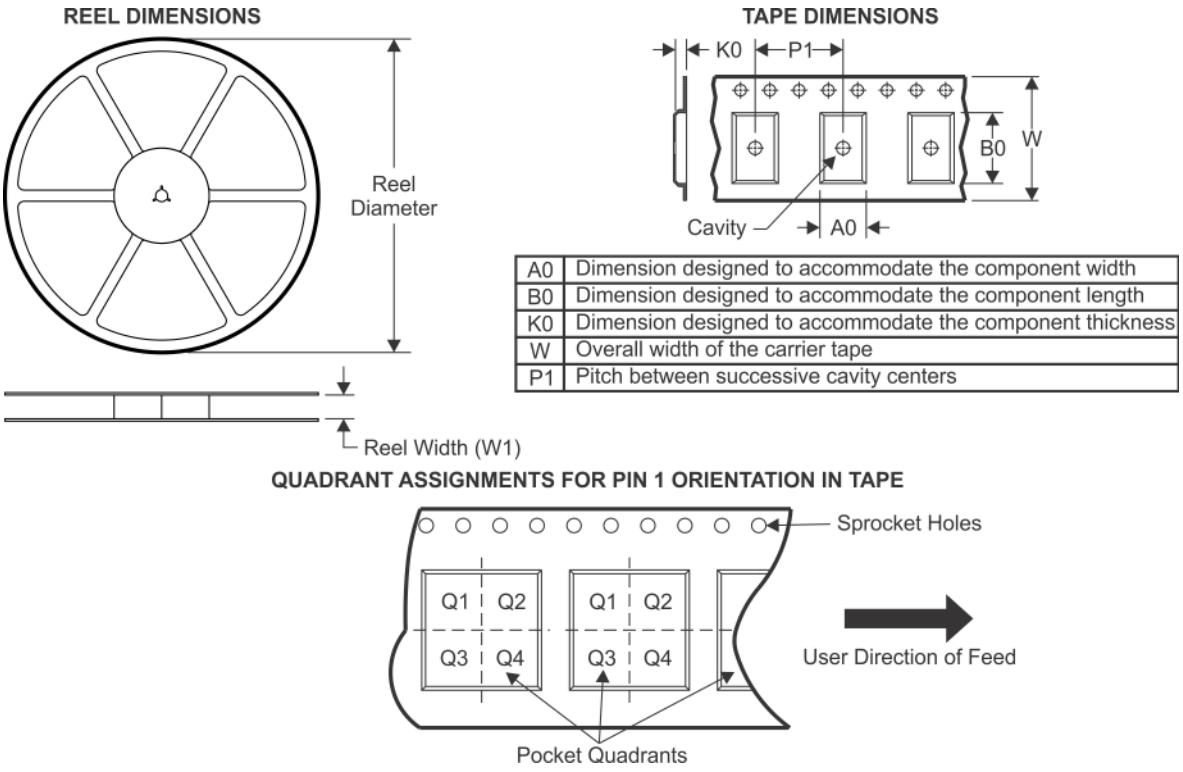
OTHER QUALIFIED VERSIONS OF TPS62243-Q1 :

- Catalog: TPS62243

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

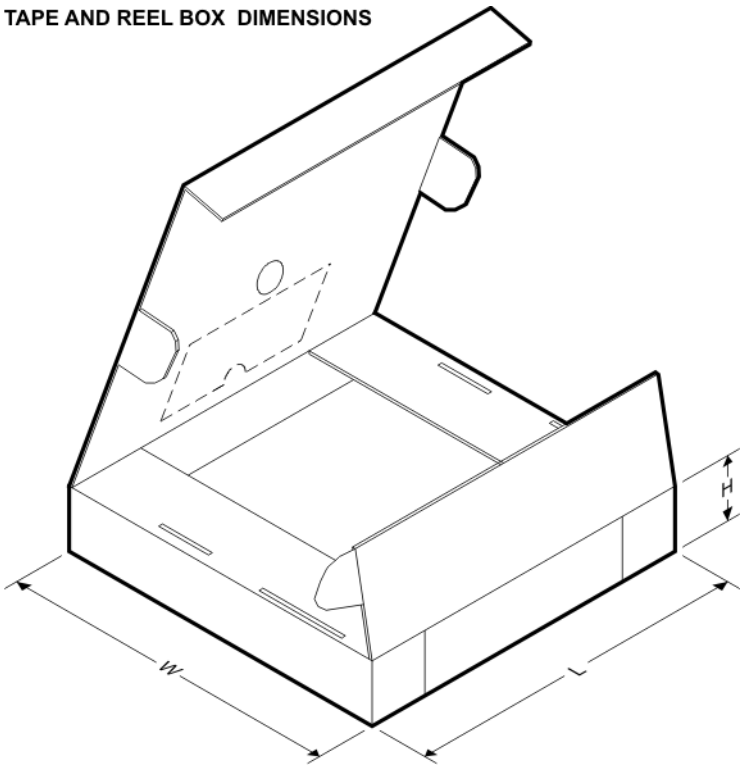


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS62243QDDCRQ1	SOT-23-THIN	DDC	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS62244QDDCRQ1	SOT-23-THIN	DDC	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

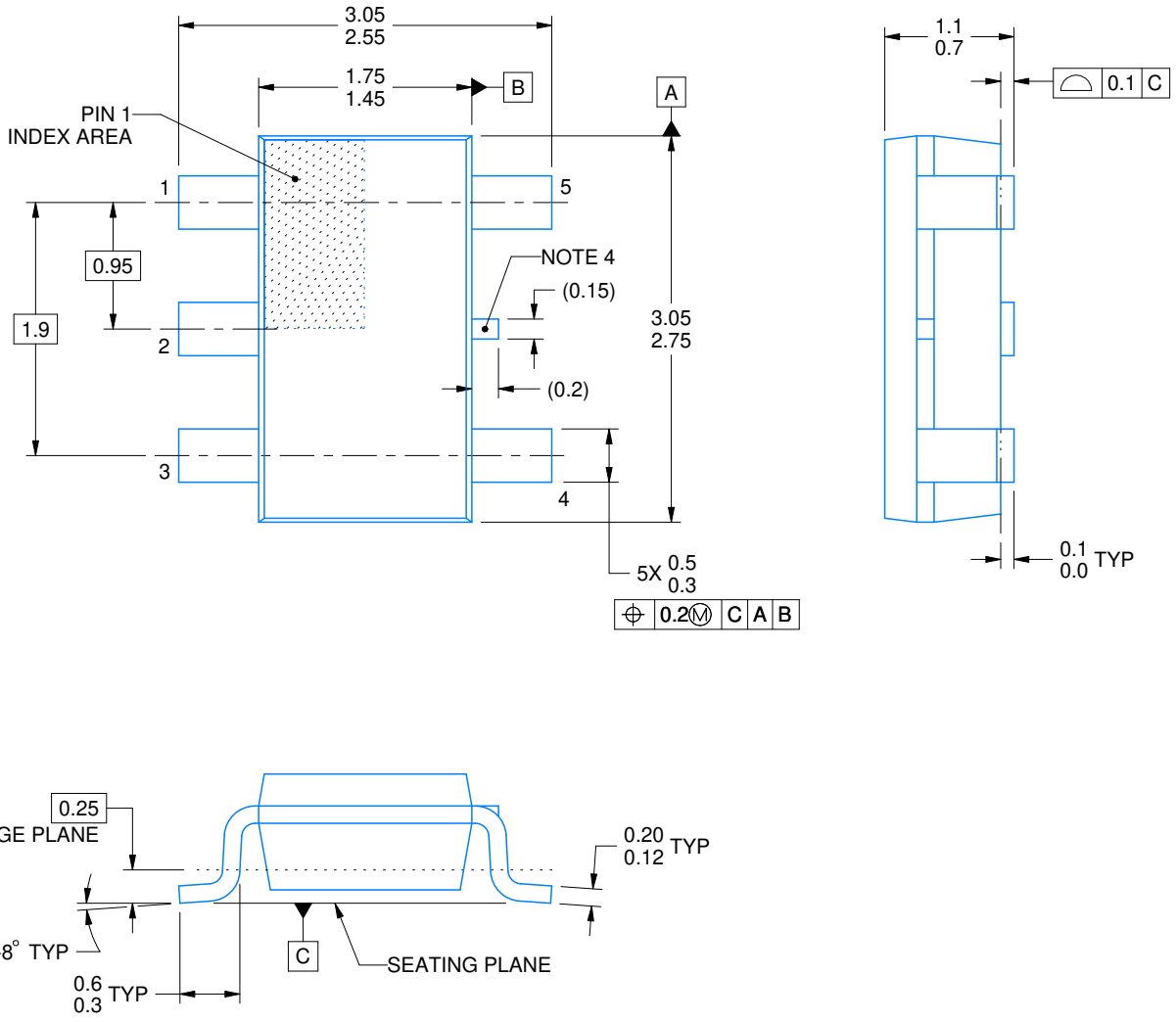
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS62243QDDCRQ1	SOT-23-THIN	DDC	5	3000	213.0	191.0	35.0
TPS62244QDDCRQ1	SOT-23-THIN	DDC	5	3000	213.0	191.0	35.0

DDC0005A

PACKAGE OUTLINE

SOT-23 - 1.1 max height

SMALL OUTLINE TRANSISTOR



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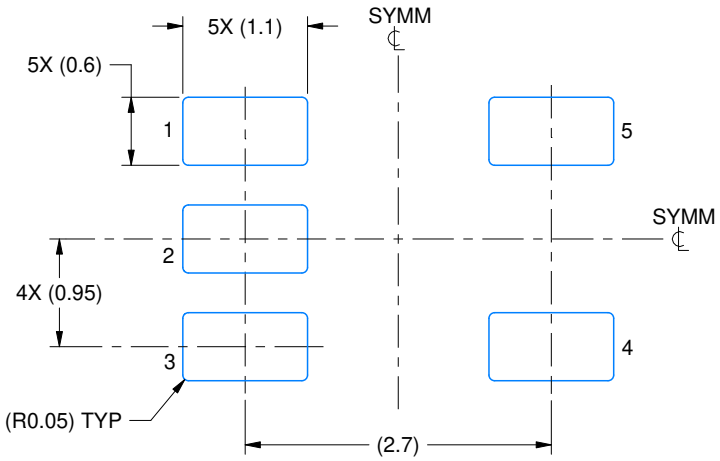
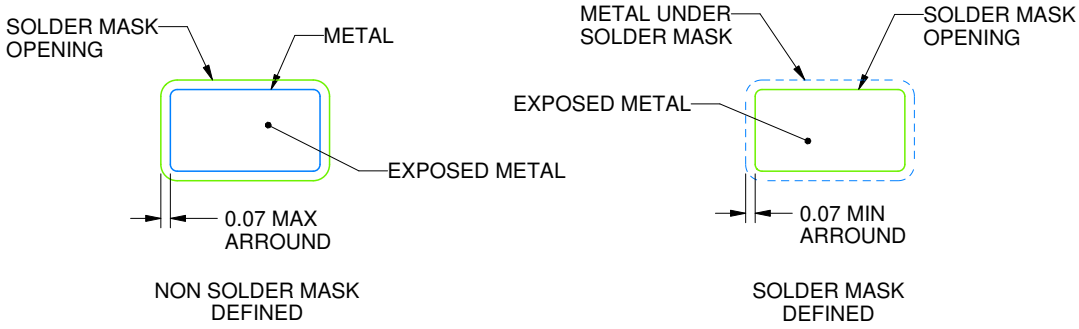
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-193.
4. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPLOSED METAL SHOWN
SCALE:15X



SOLDERMASK DETAILS

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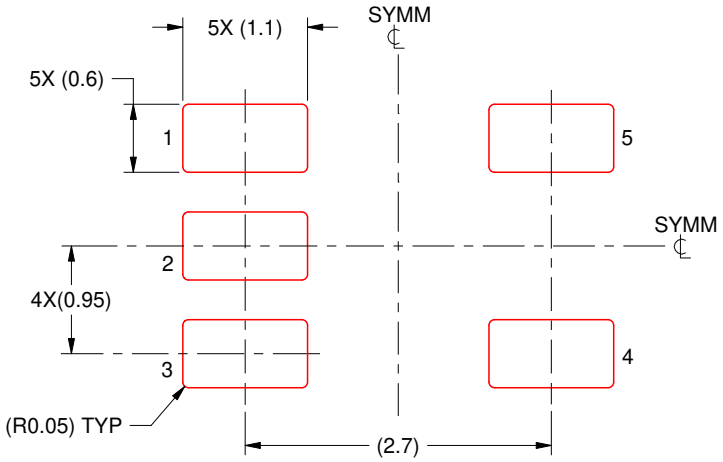
NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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