

National Semiconductor is now part of
Texas Instruments.

Search <http://www.ti.com/> for the latest technical
information and details on our current products and services.

LMC6041

CMOS Single Micropower Operational Amplifier

General Description

Ultra-low power consumption and low input-leakage current are the hallmarks of the LMC6041. Providing input currents of only 2 fA typical, the LMC6041 can operate from a single supply, has output swing extending to each supply rail, and an input voltage range that includes ground.

The LMC6041 is ideal for use in systems requiring ultra-low power consumption. In addition, the insensitivity to latch-up, high output drive, and output swing to ground without requiring external pull-down resistors make it ideal for single-supply battery-powered systems.

Other applications for the LMC6041 include bar code reader amplifiers, magnetic and electric field detectors, and hand-held electrometers.

This device is built with National's advanced Double-Poly Silicon-Gate CMOS process.

See the LMC6042 for a dual, and the LMC6044 for a quad amplifier with these features.

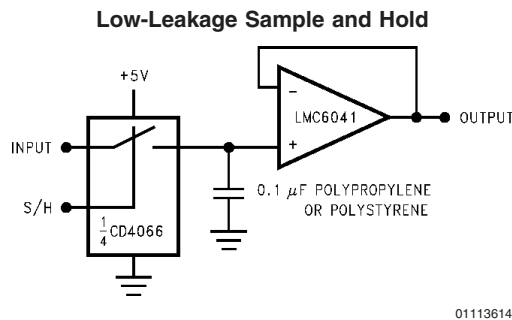
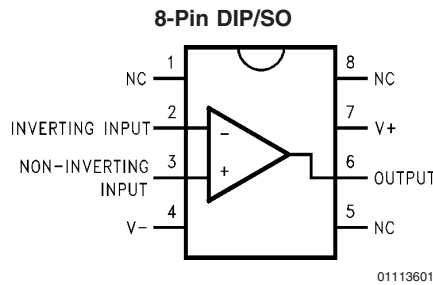
Features

- Low supply current: 14 μ A (Typ)
- Operates from 4.5V to 15.5V single supply
- Ultra low input current: 2 fA (Typ)
- Rail-to-rail output swing
- Input common-mode range includes ground

Applications

- Battery monitoring and power conditioning
- Photodiode and infrared detector preamplifier
- Silicon based transducer systems
- Hand-held analytic instruments
- pH probe buffer amplifier
- Fire and smoke detection systems
- Charge amplifier for piezoelectric transducers

Connection Diagram



Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Differential Input Voltage	±Supply Voltage
Supply Voltage (V ⁺ – V ⁻)	16V
Output Short Circuit to V ⁻	(Note 2)
Output Short Circuit to V ⁺	(Note 11)
Lead Temperature (Soldering, 10 sec.)	260°C
Storage Temperature Range	-65°C to +150°C
Junction Temperature	110°C
ESD Tolerance (Note 4)	500V
Current at Input Pin	±5 mA
Current at Output Pin	±18 mA

Current at Power Supply Pin	35 mA
Voltage at Input/Output Pin	(V ⁺) + 0.3V, (V ⁻) – 0.3V
Power Dissipation	(Note 3)

Operating Ratings

Temperature Range LMC6041AI, LMC6041I	-40°C ≤ T _J ≤ +85°C
Supply Voltage	4.5V ≤ V ⁺ ≤ 15.5V
Power Dissipation	(Note 9)
Thermal Resistance (θ _{JA}) (Note 10)	
8-Pin DIP	101°C/W
8-Pin SO	165°C/W

Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_A = T_J = 25°C. **Boldface** limits apply at the temperature extremes. V⁺ = 5V, V⁻ = 0V, V_{CM} = 1.5V, V_O = V⁺/2, and R_L > 1M unless otherwise specified.

Symbol	Parameter	Conditions	Typical (Note 5)	LMC6041AI	LMC6041I	Units (Limit)	
				Limit (Note 6)	Limit (Note 6)		
V _{OS}	Input Offset Voltage		1	3 3.3	6 6.3	mV max	
TCV _{OS}	Input Offset Voltage Average Drift		1.3			µV/°C	
I _B	Input Bias Current		0.002	4	4	pA max	
I _{OS}	Input Offset Current		0.001	2	2	pA max	
R _{IN}	Input Resistance		> 10			TeraΩ	
CMRR	Common Mode Rejection Ratio	0V ≤ V _{CM} ≤ 12.0V V ⁺ = 15V	75	68 66	62 60	dB min	
+PSRR	Positive Power Supply Rejection Ratio	5V ≤ V ⁺ ≤ 15V V _O = 2.5V	75	68 66	62 60	dB min	
-PSRR	Negative Power Supply Rejection Ratio	0V ≤ V ⁻ ≤ -10V V _O = 2.5V	94	84 83	74 73	dB min	
CMR	Input Common-Mode Voltage Range	V ⁺ = 5V and 15V for CMRR ≥ 50 dB	-0.4	-0.1 0	-0.1 0	V max	
			V ⁺ – 1.9V	V ⁺ – 2.3V V⁺ – 2.5V	V ⁺ – 2.3V V⁺ – 2.4V	V min	
A _V	Large Signal Voltage Gain	R _L = 100 kΩ (Note 7)	Sourcing	1000	400 300	300 200	V/mV min
			Sinking	500	180 120	90 70	V/mV min
		R _L = 25 kΩ (Note 7)	Sourcing	1000	200 160	100 80	V/mV min
			Sinking	250	100 60	50 40	V/mV min

Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for $T_A = T_J = 25^\circ\text{C}$. **Boldface** limits apply at the temperature extremes. $V^+ = 5\text{V}$, $V^- = 0\text{V}$, $V_{\text{CM}} = 1.5\text{V}$, $V_O = V^+/2$, and $R_L > 1\text{M}$ unless otherwise specified.

Symbol	Parameter	Conditions	Typical (Note 5)	LMC6041AI	LMC6041I	Units (Limit)		
				Limit (Note 6)	Limit (Note 6)			
V_O	Output Swing	$V^+ = 5\text{V}$ $R_L = 100\text{ k}\Omega$ to $V^+/2$	4.987	4.970 4.950	4.940 4.910	V min		
			0.004	0.030 0.050	0.060 0.090	V max		
		$V^+ = 5\text{V}$ $R_L = 25\text{ k}\Omega$ to $V^+/2$	4.980	4.920 4.870	4.870 4.820	V min		
			0.010	0.080 0.130	0.130 0.180	V max		
		$V^+ = 15\text{V}$ $R_L = 100\text{ k}\Omega$ to $V^+/2$	14.970	14.920 14.880	14.880 14.820	V min		
			0.007	0.030 0.050	0.060 0.090	V max		
		$V^+ = 15\text{V}$ $R_L = 25\text{ k}\Omega$ to $V^+/2$	14.950	14.900 14.850	14.850 14.800	V min		
			0.022	0.100 0.150	0.150 0.200	V max		
		I_{SC}	Output Current $V^+ = 5\text{V}$	Sourcing, $V_O = 0\text{V}$	22	16 10	13 8	mA min
				Sinking, $V_O = 5\text{V}$	21	16 8	13 8	mA min
		I_{SC}	Output Current $V^+ = 15\text{V}$	Sourcing, $V_O = 0\text{V}$	40	15 10	15 10	mA min
				Sinking, $V_O = 13\text{V}$ (Note 11)	39	24 8	21 8	mA min
I_S	Supply Current	$V_O = 1.5\text{V}$	14	20 24	26 30	μA max		
		$V^+ = 15\text{V}$	18	26 31	34 39	μA max		

AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_A = T_J = 25^\circ\text{C}$. **Boldface** limits apply at the temperature extremes. $V^+ = 5\text{V}$, $V^- = 0\text{V}$, $V_{\text{CM}} = 1.5\text{V}$, $V_O = V^+/2$, and $R_L > 1\text{M}$ unless otherwise specified.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC6041AI	LMC6041I	Units (Limit)
				Limit (Note 6)	Limit (Note 6)	
SR	Slew Rate	(Note 8)	0.02	0.015 0.010	0.010 0.007	V/ μs min
GBW	Gain-Bandwidth Product		75			kHz
ϕ_m	Phase Margin		60			Deg
e_n	Input-Referred Voltage Noise	$F = 1\text{ kHz}$	83			nV/ $\sqrt{\text{Hz}}$
i_n	Input-Referred Current Noise	$F = 1\text{ kHz}$	0.0002			pA/ $\sqrt{\text{Hz}}$
T.H.D.	Total Harmonic Distortion	$F = 1\text{ kHz}$, $A_V = -5$ $R_L = 100\text{ k}\Omega$, $V_O = 2\text{ V}_{\text{pp}}$ $\pm 5\text{V}$ Supply	0.01			%

AC Electrical Characteristics (Continued)

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating conditions indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

Note 2: Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 110°C. Output currents in excess of ±30 mA over long term may adversely affect reliability.

Note 3: The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA} , and T_A . The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)} - T_A)/\theta_{JA}$.

Note 4: Human body model, 1.5 kΩ in series with 100 pF.

Note 5: Typical Values represent the most likely parametric norm.

Note 6: All limits are guaranteed at room temperature (standard type face) or at operating temperature extremes (bold face type).

Note 7: $V^+ = 15V$, $V_{CM} = 7.5V$ and R_L connected to 7.5V. For Sourcing tests, $7.5V \leq V_O \leq 11.5V$. For Sinking tests, $2.5V \leq V_O \leq 7.5V$.

Note 8: $V^+ = 15V$. Connected as Voltage Follower with 10V step input. Number specified in the slower of the positive and negative slew rates.

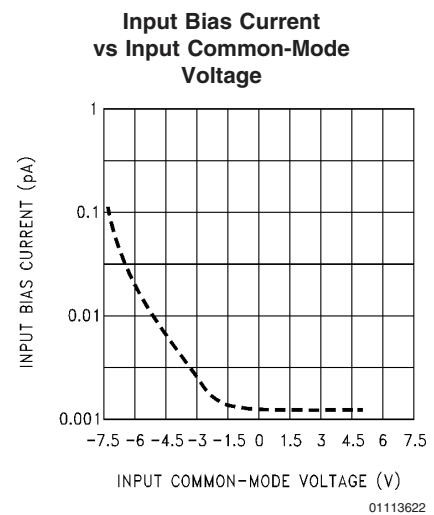
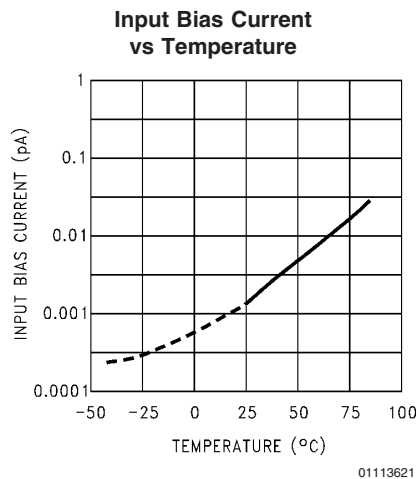
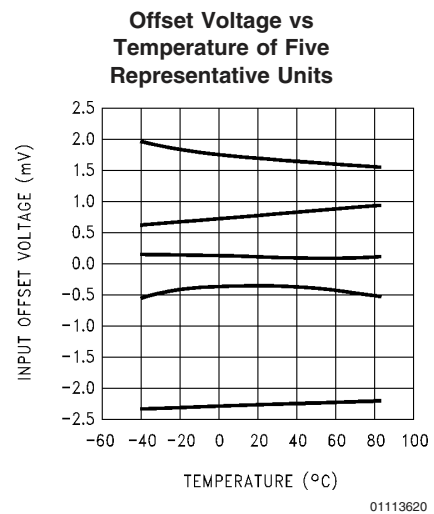
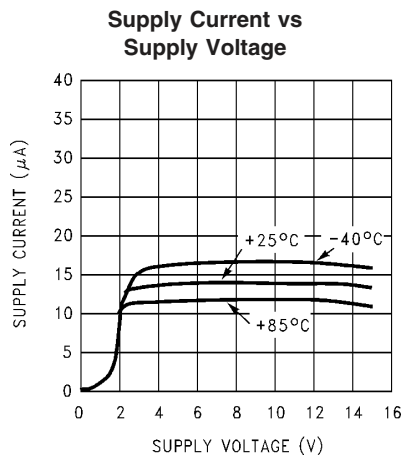
Note 9: For operating at elevated temperatures the device must be derated based on the thermal resistance θ_{JA} with $P_D = (T_J - T_A)/\theta_{JA}$.

Note 10: All numbers apply for packages soldered directly into a PC board.

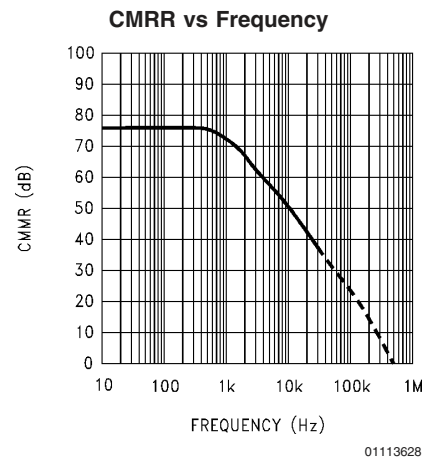
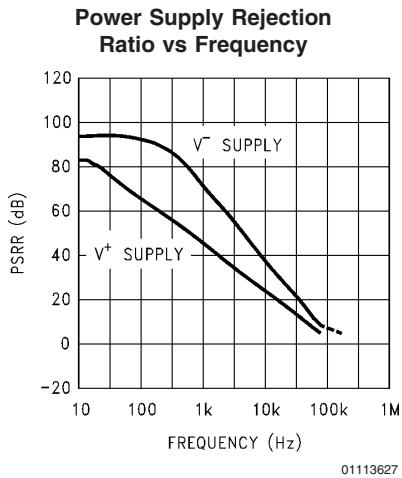
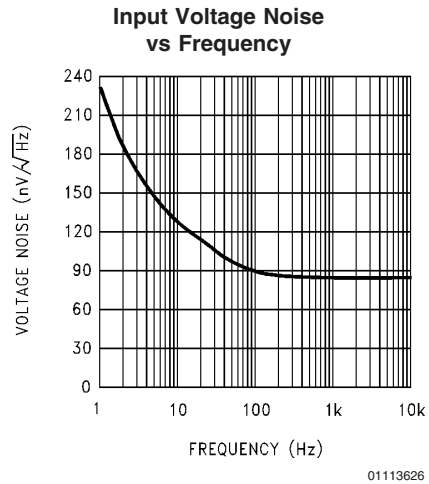
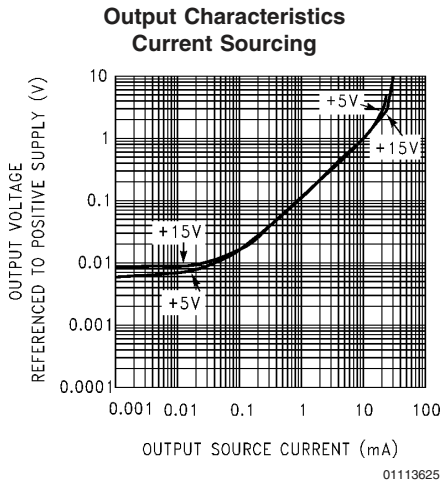
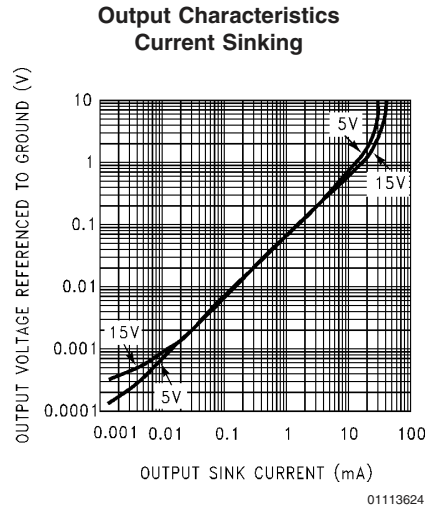
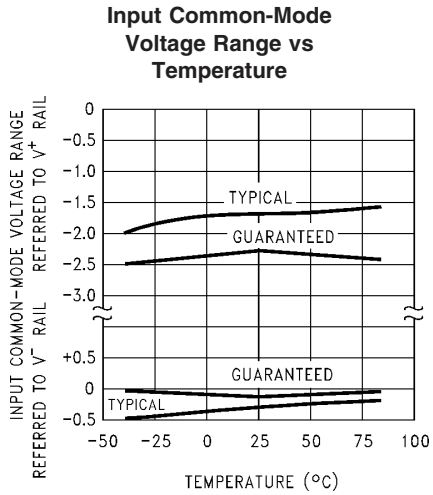
Note 11: Do not connect output to V^+ when V^+ is greater than 13V or reliability may be adversely affected.

Typical Performance Characteristics

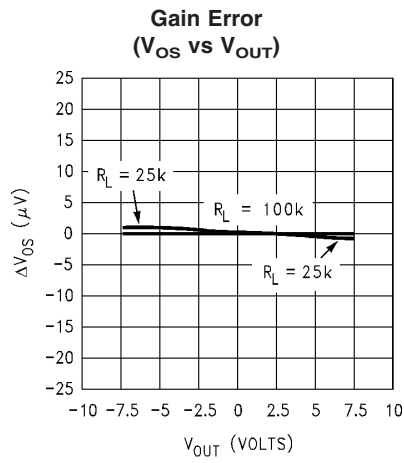
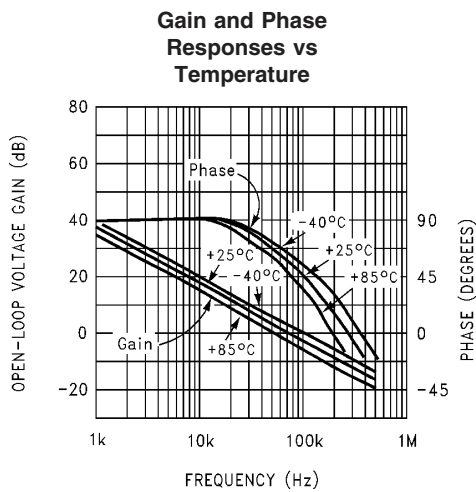
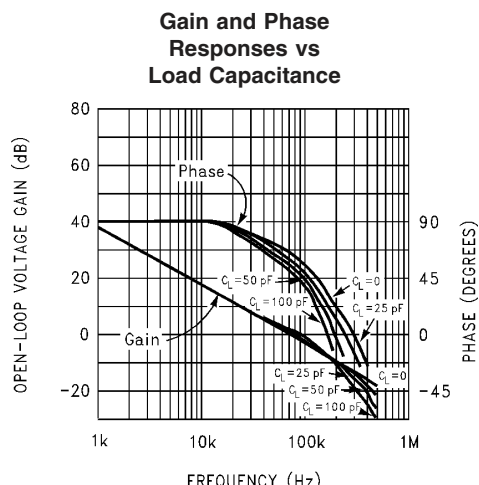
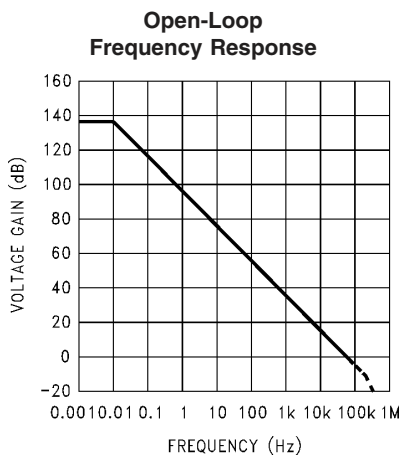
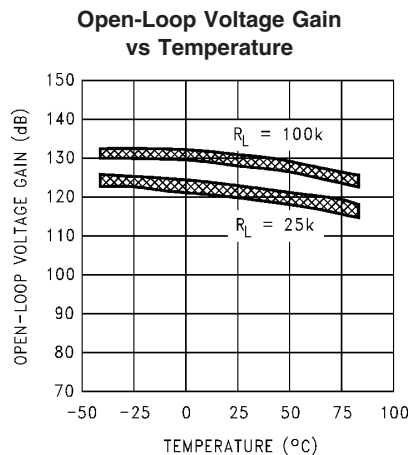
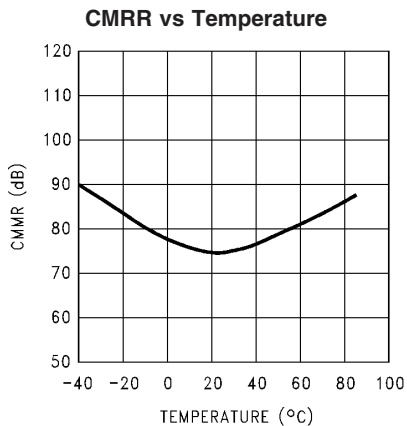
$V_S = \pm 7.5V$, $T_A = 25^\circ C$ unless otherwise specified



Typical Performance Characteristics $V_S = \pm 7.5V$, $T_A = 25^\circ C$ unless otherwise specified (Continued)

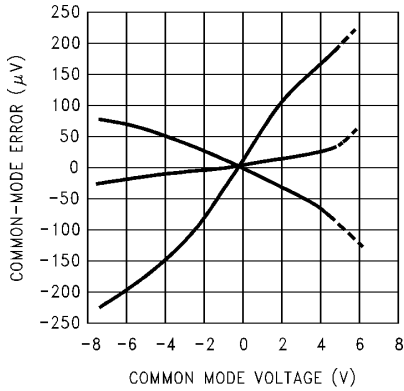


Typical Performance Characteristics $V_S = \pm 7.5V$, $T_A = 25^\circ C$ unless otherwise specified (Continued)



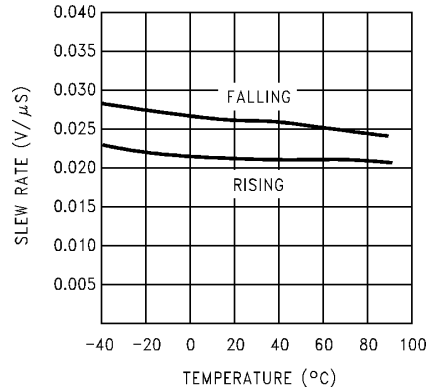
Typical Performance Characteristics $V_S = \pm 7.5V$, $T_A = 25^\circ C$ unless otherwise specified (Continued)

Common-Mode Error vs Common-Mode Voltage of Three Representative Units



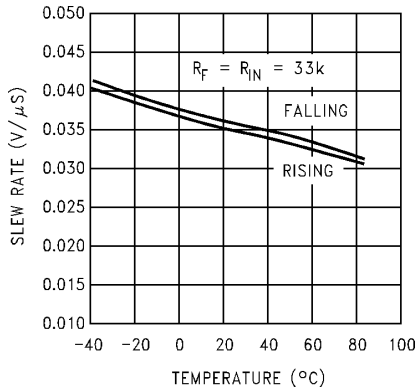
01113635

Non-Inverting Slew Rate vs Temperature



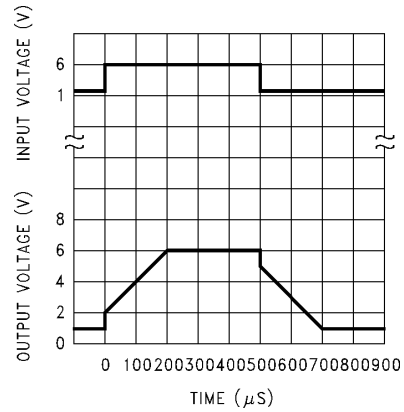
01113636

Inverting Slew Rate vs Temperature



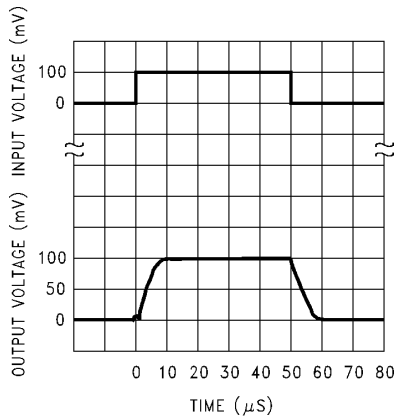
01113637

Non-Inverting Large Signal Pulse Response ($A_V = +1$)



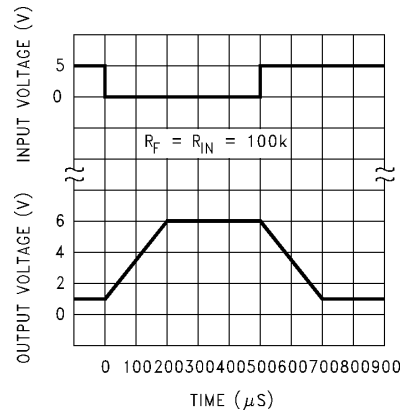
01113638

Non-Inverting Small Signal Pulse Response



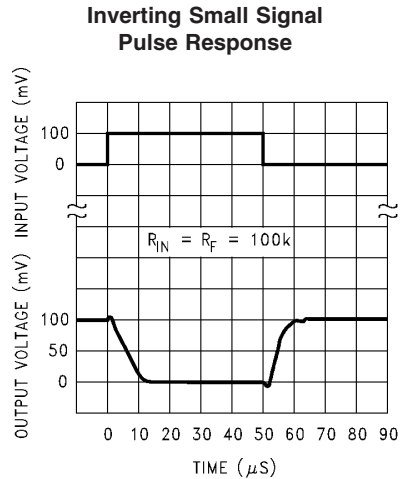
01113639

Inverting Large-Signal Pulse Response

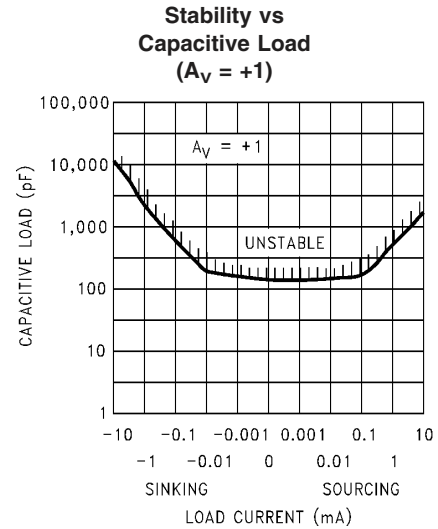


01113640

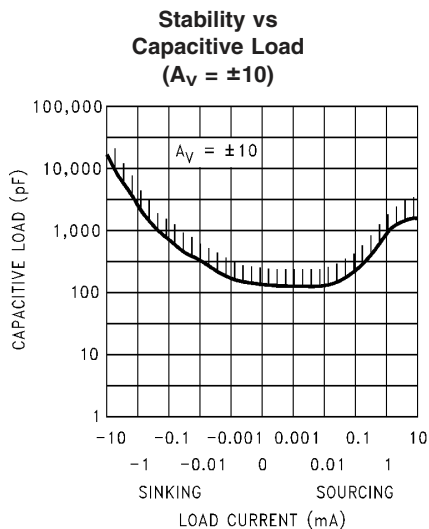
Typical Performance Characteristics $V_S = \pm 7.5V$, $T_A = 25^\circ C$ unless otherwise specified (Continued)



01113641



01113642



01113643

Applications Hints

AMPLIFIER TOPOLOGY

The LMC6041 incorporates a novel op-amp design topology that enables it to maintain rail-to-rail output swing even when driving a large load. Instead of relying on a push-pull unity gain output buffer stage, the output stage is taken directly from the internal integrator, which provides both low output impedance and large gain. Special feed-forward compensation design techniques are incorporated to maintain stability over a wider range of operating conditions than traditional micropower op-amps. These features make the LMC6041 both easier to design with, and provide higher speed than products typically found in this ultra-low power class.

COMPENSATING FOR INPUT CAPACITANCE

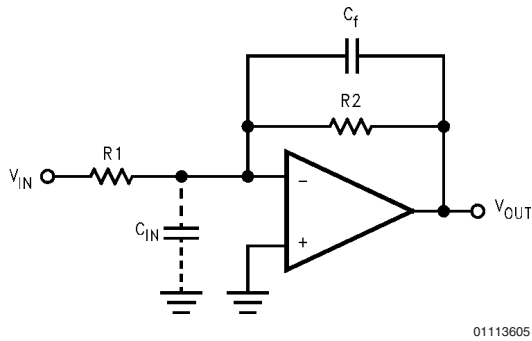
It is quite common to use large values of feedback resistance with amplifiers with ultra-low input current, like the LMC6041.

Although the LMC6041 is highly stable over a wide range of operating conditions, certain precautions must be met to

achieve the desired pulse response when a large feedback resistor is used. Large feedback resistors and even small values of input capacitance, due to transducers, photo-diodes, and circuits board parasitics, reduce phase margins.

When high input impedance are demanded, guarding of the LMC6041 is suggested. Guarding input lines will not only reduce leakage, but lowers stray input capacitance as well. (See **Printed-Circuit-Board Layout for High Impedance Work.**)

Applications Hints (Continued)



01113605

FIGURE 1. Cancelling the Effect of Input Capacitance

The effect of input capacitance can be compensated for by adding a capacitor, C_f , around the feedback resistor (as in *Figure 1*) such that:

$$\frac{1}{2\pi R_1 C_{IN}} \geq \frac{1}{2\pi R_2 C_f}$$

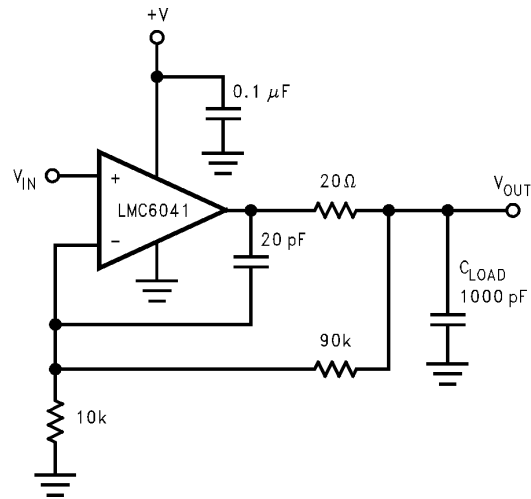
or

$$R_1 C_{IN} \leq R_2 C_f$$

Since it is often difficult to know the exact value of C_{IN} , C_f can be experimentally adjusted so that the desired pulse response is achieved. Refer to the LMC660 and the LMC662 for a more detailed discussion on compensating for input capacitance.

CAPACITIVE LOAD TOLERANCE

Direct capacitive loading will reduce the phase margin of many op-amps. A pole in the feedback loop is created by the combination of the op-amp's output impedance and the capacitive load. This pole induces phase lag at the unity-gain crossover frequency of the amplifier resulting in either an oscillatory or underdamped pulse response. With a few external components, op amps can easily indirectly drive capacitive loads, as shown in *Figure 2*.

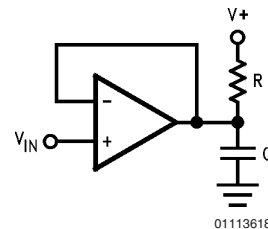


01113606

FIGURE 2. LMC6041 Noninverting Gain of 10 Amplifier, Compensated to Handle Capacitive Loads

In the circuit of *Figure 2*, R_1 and C_1 serve to counteract the loss of phase margin by feeding the high frequency component of the output signal back to the amplifier's inverting input, thereby preserving phase margin in the overall feedback loop.

Capacitive load driving capability is enhanced by using a pull up resistor to V^+ (*Figure 3*). Typically a pull up resistor conducting 10 μ A or more will significantly improve capacitive load responses. The value of the pull up resistor must be determined based on the current sinking capability of the amplifier with respect to the desired output swing. Open loop gain of the amplifier can also be affected by the pull up resistor (see Electrical Characteristics).



01113618

FIGURE 3. Compensating for Large Capacitive Loads with a Pull Up Resistor

PRINTED-CIRCUIT-BOARD LAYOUT FOR HIGH-IMPEDANCE WORK

It is generally recognized that any circuit which must operate with less than 1000 pA of leakage current requires special layout of the PC board. When one wishes to take advantage of the ultra-low bias current of the LMC6041, typically less than 2fA, it is essential to have an excellent layout. Fortunately, the techniques of obtaining low leakages are quite simple. First, the user must not ignore the surface leakage of the PC board, even though it may sometimes appear acceptably low, because under conditions of high humidity or dust or contamination, the surface leakage will be appreciable.

To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LMC6041's inputs and the

Applications Hints (Continued)

terminals of capacitors, diodes, conductors, resistors, relay terminals, etc. connected to the op-amp's inputs, as in *Figure 4*. To have a significant effect, guard rings should be placed on both the top and bottom of the PC board. This PC foil must then be connected to a voltage which is at the same voltage as the amplifier inputs, since no leakage current can flow between two points at the same potential. For example, a PC board trace-to-pad resistance of $10^{12}\Omega$, which is normally considered a very large resistance, could leak 5 pA if the trace were a 5V bus adjacent to the pad of the input. This would cause a 100 times degradation from the LMC6041's actual performance. However, if a guard ring is held within 5 mV of the inputs, then even a resistance of $10^{11}\Omega$ would cause only 0.05 pA of leakage current. See *Figure 5* for typical connections of guard rings for standard op-amp configurations.

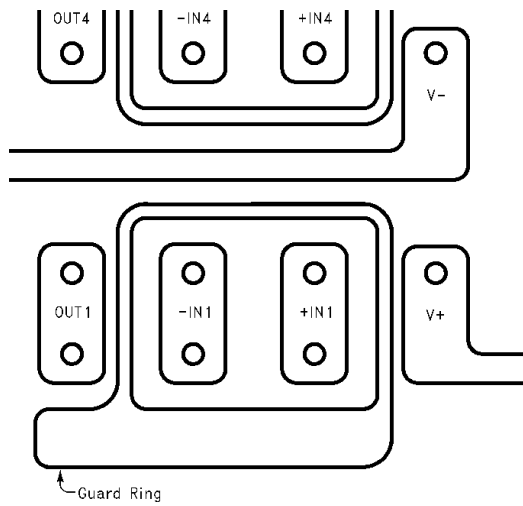
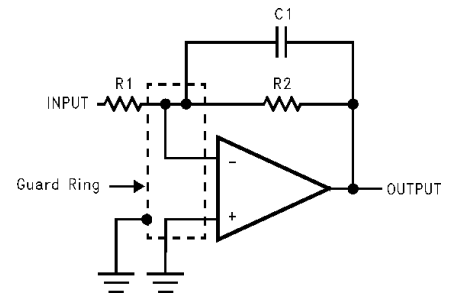


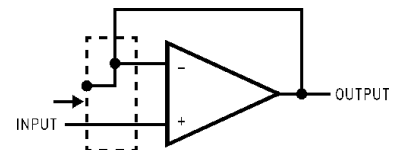
FIGURE 4. Example of Guard Ring in P.C. Board Layout

01113607



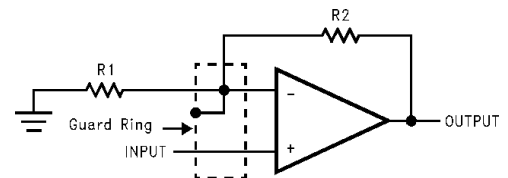
Inverting Amplifier

01113608



Follower

01113609

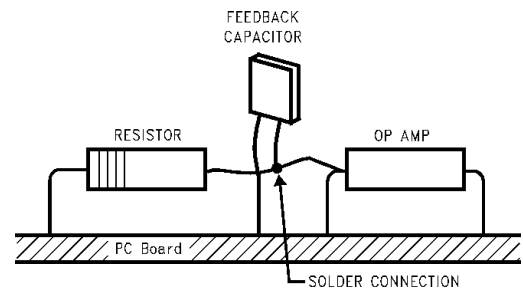


Non-Inverting Amplifier

01113610

FIGURE 5. Typical Connections of Guard Rings

The designer should be aware that when it is inappropriate to lay out a PC board for the sake of just a few circuits, there is another technique which is even better than a guard ring on a PC board: Don't insert the amplifier's input pin into the board at all, but bend it up in the air and use only air as an insulator. Air is an excellent insulator. In this case you may have to forego some of the advantages of PC board construction, but the advantages are sometimes well worth the effort of using point-to-point up-in-the-air wiring. See *Figure 6*.



(Input pins are lifted out of PC board and soldered directly to components. All other pins connected to PC board.)

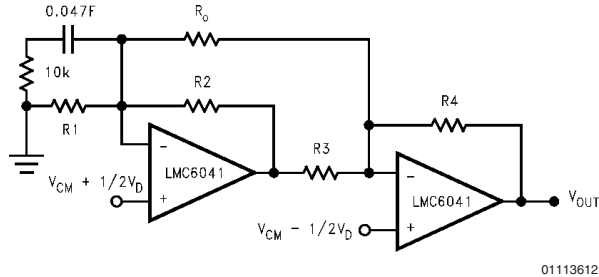
01113611

FIGURE 6. Air Wiring

Typical Single-Supply Applications

($V^+ = 5.0 V_{DC}$)

The extremely high input impedance, and low power consumption, of the LMC6041 make it ideal for applications that require battery-powered instrumentation amplifiers. Examples of these type of applications are hand-held pH probes, analytic medical instruments, magnetic field detectors, gas detectors, and silicon based pressure transducers.



01113612

FIGURE 7. Two Op-Amp Instrumentation Amplifier

The circuit in Figure 7 is recommended for applications where the common-mode input range is relatively low and the differential gain will be in the range of 10 to 1000. This two op-amp instrumentation amplifier features an independent adjustment of the gain and common-mode rejection trim, and a total quiescent supply current of less than 28 μ A. To maintain ultra-high input impedance, it is advisable to use ground rings and consider PC board layout an important part of the overall system design (see Printed-Circuit-Board Lay-

out for High Impedance Work). Referring to Figure 7, the input voltages are represented as a common-mode input V_{CM} plus a differential input V_D .

Rejection of the common-mode component of the input is accomplished by making the ratio of $R1/R2$ equal to $R3/R4$. So that where,

$$\frac{R3}{R4} = \frac{R2}{R1}$$

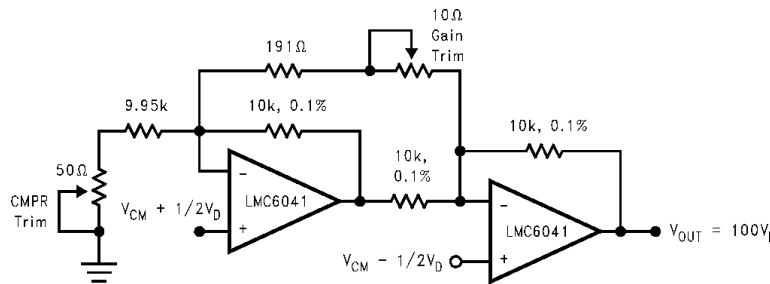
$$V_{OUT} = \frac{R4}{R3} \left(1 + \frac{R3}{R4} + \frac{R2 + R3}{R_O} \right) V_D$$

A suggested design guideline is to minimize the difference of value between $R1$ through $R4$. This will often result in improved resistor tempco, amplifier gain, and CMRR over temperature. If $R_N = R1 = R2 = R3 = R4$ then the gain equation can be simplified:

$$V_{OUT} = 2 \left(1 + \frac{R_N}{R_O} \right) V_D$$

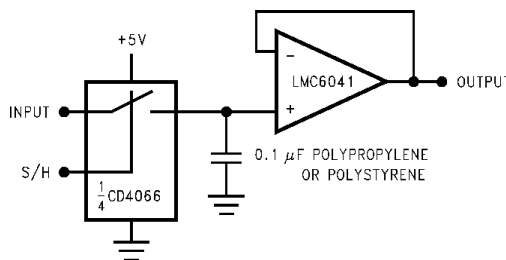
Due to the “zero-in, zero-out” performance of the LMC6041, and output swing rail-rail, the dynamic range is only limited to the input common-mode range of $0V$ to $V_S - 2.3V$, worst case at room temperature. This feature of the LMC6041 makes it an ideal choice for low-power instrumentation systems.

A complete instrumentation amplifier designed for a gain of 100 is shown in Figure 8. Provisions have been made for low sensitivity trimming of CMRR and gain.



01113613

FIGURE 8. Low-Power Two-Op-Amp Instrumentation Amplifier



01113614

FIGURE 9. Low-Leakage Sample and Hold

Typical Single-Supply Applications ($V^+ = 5.0 V_{DC}$) (Continued)

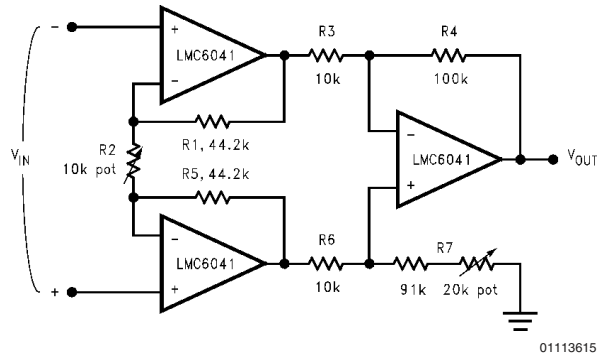


FIGURE 10. Instrumentation Amplifier

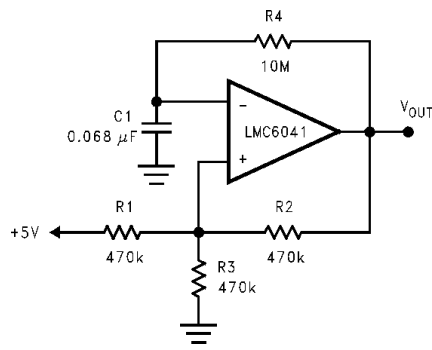


FIGURE 11. 1 Hz Square-Wave Oscillator

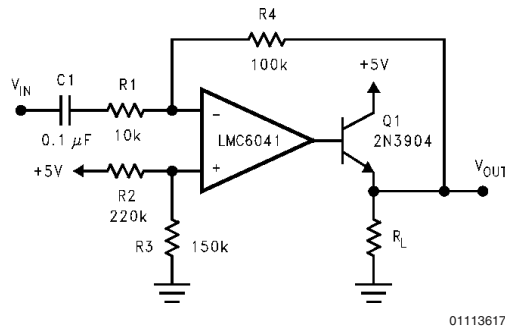
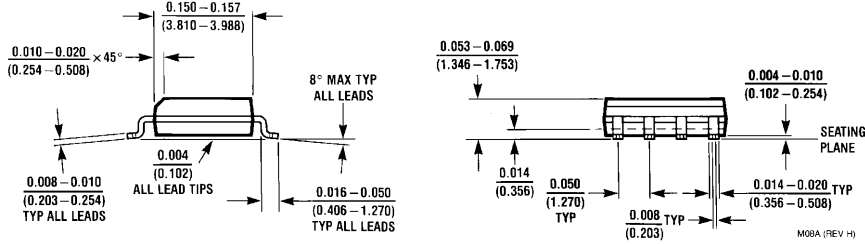
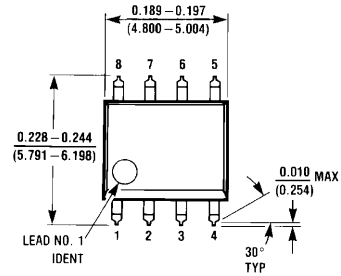


FIGURE 12. AC Coupled Power Amplifier

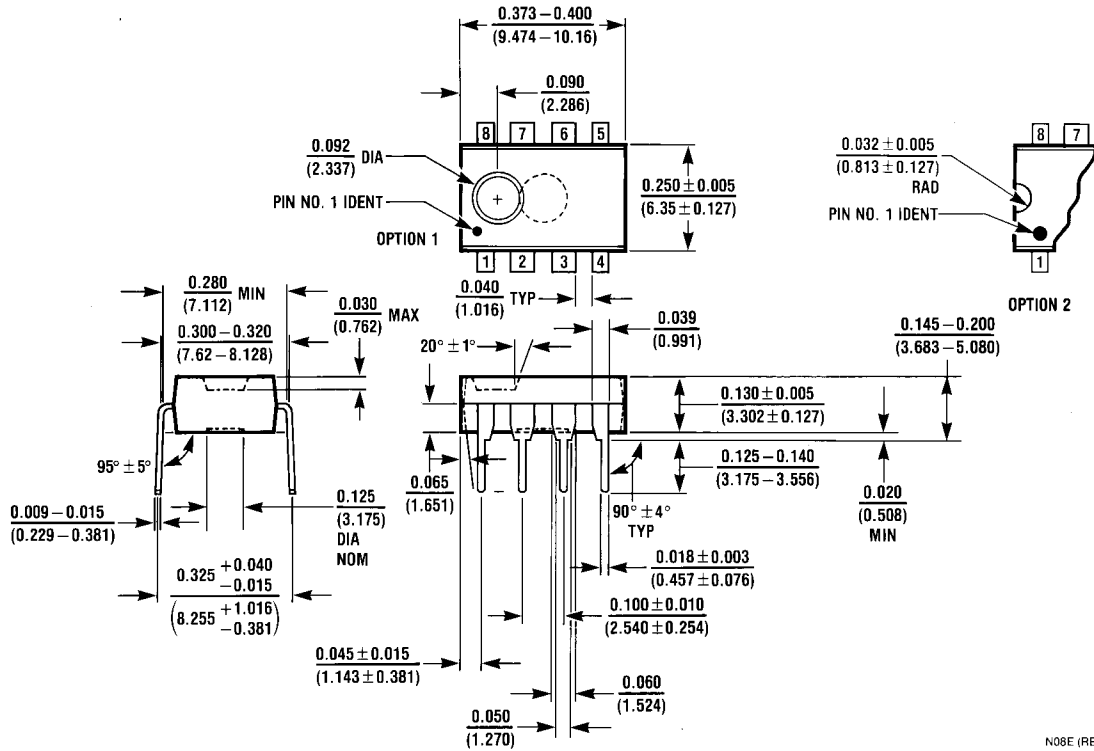
Ordering Information

Package	Temperature Range	NSC Drawing	Transport Media
	Industrial -40°C to +85°C		
8-Pin Small Outline	LMC6041AIM, LMC6041AIMX LMC6041IM, LMC6041IMX	M08A	Rail Tape and Reel
8-Pin Molded DIP	LMC6041AIN LM6041IN	N08E	Rail

Physical Dimensions inches (millimeters) unless otherwise noted



8-Pin Small Outline
 Order Number LMC6041AIM, LMC6041AIMX, LMC6041IM or LMC6041IMX
 NS Package Number M08A



8-Pin Molded DIP
 Order Number LMC6041AIN or LMC6041IN
 NS Package Number N08E

Notes

National does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and National reserves the right at any time without notice to change said circuitry and specifications.

For the most current product information visit us at www.national.com.

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT AND GENERAL COUNSEL OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

BANNED SUBSTANCE COMPLIANCE

National Semiconductor certifies that the products and packing materials meet the provisions of the Customer Products Stewardship Specification (CSP-9-111C2) and the Banned Substances and Materials of Interest Specification (CSP-9-111S2) and contain no "Banned Substances" as defined in CSP-9-111S2.



National Semiconductor
Americas Customer
Support Center
Email: new.feedback@nsc.com
Tel: 1-800-272-9959

National Semiconductor
Europe Customer Support Center
Fax: +49 (0) 180-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 69 9508 6208
English Tel: +44 (0) 870 24 0 2171
Français Tel: +33 (0) 1 41 91 8790

National Semiconductor
Asia Pacific Customer
Support Center
Email: ap.support@nsc.com

National Semiconductor
Japan Customer Support Center
Fax: 81-3-5639-7507
Email: jpn.feedback@nsc.com
Tel: 81-3-5639-7560