MOTOROLA

MC75368

DUAL MECL-to-MOS DRIVER

SILICON MONOLITHIC INTEGRATED CIRCUIT

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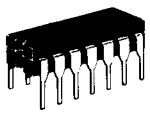
DUAL MECL-to-MOS DRIVER

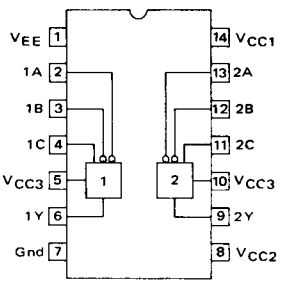
The MC75368 is a dual MECL-to-MOS driver and interface circuit. The device accepts standard MECL 10,000 and IBM grounded-reference ECL input signals and creates high-current and high-voltage output levels suitable for driving MOS circuits. Specifically, it may be used to drive address, control, and timing inputs for several types of MOS RAMs. The device may also be used as a MECL-to-MTTL translator.

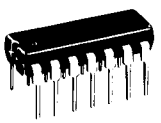
The MC75368 is optimized for higher voltage capability.

- Dual MECL-to-MOS Driver
- Dual MECL-to-MTTL Driver
- Versatile Interface Circuit for Use Between MECL and High-Current, High-Voltage Systems

L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116

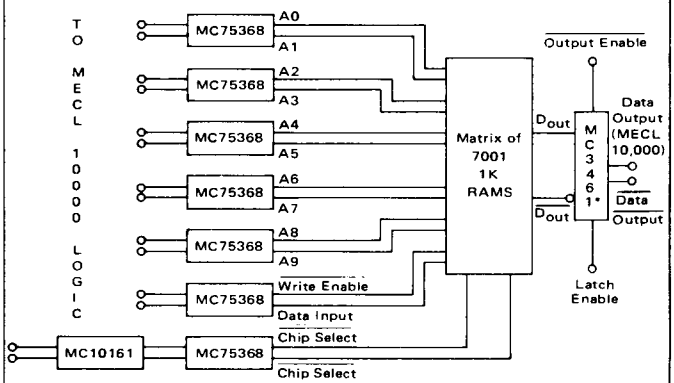






P SUFFIX
PLASTIC PACKAGE
CASE 646

FIGURE 1 – TYPICAL APPLICATION WITH 7001 1K NMOS RAM



*MC3461 Dual Sense Amplifier

FUNCTION TABLE

Input Voltage Conditions		Output
Differential	**Logic Level**	
(More positive of A or B) -C	A B C	Y
($V_{ID} \geq 150$ mV)	L H L H L H H H L	L
(-150 mV $\leq V_{ID} \leq$ 150 mV)	X X X	Indeterminate
($V_{ID} \leq$ -150 mV)	L L H	H

H = high logic level, L = low logic level,
X = irrelevant

MAXIMUM RATINGS (Unless otherwise noted, voltages measured with respect to GND terminals, T_A = 25°C.)

Rating	Symbol	Value	Unit
Power Supply Voltages	V_{CC1}	-0.5 to 7.0	Vdc
	V_{CC2}	-0.5 to 22	Vdc
	V_{CC3}	-0.5 to 30	Vdc
	V_{EE}	-8.0 to 0.5	Vdc
Most Negative of V_{CC1}, V_{CC2}, or V_{CC3} with respect to V_{EE}	–	-0.5	Vdc
Input Voltage	V_I	-8.0 to 0.5	Vdc
Inter-Input Voltage(1)	–	5.5	Vdc
Most negative Input Voltage with respect to V_{EE}	$V_I - V_{EE}$	-5.0	Vdc
Power Dissipation (Package Limitation)			
Ceramic Package @ T_A = 25°C	P_D	1000	mW
Derate above T_A = 25°C	$1/R_{\theta JA}$	6.6	mW/°C
Plastic Package @ T_A = 25°C	P_D	830	mW
Derate above T_A = 25°C	$1/R_{\theta JA}$	6.6	mW/°C
Ceramic Package @ T_C = 25°C	P_D	3.0	Watts
Derate above T_C = 25°C	$1/R_{\theta JC}$	20	mW/°C
Plastic Package @ T_C = 25°C	P_D	1.8	Watts
Derate above T_C = 25°C	$1/R_{\theta JC}$	14	mW/°C
Operating Ambient Temperature Range	T_A	0 to 70	°C
Storage Temperature Range	T_{stg}	-65 to 150	°C

(1) With respect to any pair of inputs to either of the input gates.

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply Voltages	V_{CC1}	4.75	5.0	5.25	V
	V_{CC2}	4.75	20	22	V
	V_{CC3}	V_{CC2}	24	28	V
	$V_{CC3} - V_{CC2}$	0	4.0	10	V
	V_{EE}	-4.68	-5.2	-5.72	V
Operating Ambient Temperature Range	T_A	0	–	70	°C
DEFINITION OF INPUT LOGIC LEVELS					
Input Voltage – High Logic State (Any Input) (1)	V_{IH}	-1.5	–	-0.7	V
Input Voltage – Low Logic State (Any Input) (1)	V_{IL}	V_{EE}	–	V_{IH}-150	mV
Input Differential Voltage – High Logic State (2)	V_{IDH}	150	–	–	mV
Input Differential Voltage – Low Logic State (2)	V_{IDL}	-150	–	–	mV

(1) The definition of these Logic Levels use Algebraic System of notation.

(2) The input differential voltage is measured from the more positive inverting input (A or B) with respect to the non-inverting input (C) of the same gate.

ELECTRICAL CHARACTERISTICS (Unless otherwise noted, specifications apply over recommended power supply and temperature ranges. Typical values measured at V_{CC1} = 5.0 V, V_{EE} = -5.2 V, T_A = 25°C and V_{CC2} = 20, V_{CC3} = 24 V.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage – High Logic State (V_{CC3} = V_{CC2} + 3.0 V, V_{IDL} = -150 mV, I_{OH} = -100 μA)	V_{OH1}	V_{CC2} - 0.3	V_{CC2} - 0.1	–	V
(V_{CC3} = V_{CC2} + 3.0 V, V_{IDL} = -150 mV, I_{OH} = -10 mA)	V_{OH2}	V_{CC2} - 1.2	V_{CC2} - 0.9	–	V
(V_{CC3} = V_{CC2}, V_{IDL} = -150 mV, I_{OH} = -50 μA)	V_{OH3}	V_{CC2} - 1.0	V_{CC2} - 0.7	–	V
(V_{CC3} = V_{CC2}, V_{IDL} = -150 mV, I_{OH} = -10 mA)	V_{OH4}	V_{CC2} - 2.3	V_{CC2} - 1.8	–	V
Output Voltage – Low Logic State (V_{IDH} = 150 mV, I_{OL} = 10 mA)	V_{OL1}	–	0.15	0.3	V
(V_{IDH} = 150 mV, I_{OL} = 30 mA) 10 V ≤ V_{CC3} ≤ 22 V 10 V ≤ V_{CC2} ≤ 28 V	V_{OL2}	– –	– 0.2	– 0.4	V
Output Clamp Voltage (V_{IDH} = 500 mV, I_{OC} = 20 mA)	V_{OC}	–	–	V_{CC2}+1.5 V	V
Input Current – High Logic State (V_{EE} = -5.72 V, V_{IL} = -5.72 V, V_{IH} = -0.7 V)	I_{IH}	–	300	800	μA
Input Current – Low Logic State (V_{IH} = -0.7 V, V_{IL} = -2.0 V) (V_{EE} = -5.72 V, V_{IH} = -0.7 V, V_{IL} = -5.72 V)	I_{IL1} I_{IL2}	– –	– –	-10 -100	μA
Power Supply Current – Both Outputs High Logic State (V_{CC} = 5.25 V, V_{CC2} = 22 V, V_{CC3} = 26 V V_{EE} = -5.72 V, V_{IL} (A) and (B) = -2.0 V, V_{IH}(C) = -0.7 V, I_{OH} = 0)	$I_{CC1(H)}$ $I_{CC2(H)}$ $I_{CC3(H)}$ $I_{EE(H)}$	– – – –	21 -1.1 0.6 -21	38 +0.25 1.0 -38	mA mA mA mA
Power Supply Current – Both Outputs Low Logic State (V_{CC1} = 5.25 V, V_{CC2} = 22 V, V_{CC3} = 28 V, V_{EE} = -5.72 V, V_{IH}(A) and (B) = -0.7 V, V_{IL}(C) = -2.0 V, I_{OL} = 0)	$I_{CC1(L)}$ $I_{CC2(L)}$ $I_{CC3(L)}$ $I_{EE(L)}$	– – – –	13 0.5 4.0 -21	24 1.0 7.0 -38	mA mA mA mA
Power Supply Current – Both Outputs High Logic State (V_{CC1} = 5.25 V, V_{CC2} = 22.V, V_{CC3} = 22 V, V_{EE} = -5.72 V, V_{IL}(A) and (B) = -2.0 V, V_{IH}(C) = -0.7 V, I_{OL} = 0)	$I_{CC2(H)}$ $I_{CC3(H)}$	– –	– –	0.25 0.25	mA mA
Power Supply Current – Stand By Condition (V_{CC1} = 0 V, V_{CC2} = 22 V, V_{CC3} = 22 V, V_{EE} = 0 V, V_{IH}(A) and (B) = -0.7 V, V_{IL}(C) = -2.0 V, I_{OL} = 0)	$I_{CC2(S)}$ $I_{CC3(S)}$	– –	– –	0.25 0.25	mA mA

SWITCHING CHARACTERISTICS (Unless otherwise noted, V_{CC1} = 5.0 V, V_{EE} = -5.2 V, T_A = 25°C and V_{CC2} = 20 V.)

Characteristic	Symbol	Min	Typ	Max	Unit
Delay Time – Low to High Output Logic Level (V_{CC3} = 24 V) (V_{CC3} = 20 V)	t_{DLH}	– –	12 13	24 25	ns
Delay Time – High to Low Output Logic Level (V_{CC3} = 24 V) (V_{CC3} = 20 V)	t_{DHL}	– –	13 15	24 26	ns
Transition Time, Low-to-High Output Logic Level (V_{CC3} = 24 V) (V_{CC3} = 20 V)	t_{TLH}	– –	19 20	30 30	ns
Transition Time, High-to-Low Output Logic Level (V_{CC3} = 24 V) (V_{CC3} = 20 V)	t_{THL}	– –	20 18	33 30	ns
Propagation Delay Time, Low-to-High Logic Level (V_{CC3} = 24 V) (V_{CC3} = 20 V)	t_{PLH}	– –	31 33	54 55	ns
Propagation Delay Time, High-to-Low Logic Level (V_{CC3} = 24 V) (V_{CC3} = 20 V)	t_{PHL}	– –	33 33	57 56	ns

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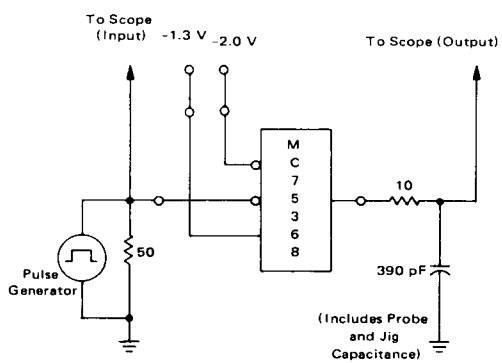
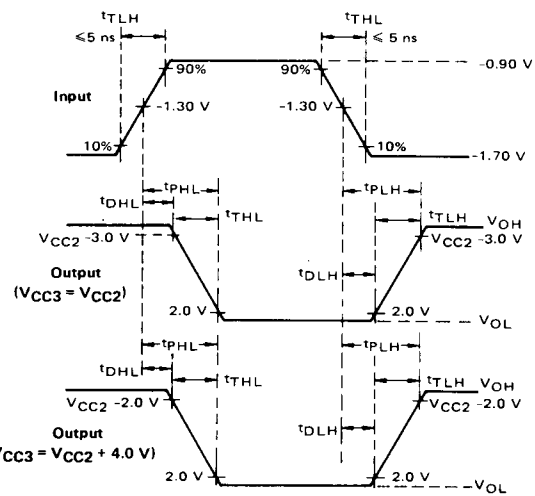
FIGURE 2 – SWITCHING TIMES TEST CIRCUIT



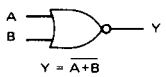
The pulse generator has the following characteristics:
PRR = 1 MHz, $z_o \approx 50\ \Omega$.
Duty Cycle = 50%

FIGURE 3 – SWITCHING TIMES WAVEFORM



APPLICATIONS INFORMATION
MODES OF OPERATION

FIGURE 4 – POSITIVE-NOR GATE

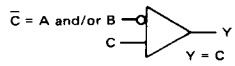


FUNCTION TABLE

CONFIGURATION	INPUTS A	B	C	OUTPUT Y
C at V_{BB}	L	L	V_{BB}	H
	H	X	V_{BB}	L
	X	H	V_{BB}	L

H = High Level, L = Low Level, X = Irrelevant
V_{BB} = Reference Supply voltage for MECL 10,000.

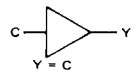
FIGURE 5 – DIFFERENTIAL MECL LINE RECEIVER



FUNCTION TABLE

CONFIGURATION	INPUTS A	B	C	OUTPUT Y
A and B connected together	H	H	L	L
	L	L	H	H
A not used but connected low	L	H	L	L
	L	L	H	H
B not used but connected low	H	L	L	L
	L	L	H	H

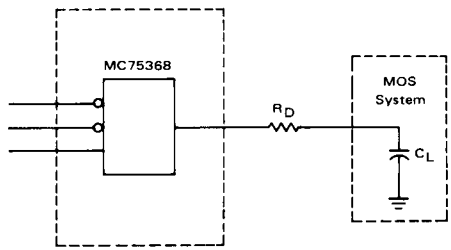
FIGURE 6 – NON-INVERTING GATE



FUNCTION TABLE

CONFIGURATION	INPUTS A	B	C	OUTPUT Y
A and B at V_{BB}	V_{BB}	V_{BB}	L	L
	V_{BB}	V_{BB}	H	H
A at V_{BB}, B connected low	V_{BB}	L	L	L
	V_{BB}	L	H	H
B at V_{BB}, A connected low	L	V_{BB}	L	L
	L	V_{BB}	H	H

FIGURE 7 – USE OF DAMPING RESISTOR TO REDUCE OR ELIMINATE OUTPUT TRANSIENT OVERSHOOT IN CERTAIN MC75368 APPLICATIONS



Note: $R_D \approx 10\Omega$ to 30Ω (optional)

The need for four separate power supplies V_{CC1}, V_{CC2}, V_{CC3} and V_{EE} can be avoided in many cases by tying V_{CC2} to V_{CC3}. However, performance advantages can be obtained by connecting either one or both V_{CC3} pins to an additional power supply of higher voltage than V_{CC2}. Both V_{CC3} pins do not have to be held at the same voltage. For MECL-to-TTL level converter applications both V_{CC2} and V_{CC3} are generally connected to a +5.0 V power source.

By providing two out-of-phase (A and B) inputs and one in-phase (C) input, each gate can be used as positive NOR, or as a inverting or non-inverting gate. This flexibility is achieved by connecting an externally supplied MECL 10,000 Series reference supply voltage (V_{BB}) to the appropriate input as shown in Figures 4 thru 6. An unused out-of-phase input should be tied low or connected to the other out-of-phase input of the same gate. The required V_{BB} voltage source may be obtained from MECL 10,000 Series devices such as the MC10115 line receiver, or by connecting the output of a MECL 10,000 gate, like the MC10102, to the respective out-of-phase inputs (as an example connect pins 4 and 5 to 2 of the MC10102 to obtain a V_{BB} reference voltage).

When driven differentially, the MC75368 may be used as a differential MECL line receiver, without the need for the V_{BB} reference voltage.

Undesirable output transient overshoot due to load or wiring inductance and the fast switching speeds of the MC75368 can be eliminated or reduced by adding a small amount of series resistance. The value of this damping resistance is dependent on specific load characteristics and switching speed but typical values lie in the range of 10 to 30 ohms. This is illustrated in Figure 7.