Atmel U3280M

Transponder Interface for Microcontroller

DATASHEET

Features

- Contactless power supply and communication interface
- Up to 10Kbaud data rate (R/O)
- Power management for contactless and battery power supply
- Frequency range 100kHz to 150kHz
- 32 x 16-bit EEPROM
- Two-wire serial interface
- Shift register supported bi-phase and Manchester modulator stage
- Reset I/O line
- Field clock extractor
- Field and gap detection output for wake-up and data reception
- Field modulator with energy-saving damping stage

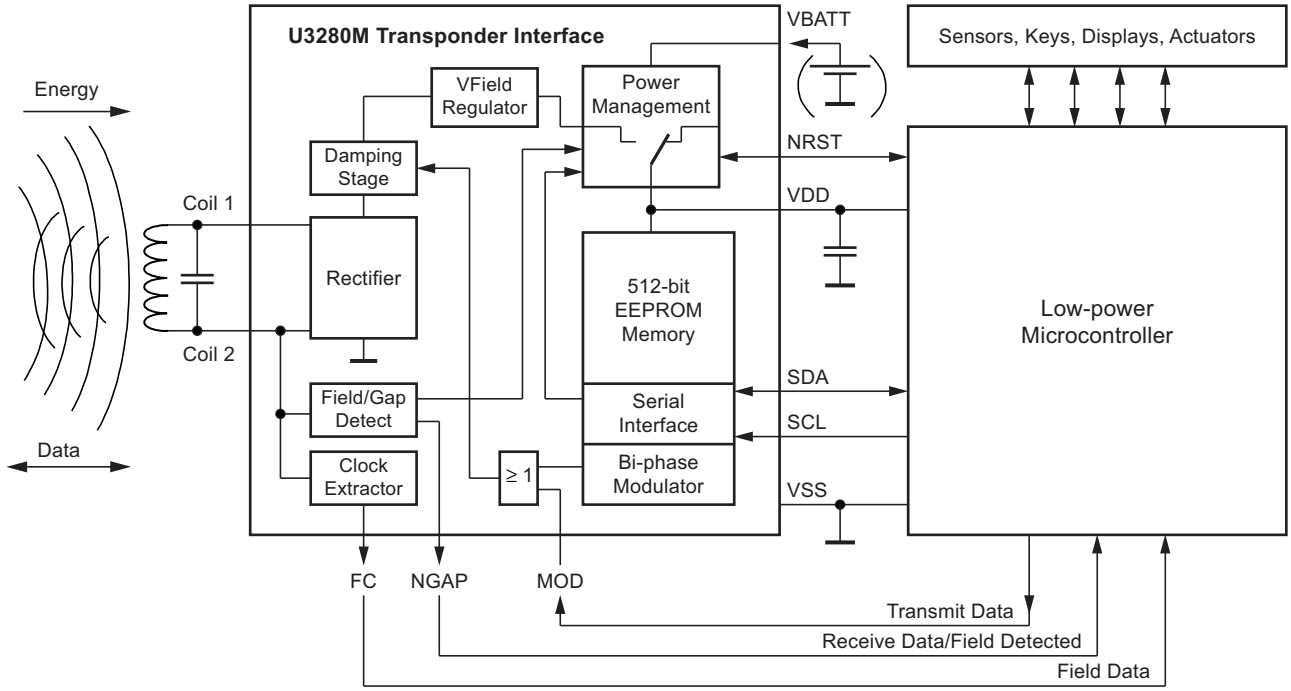
Applications

- Main areas
  - Access control
  - Telemetry
  - Wireless sensors
- Examples:
  - Wireless passive access and active alarm control for protection of valuables
  - Contactless position sensors for alignments of machines
  - Contactless status verification and/or data readout from sensors

1. Description

The Atmel® U3280M is a transponder interface for use in contactless ID systems, remote control systems, tag and sensor applications. It supplies the microcontroller with power from an RF field via an LC-resonant circuit and it enables contactless bi-directional data communication via this RF field. It includes power management that handles switching between the magnetic field and a battery power supply. To store permanent data like an identifier code and configuration data, the Atmel U3280M includes a 512-bit EEPROM with a serial interface.

Figure 1-1. Block Diagram



2. Pin Configuration

Figure 2-1. Pinning

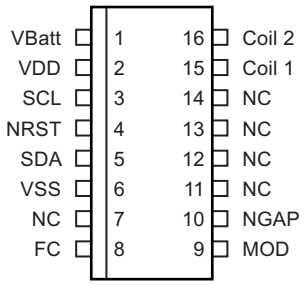


Table 2-1. Pin Description

Pin	Symbol	Function
1	VBatt	Power supply voltage input to connect a battery
2	VDD	Power supply voltage for the microcontroller and EEPROM. At this pin a buffer capacitor (0.5 to 10µF) must be connected to buffer the voltage during field supply and to block the VDD of the microcontroller.
3	SCL	Serial clock line
4	NRST	Reset line bi-directional
5	SDA	Serial data line
6	VSS	Circuit ground
7	NC	Not connected
8	FC	Field clock output of the front-end clock extractor
9	MOD	Modulation input
10	NGAP	Gap and field detect output
11	NC	Not connected
12	NC	Not connected
13	NC	Not connected
14	NC	Not connected
15	Coil 1	Coil input 1. Use pin to connect a resonant circuitry for communication and field supply
16	Coil 2	Coil input 2. Use pin to connect a resonant circuitry for communication and field supply

3. Functional Description

3.1 Transponder Interface

The Atmel® U3280M is a transponder interface IC that can operate microcontrollers using wireless technology and battery independently. Wireless data communication and the power supply are handled via an electromagnetic field and the coil antenna of the transponder interface. The Atmel U3280M consists of a rectifier stage for the antenna, power management to handle field and battery power supplies, a damping modulator, and a field-gap detection stage for contactless data communication. Furthermore, a field clock extraction and an EEPROM are on-chip.

The internal rectifier stage rectifies the AC from the LC-resonant circuit at the coil inputs and supplies the Atmel U3280M device and an additional microcontroller device with power. It is also possible to supply the device via the V_{Batt} input with DC from a battery. The power management handles switching between battery supply (V_{Batt} pin) and field supply automatically. It switches to field supply if a field is applied at the coil, and it switches back to battery if the field is removed. The voltage from the coil or the V_{Batt} pin is output at the V_{DD} pin to supply the microcontroller or any other suited device. At the V_{DD} pin a capacitor must be connected to smooth and buffer the supply voltage. This capacitor is also necessary to buffer the supply voltage during communication (damping and gaps in the field).

For communication, the chip contains a damping stage and gap-detect circuitry. By means of the damping stage the coil voltage can be modulated to transmit data via the field. It can be controlled with the modulator input (MOD pin) via the microcontroller. The gap-detection circuitry detects gaps in the field and outputs the gap/field signal at the gap-detect output (pin NGAP).

To store data like keycodes, identifiers and configuration bits, a 512-bit EEPROM is available on-chip. It can be read and written by the microcontroller via a two-wire serial interface.

The serial interface, the EEPROM and the microcontroller are supplied with the voltage at the V_{DD} pin. That means the microcontroller can read and write the EEPROM if the supply voltage at V_{DD} is in the operating range of the IC.

The Atmel U3280M has built-in operating modes to support a wide range of applications. These modes can be activated via the serial interface with special mode control bytes.

To support applications with battery supply only, power management can be switched off by software to disable the automatic switching to field supply.

An on-chip Bi-phase and Manchester modulator can be activated and controlled by the serial interface. If this modulator is used, it modulates the serial data stream at the serial inputs SDA and SCL into a Bi-phase or Manchester-coded signal for the damping stage.

3.2 Modulation

The transponder interface can modulate the magnetic field by its damping stage to transmit data to a base station. It modulates the coil voltage by varying the coil's load. The modulator can be controlled via the MOD pin. A high level ("1") increases the current into the coil and damps the coil voltage. A low level ("0") decreases the current and increases the coil voltage. The modulator generates a voltage stroke of about 2 V_{pp} at the coil. A high level at the MOD pin makes the maximum of the field energy available at V_{DD}. During reset mode, a high level at the MOD pin causes optimum conditions for starting the device and charging the capacitor at V_{DD} after the field has been applied at the coil.

3.2.1 Digital Input to Control the Damping Stage (MOD)

MOD = 0: coil not damped

$$V_{coil\text{-}peak} = V_{DD} \times \sqrt{2} + V_{CMS} = V_{CU}$$

MOD = 1: coil damped

$$V_{coil\text{-}peak} = V_{DD} \times \sqrt{2} = V_{CD}$$

$V_{CMS} = V_{CID}$: modulation voltage stroke at coil inputs

Note: If the automatic power management is disabled, the internal front-end V_{DD} is limited at V_{DDC}. In this case the value V_{DDC} must be used in the above formula.

3.3 Field Clock

The field clock extractor of the interface makes the field clock available for the microcontroller. It can be used to supply timer inputs to synchronize modulation and demodulation with the field clock.

3.4 Gap Detect

The transponder interface can also receive data. The base station modulates the data with short gaps in the field. The gap-detection circuit detects these gaps in the magnetic field and outputs the NGAP/field signal at the NGAP pin. A high level indicates that a field is applied at the coil and a low level indicates a gap or that the field is off. The microcontroller must demodulate the incoming data stream at one of its inputs.

4. U3280M Signals and Timing

Figure 4-1. Modulation

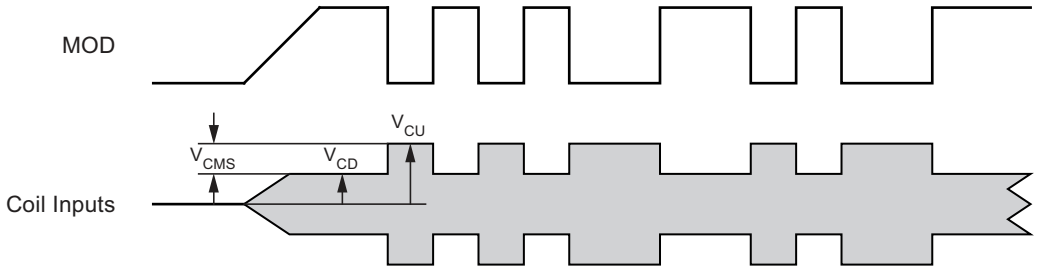
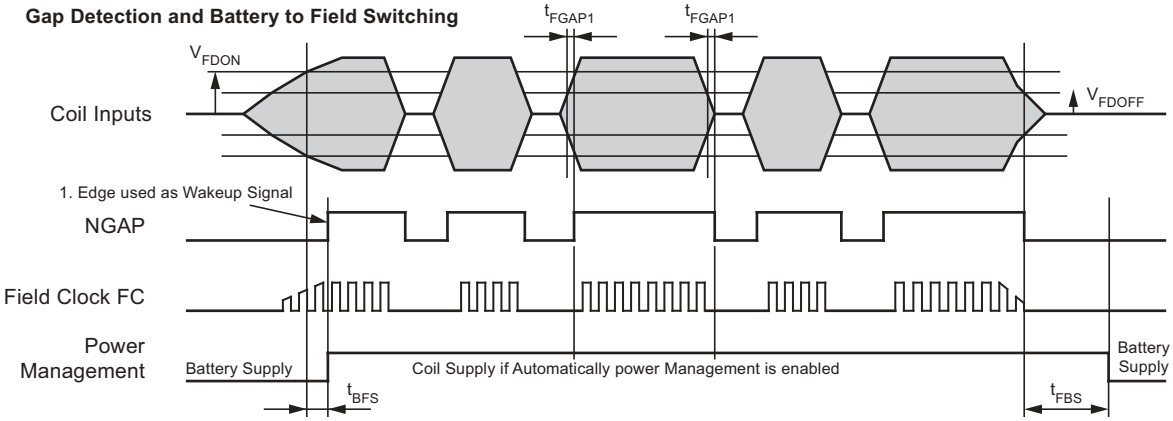


Figure 4-2. GAP and Modulation Timing



4.1 Digital Output of the Gap-detection Stage (NGAP)

NGAP = 0: gap detected/no field $V_{coil\text{-}peak} = V_{FDoff}$

NGAP = 1: field detected $V_{coil\text{-}peak} = V_{FDon}$

Note: No amplifier is used in the gap-detection stage. A digital Schmitt trigger evaluates the rectified and smoothed coil voltage.

4.2 Wake-up Signal

If a field is applied at the coil of the transponder interface, the microcontroller can be woken up with the wake-up signal at the NGAP pin. For that purpose, the NGAP pin must be connected to an interrupt input of the microcontroller. A high level at the NGAP output indicates an applied field and can be used as a wake-up signal for the microcontroller via an interrupt. The wake-up signal is generated if power management switches to field supply. The field-detection stage of the power management has lowpass characteristics to avoid generating wake-up signals and unnecessary switching between battery and field supply in case of interferences at the coil inputs.

4.3 Power Supply

The Atmel® U3280M has a power management that handles two power supply sources. Normally, the IC is supplied by a battery at the V_{Batt} pin. If a magnetic field is applied at the LC-resonant circuit of the device, the field detection circuit switches automatically from V_{Batt} to field supply.

The V_{DD} pin is used to connect a capacitor to smooth the voltage from the rectifier and to buffer the power while the field is modulated by gaps and damping. The EEPROM and the connected controller always operate with the voltage at the V_{DD} pin.

Note: During field supply the maximum energy from the field is used if a high level is applied at the MOD input.

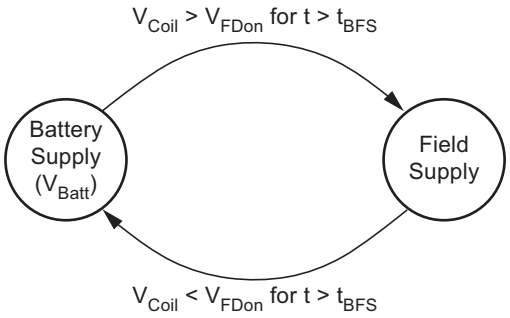
4.3.1 Automatic Power Management

There are different conditions that cause a switch from the battery to field and back from field to the battery.

The power management switches from battery to field if the rectified voltage (V_{coil}) from the coil inputs becomes higher than the field-on-detection voltage (V_{FDon}), even if no battery voltage is available ($0 < V_{Batt} < 1.8V$). It switches back to battery if the coil voltage becomes lower than the field-off-detection voltage (V_{FDoff}).

The field detection stage of the power management has low pass characteristics to suppress noise. An applied field needs a time delay t_{BFS} (battery-to-field switch delay) to change the power supply. If the field is removed from the coil, the power management will generate a reset that can be connected to the microcontroller.

Figure 4-3. Switch Conditions for Power Management



Note: The rectified supply voltage from the coil is limited to V_{DDC} (2.9V). During field supply, the battery is switched off and V_{DD} changes to V_{DDC}.

4.3.2 Controlling Power Management via the Serial Interface

The automatic mode of the power management can be switched off and on by a command from the microcontroller. If the automatic mode is switched off, the IC is always supplied by the battery up to the next power-on reset or to a switch-on command. The power management's on and off command must be transferred via the serial interface.

If the power management is switched off and the device is supplied from the battery, it can communicate via the field without loading the field. This mode can be used to realize applications with battery supply if the field is too weak to supply the IC with power.

4.3.3 Buffer Capacitor C_B

The buffer capacitor connected at V_{DD} is used to buffer the supply voltage for the microcontroller and the EEPROM during field supply. It smooths the rectified AC from the coil and buffers the supply voltage during modulation and gaps in the field. The size of this capacitor depends on the application. It must be of a dimension so that during modulation and gaps the ripple on the supply voltage is in the range of 100mV to 300mV. During gaps and damping the capacitor is used to supply the device, which means the size of the capacitor depends on the length of the gaps and damping cycles.

Table 4-1. Example for a 350µA Supply Current, 200mV Ripple at V_{DD}

No Field Supply During	Necessary C_B
250µs	470nF
500µs	1000nF

4.4 Serial Interface

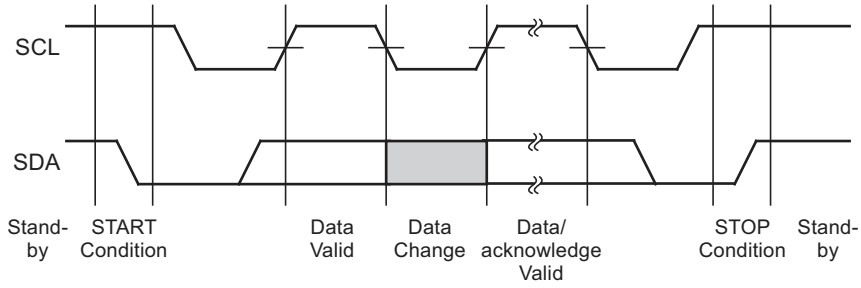
The transponder interface has a serial interface to the microcontroller for read and write access to the EEPROM. In a special mode, the serial interface can also be used to control the Bi-phase/Manchester modulator or the power management of the Atmel® U3280M.

The serial interface of the Atmel U3280M device must be controlled by a master device (normally the microcontroller) which generates the serial clock and controls the access via the SCL and SDA lines. SCL is used to clock the data in and out of the device. SDA is a bi-directional line and used to transfer data into and out of the device. The following protocol is used for the data transfers.

4.4.1 Serial Protocol

- Data states on the SDA line change only when SCL is low.
- Changes in the SDA line while SCL is high will be interpreted as a START or STOP condition.
- A STOP condition is defined as a high-to-low transition on the SDA line while the SCL line is high.
- Each data transfer must be initialized with a START condition and terminated with a STOP condition. The START condition awakens the device from standby mode, and the STOP condition returns the device to standby mode.
- A receiving device generates an acknowledge (A) after the reception of each byte. For that purpose the master device must generate an extra clock pulse. If the reception was successful, the receiving master or slave device pulls down the SDA line during that clock cycle. If an acknowledge has not been detected (N) by the interface in transmit mode, it will terminate further data transmissions and switch to receive mode. A master device must finish its read operation by a not acknowledge and then issue a STOP condition to switch the device to a known state.

Figure 4-4. Serial Protocol



Control Byte Format

	EEPROM address					Mode control bits		Read/ NWrite	
START	A4	A3	A2	A1	A0	C1	C0	R/NW	Ackn

The control byte follows the START condition and consists of the 5-bit row address, 2 mode control bits and the read/not-write bit.

Data Transfer Sequence

START	Control byte	Ackn	Data byte	Ackn	Data byte	Ackn	STOP

- After the STOP condition and before the START condition the device is in standby mode and the SDA line is switched to an input with the pull-up resistor.
- The START condition follows a control byte that determines the following operation. Bit 0 of the control byte is used to control the following transfer direction. A “0” defines a write access and a “1” defines a read access.

5. EEPROM

The EEPROM has a size of 512 bits and is organized as a 32 × 16-bit matrix. To read and write data to and from the EEPROM, the serial interface must be used. The interface supports one and two-byte write access and one to n-byte read access to the EEPROM.

5.1 EEPROM Operating Modes

The operating modes of the EEPROM are defined by the control byte. The control byte contains the row address, the mode control bits and the read/not-write bit that is used to control the direction of the following transfer. A “0” defines the write access and a “1” defines a read access. The five address bits select one of the 32 rows of EEPROM memory to be accessed. For complete access the complete 16-bit word of the selected row is loaded into a buffer. The buffer must be read or overwritten via the serial interface. The two mode control bits C1 and C2 define in which order the access to the buffer is performed: high byte – low byte or low byte – high byte. The EEPROM also supports auto-increment and auto-decrement read operations. After sending the START address with the corresponding mode, consecutive memory cells can be read row by row without transmission of the row addresses.

5.2 Write Operations

The EEPROM allows for 8-bit and 16-bit write operations. A write access starts with the START condition followed by writing a write control byte and one or two data bytes from the master. It is completed with the STOP condition from the master after the acknowledge cycle.

When the EEPROM receives the control byte, it loads the addressed memory cell into a 16-bit read/write buffer. The following data bytes overwrite the buffer. The internal EEPROM programming cycle is started by a STOP condition after the first or second data byte. During the programming cycle, the addressed EEPROM cells are cleared and the contents of the buffer is written back to the EEPROM cells. The complete erase-write cycle takes about 10 ms.

5.2.1 Acknowledge Polling

If the EEPROM is busy with an internal write cycle, all inputs are disabled and the EEPROM will not acknowledge until the write cycle is finished. This can be used to determine when the write cycle is complete. The master must perform acknowledge polling by sending a START condition followed by the control byte. If the device is still busy with the write cycle, it will not return an acknowledge and the master has to generate a STOP condition or perform further acknowledge polling sequences.

If the cycle is complete, the device returns an acknowledge and the master can proceed with the next read or write cycle.

5.2.1.1 Write One Data Byte

START	Control byte	A	Data byte 1	A	STOP

5.2.1.2 Write Two Data Bytes

START	Control byte	A	Data byte 1	A	Data byte 2	A	STOP

5.2.1.3 Write Control Byte Only

START	Control byte	A	STOP
A →acknowledge			

5.2.1.4 Write Control Bytes

Write Low Byte First

MSB LSB

A4	A3	A2	A1	A0	C1	C0	R/NW
Row address					0	1	0

Byte Order

LB(R)	HB(R)

Write High Byte First

MSB LSB

A4	A3	A2	A1	A0	C1	C0	R/NW
Row address					1	0	0

Byte Order

HB(R)	LB(R)

HB: high byte; LB: low byte; R: row address

5.2.2 Read Operations

The EEPROM allows byte-, word- and current address read operations. The read operations are initiated in the same way as write operations. Each read access is initiated by sending the START condition followed by the control byte which contains the address and the read mode. When the device has received a read command, it returns an acknowledge, loads the addressed word into the read/write buffer and sends the selected data byte to the master. The master has to acknowledge the received byte to proceed with the read operation. If two bytes are read out from the buffer, the device automatically increments or decrements the word address and loads the buffer with the next word. The read mode bit determines if the low or high byte is read first from the buffer and if the word address is incremented or decremented for the next read access. When the memory address limit has been reached, the data word address will “roll over” and the sequential read will continue. The master can terminate the read operation after every byte by not responding with an acknowledge (N) and by issuing a STOP condition.

5.2.2.1 Read One Data Byte

START	Control byte	A	Data byte 1	N	STOP

5.2.2.2 Read Two Data Bytes

START	Control byte	A	Data byte 1	A	Data byte 2	N	STOP

5.2.2.3 Read n Data Bytes

START	Control byte	A	Data byte 1	A	Data byte 2	A	- - - - - -	Data byte n	N	STOP

A →acknowledge, N →no acknowledge

5.2.2.4 Read Control Bytes

Read Low Byte First, Address Increment

MSB LSB

A4	A3	A2	A1	A0	C1	C0	R/NW
Row address					0	1	1

Byte Order

LB(R)	HB(R)	LB(R+1)	HB(R+1)	- - - -	LB(R+n)	HB(R+n)

Read High Byte First, Address Decrement

MSB LSB

A4	A3	A2	A1	A0	C1	C0	R/NW
Row address					1	0	1

Byte Order

HB(R)	LB(R)	HB(R-1)	LB(R-1)	- - - -	HB(R-n)	LB(R-n)
HB: high byte; LB: low byte; R: row address						

5.2.3 Initialization after a Reset Condition

The EEPROM with the serial interface has reset circuitry on-chip. In systems with microcontrollers that have their own reset circuitry for power-on reset, watchdog reset or brown-out reset, it may be necessary to bring the Atmel® U3280M into a known state independently of the internal reset. This is performed by reading one byte without acknowledging and then generating a STOP condition.

5.2.4 Special Modes

Table 5-1. Control Byte Description

Control Byte	Description
1100x111b	Bi-phase modulation
1101x111b	Manchester modulation
11xx0111b	Switch power management off --> disables switching from battery to field supply
11xx1111b	Switch power management on --> enables automatic switching between battery and field supply
xxxxx110b	Reserved

Data Transfer Sequence for Bi-phase and Manchester Modulation

START	Control byte	Ackn	Bit 1	Bit 2	Bit 3	- - - - - - - - - -	Bit n	STOP

By using special control bytes, the serial interface can control the modulator stage or the power management. The EEPROM access and the serial interface are disabled in these modes until the next STOP condition. If no START or STOP condition is generated, the SCL and SDA lines can be used for the modulator stage. SCL is used for the modulator clock and SDA is used for the data. In this mode, the same conditions for clock and data changing, as in normal mode, are valid. The SCL and SDA lines can be used for continuous bit transfers, an acknowledge cycle after 8 bits must not be generated.

Note: After a reset of the microcontroller it is not assured that the transponder interface has been reset as well. It could still be in a receive or transmit cycle. To switch the device's serial interface to a known state, the microcontroller should read one byte from the device without acknowledge and then generate a STOP condition.

5.2.5 Power-on Reset, NRST

The Atmel® U3280M transponder front end starts working with the applied field. For the digital circuits like the EEPROM serial interface and registers there is reset circuitry. A reset is generated by a power-on condition at V_{DD}, by switching back from field to battery supply and if a low signal is applied at the NRST-pin.

The NRST-pin is a bi-directional pin and can also be used as a reset output to generate a reset for the microcontroller if the circuit switches over from field to battery supply. This sets the microcontroller in a well-defined state after the uncertain power supply condition during switching.

5.2.6 Antenna

For the transponder interface a coil must be used as an antenna. Air and ferrite cored coils can be used. The achievable working distance (passive mode, not battery assisted) depends on the minimum coupling factor of an application, the power consumption, and the size of the antennas of the IC and the base station. With a power consumption of 150µA, a minimum magnetic coupling factor below 0.5% is within reach. For applications with a higher power consumption, the coupling factor must be increased.

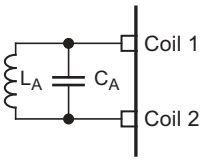
The Q-factor of the antenna coil should be in a range between 30 and 80 for read only applications and below 40 for bi-directional read-write applications.

The antenna coil must be connected with a capacitor as a parallel LC resonant circuit to the Coil 1 and Coil 2 pins of the IC. The resonance frequency f_0 of the antenna circuit should be in the range of 100kHz to 150kHz.

The correct LC combination can be calculated with the following formula:

$$L_A = \frac{1}{C_A \times (2 \times \pi \times f_0)^2}$$

Figure 5-1. Antenna Circuit Connection



Example: Antenna frequency: f_0 = 125kHz, capacitor: C_A = 2.2nF

$$L_A = \frac{1}{2.2\ \text{nF} \times (2 \times \pi \times 125\ \text{kHz})^2} = 737\mu\text{H}$$

6. Absolute Maximum Ratings

Stresses greater than those listed under absolute maximum ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at any condition beyond those indicated in the operational section of these specification is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability. All inputs and outputs are protected against high electrostatic voltages or electric fields. However, precautions to minimize build-up of electrostatic charges during handling are recommended. Reliability of operation is enhanced if unused inputs are connected to an appropriate logic voltage level (for example, V_{DD}).

Voltages are given relative to V_{SS}

Parameter	Symbol	Value	Unit
Supply voltage	V_{DD}, V_{Batt}	0V to +7.0V with reverse protection	V
Maximum current out of V_{SS} pin	I_{SS}	15	mA
Maximum current into V_{Batt} pin	I_{Batt}	15	mA
Input voltage (on any pin)	V_{IN}	V_{SS} –0.6 ≤ V_{IN} ≤ V_{DD} +0.6	V
Input/output clamp current (V_{SS} > Vi/Vo > V_{DD})	I_{IK}/I_{OK}	±15	mA
Min. ESD protection (100pF through 1.5kΩ)		±2	kV
Operating temperature range	T_{amb}	–40 to +85	°C
Storage temperature range	T_{STG}	–40 to +125	°C
Soldering temperature (t ≤ 10s)	T_{SD}	260	°C

7. Thermal Resistance

Parameter	Symbol	Value	Unit
Junction ambient	R_{thJA}	180	K/W

8. DC Characteristics

Supply voltage V_{DD} = 1.8V to 6.5V, V_{SS} = 0V, T_{amb} = –40°C to 85°C unless otherwise specified

Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit
Power Supply							
Operating voltage at V_{Batt}			V_{Batt}	2.0		6.5	V
Operating voltage at V_{DD} during battery supply			V_{DDB}		V_{Batt} – V_{SD}		V
V_{DD}-limiter voltage during coil supply			V_{DDC}	2.6	2.9	3.2	V
Operating current during field supply	V_{DD} > 2.0V		I_{Fi}		40	80	µA
Sleep current			I_{Sl}			0.4	µA
EEPROM							
Operating current during erase/write cycle	V_{DD} = 2.0V V_{DD} = 6.5V		I_{WR} I_{WR}		400	500 1200	µA µA
Operating current during read cycle	V_{DD} = 2.0V V_{DD} = 6.5V Peak current during 1/4 of read cycle		I_{Rdp} I_{Rdp}			300 350	µA µA

8. DC Characteristics (Continued)

Supply voltage V_{DD} = 1.8V to 6.5V, V_{SS} = 0V, T_{amb} = –40°C to 85°C unless otherwise specified

Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit
Power Management							
Field-on detection voltage	V_{DD} > 1.8V		V_{FDon}	2.3	2.5	2.9	V
Field-off detection voltage	V_{DD} > 1.8V		V_{FDoff}		0.8		V
Voltage drop at power-supply switch	I_S = 0.5mA, V_{Batt} = 2V		V_{SD}			150	mV
Coil Inputs: Coil 1 and Coil 2							
Coil input current			I_{CI}			20	mA
Input capacitance			C_{IN}	30			pF
Coil voltage stroke during modulation	V_{CU} > 5V I_{coil} = 3 to 20mA		V_{CMS}	1.8	2.3	4.0	V
Pin MOD							
Input LOW voltage			V_{IL}	V_{IH}		$0.2 \times V_{DD}$	V
Input LOW voltage			V_{IH}	$0.8 \times V_{DD}$		V_{DD}	V
Input leakage current			$I_{Ileakage}$		10		nA
Pin NGAP/FC							
Output LOW current	V_{DD} = 2.0V $V_{OL} = 0.2 \times V_{DD}$		I_{OL}	0.08	0.2	0.3	mA
Output HIGH current	V_{DD} = 2.0V $V_{OH} = 0.8 \times V_{DD}$		I_{OH}	–0.06	–0.15	–0.25	mA
Serial Interface I/O Pins SCL and SDA							
Input LOW voltage			V_{IL}	V_{IH}		$0.3 \times V_{DD}$	V
Input HIGH voltage			V_{IH}	$0.7 \times V_{DD}$		V_{DD}	V
Input leakage current			$I_{Ileakage}$		10		nA
Output LOW current	V_{DD} = 2.0V $V_{OL} = 0.2V_{DD}$ V_{DD} = 6.0V		I_{OL}	0.7 2.8	0.9 3.5	1.1 4.2	mA mA
Output HIGH current	V_{DD} = 2.0V $V_{OH} = 0.8V_{DD}$ V_{DD} = 6.0V		I_{OH}	–0.5 –1.8	–0.6 –2.2	–0.7 –2.6	mA mA

9. AC Characteristics

Supply voltage V_{DD} = 1.8V to 6.5V, V_{SS} = 0V, T_{amb} = –40°C to 85°C unless otherwise specified

Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit
Serial Interface Timing							
SCL clock frequency			f_{SCL}	0		100	kHz
Clock low time			t_{LOW}	4.7			µs
Clock high time			t_{HIGH}	4.0			µs
SDA and SCL rise time			t_R			1000	ns
SDA and SCL fall time			t_F			300	ns
START condition setup time			t_{SUSTA}	4.7			µs
START condition hold time			t_{HDSTA}	4.0			µs
Data input setup time			t_{SUDAT}	250			ns
Data input hold time			t_{HDDAT}	0			ns
STOP condition setup time			t_{SUSTO}	4.7			µs
Bus free time			t_{BUF}	4.7			µs
Input filter time			t_I			100	ns
Data output hold time			t_{DH}	300		1000	ns
Coil Inputs							
Coil frequency			f_{COIL}	100	125	150	kHz
Gap Detection							
Delay field off to GAP = 0	$V_{coilGap} < 0.7V_{DC}$		T_{FGAP0}	10		50	µs
Delay field on to GAP = 1	$V_{coilGap} > 3V_{DC}$		T_{FGAP1}	1		50	µs
Power Management							
Battery to field switch delay			t_{BFS}			1000	µs
Field to battery switch delay	V_{Batt} = 6.5V		t_{FBS}	5	10	30	ms
EEPROM							
Endurance	Erase/write cycles		E_D	500000			Cycles
Data erase/write cycle time	For 16-bit access		t_{DEW}		9	12	ms
Data retention time	T_{amb} = 25°C		t_{DR}	10			years
Power up to read operation			t_{PUR}			0.2	ms
Power up to write operation			t_{PUw}			0.2	ms
Reset							
Power-on reset	V_{DDrise} = 0 to 2V		t_{rise}			10	ms
NRST	VII < $0.2V_{DD}$		t_{res}	1			µs

Figure 9-1. Typical Reset Delay After Switching V_{DD} On

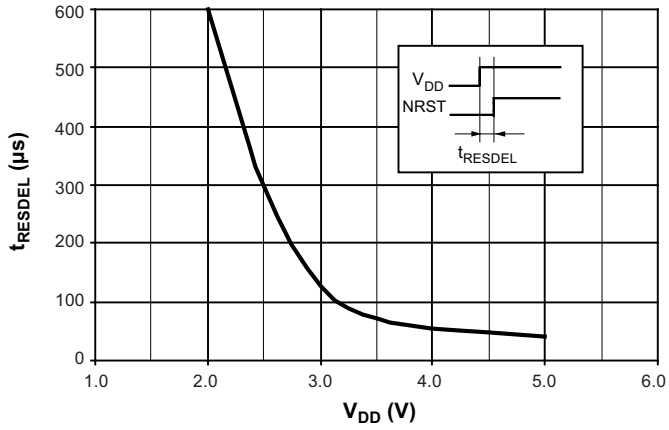


Figure 9-2. Typical Reset Delay After Switching V_{DD} On

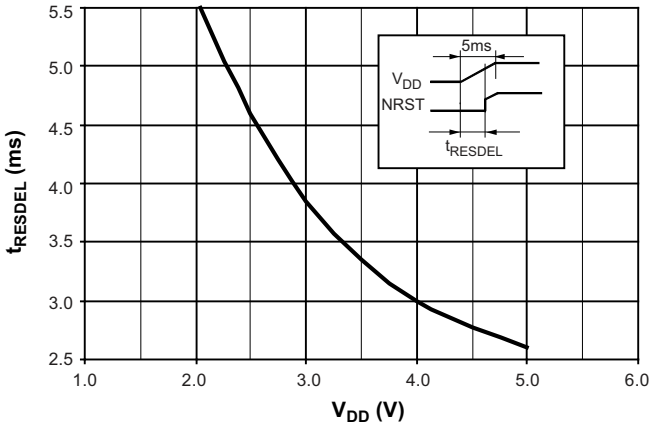
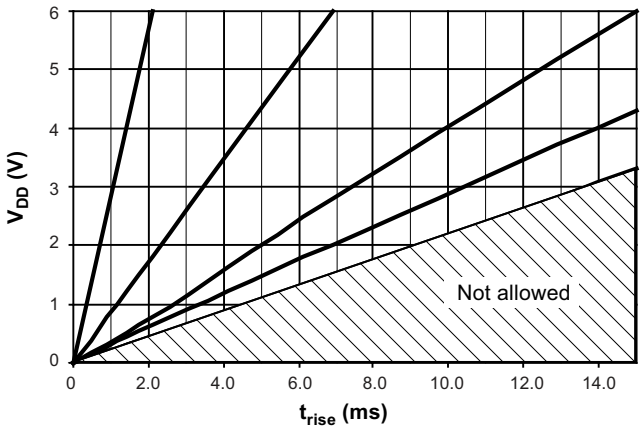


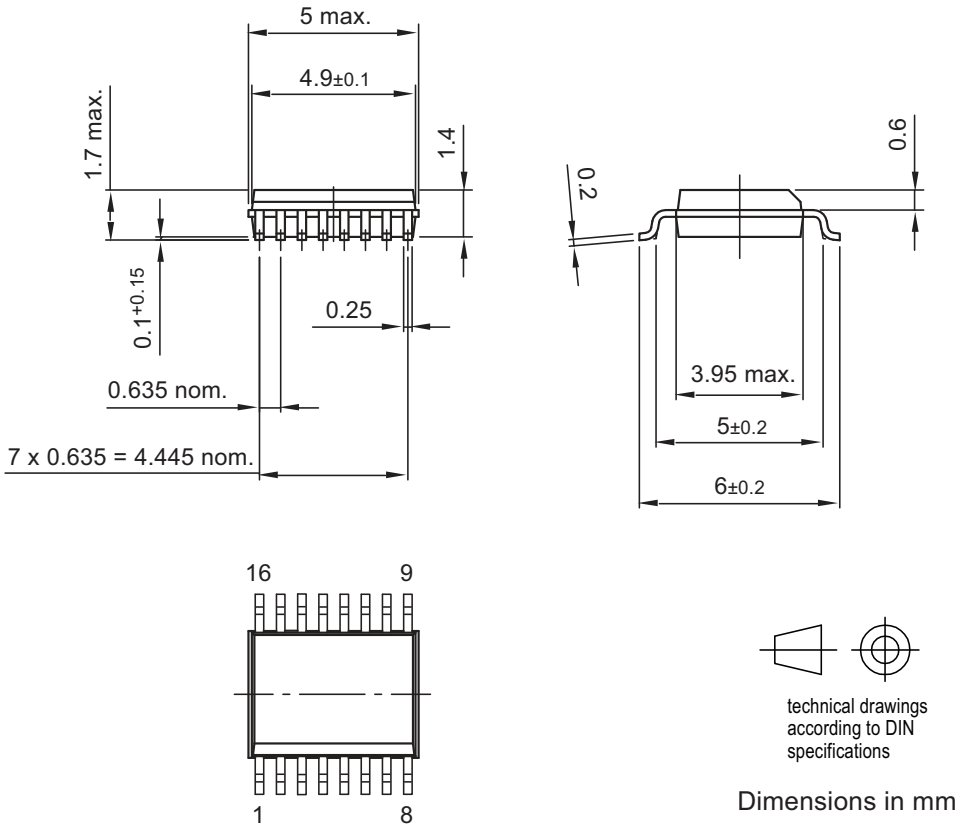
Figure 9-3. V_{DD} Rise Time to Ensure Power-on Reset



10. Ordering Information

Extended Type Number	Package	Remarks
U3280M-NFBY-18	SSO16	Tube, Pb-free
U3280M-NFBG3Y-18	SSO16	Taped and reeled, Pb-free

11. Package Information



Dimensions in mm

Package acc. JEDEC MO 137 AB

02/05/99

	TITLE	GPC	DRAWING NO.	REV.
Atmel Package Drawing Contact: packagedrawings@atmel.com	Package: SSO16		6.543-5060.01-4	2

12. Revision History

Please note that the following page numbers referred to in this section refer to the specific revision mentioned, not to this document.

Revision No.	History
4688E-RFID-05/13	• Section 10 “Ordering Information” on page 17 updated
4688D-RFID-03/07	• Put datasheet in a new template • Pb-free logo on page 1 deleted • Section 5.1 “EEPROM Operating Modes” on page 10 changed
4688C-RFID-09/05	• Put datasheet in a new template • Pb-free logo on page 1 added • Table “Ordering Information” on page 19 changed
4688B-RFID-12/04	• Page 10: Data Transfer Sequence: Text changed • Page 13: Antenna: Text changed • Page 16: Ordering Information table changed

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